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Signal and Power Integrity Analysis of DDR4 Address Bus of Onboard Memory Module

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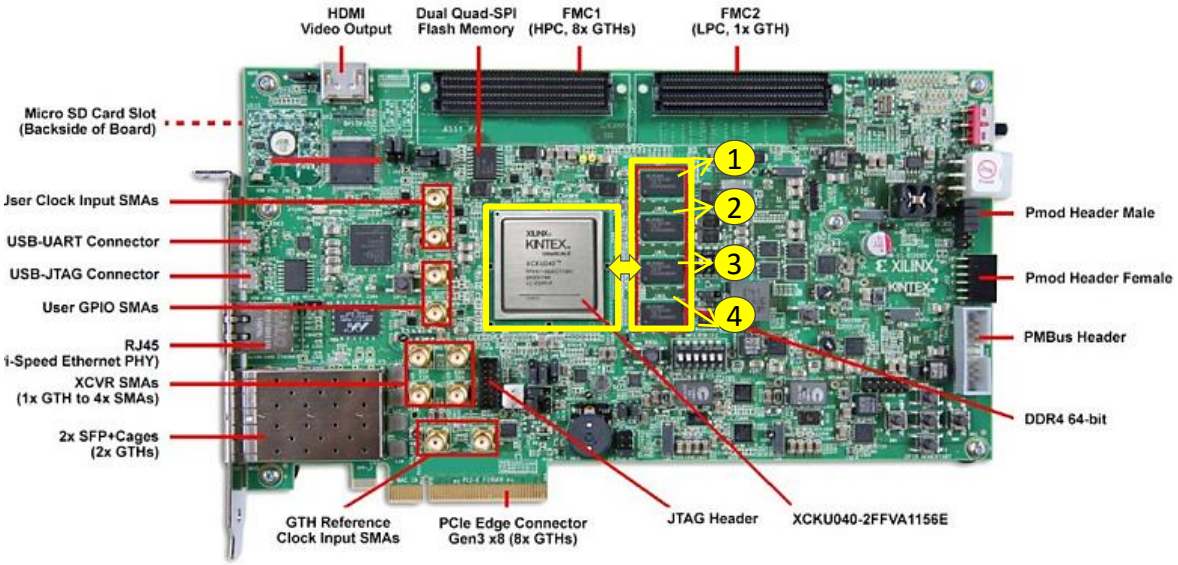
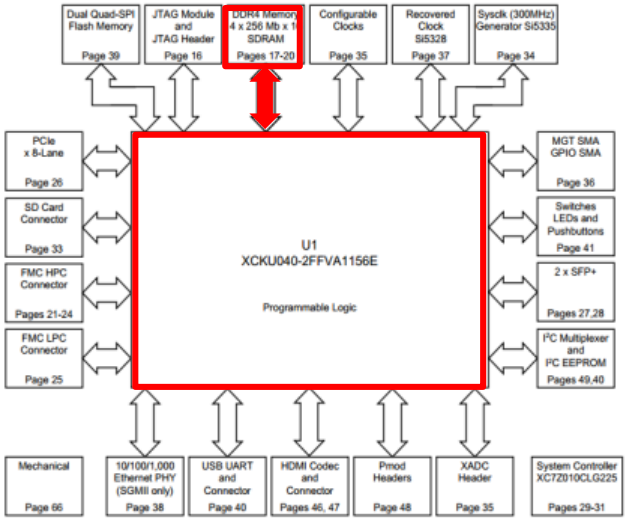
Presentation Outline

- DDR4 Signal Groups
- High Speed Design Challenges
- Address Bus SI-PI Analysis Flow
- Address Bus Power Integrity Analysis
- Address Bus Layout Design and Routing
- DC/AC Simulation and Result
- Electro-Thermal Analysis
- Power Aware SI Simulation of Address Bus

DDR4 Memory: Xilinx FPGA Board





FPGA: Kintex XCKU040-2FFVA1156E FPGA

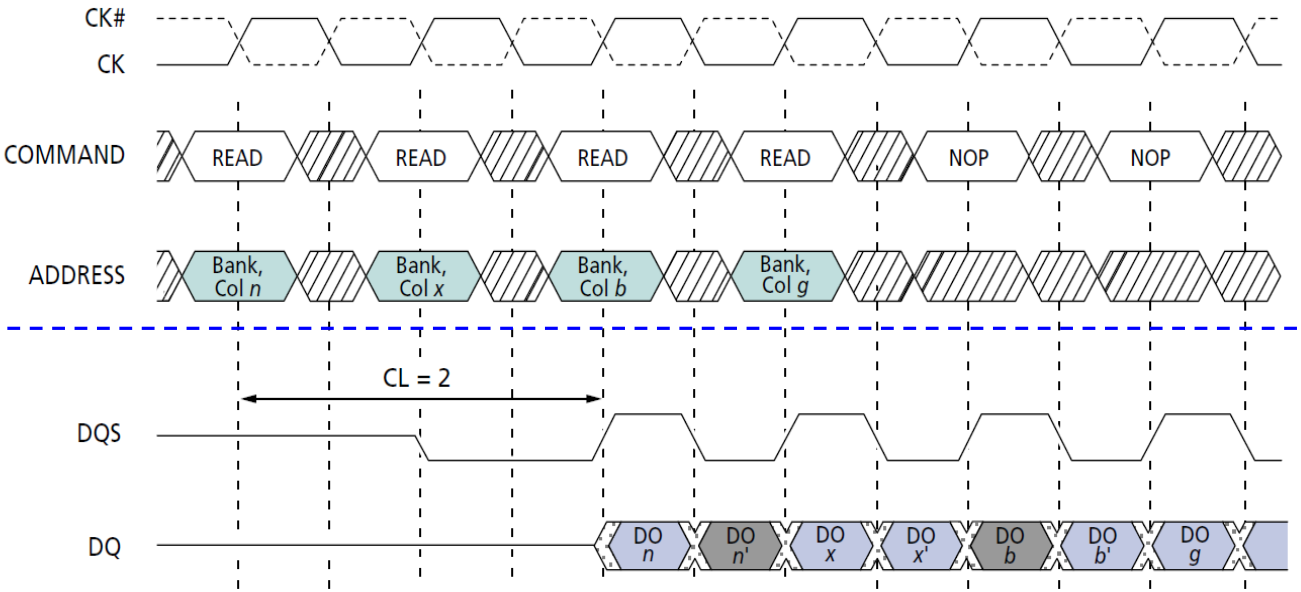
- ROHS compliant KCU105 kit including the XCKU040-2FFVA1156E FPGA

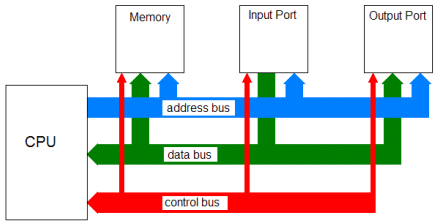
Memory : Micron EDY4016AABG-DR-F-D

- 2GB DDR4 component memory (four [256 Mb x 16] devices) at 1200MHz / 2400Mbpsps

The 2 GB DDR4 component memory system is comprised of four 256 Mb x 16 DDR4 SDRAM devices (Micron **EDY4016AABG-DR-F-D**) located at U60-U63. This memory system is connected to the XCKU040 HP banks 44, 45, and 46. The DDR4 0.6V VTT termination voltage (net **DDR4_VTT**) is sourced from the TI **TPS51200DR** linear regulator U24. The connections between the DDR4 component memories and the XCKU040 banks 44, 45, and 46 are listed

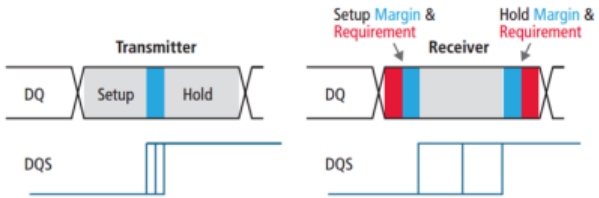
DDR4 Signal Groups





Address Signal (All memory group)
- Power Net : VTT & VCC1v2_FPGA
- Address Lines : A0-A15
- One Clock Pair
- Command Signals
- Decaps

Data Signal (one memory group)
- Power Net : VCC1v2_FPGA
- Data Line : DQ0- DQ15
- Strobe Signal : DQS differential pairs
- One Clock Pair

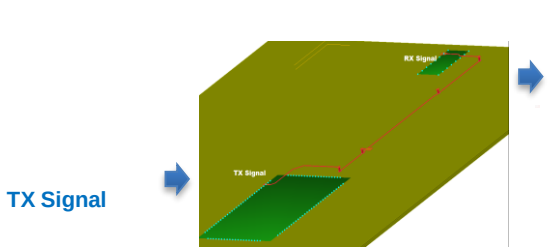


The SI/PI analysis presented here, focuses on the design of the physical layer interface that facilitates communication between the DDR4 module and its controller

High Speed Design Challenges

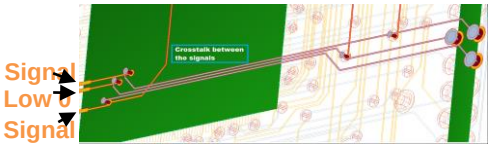
1. Signal Quality of Net :

- Signal distorts due to frequency dependent losses.
- Receiver circuits fails to distinguish between 1 or 0 logic.



2. Crosstalk :

- Caused due to mutual capacitance or inductance between two or more signals.
- Occurs mostly when signals travel parallel to each other for long distances.

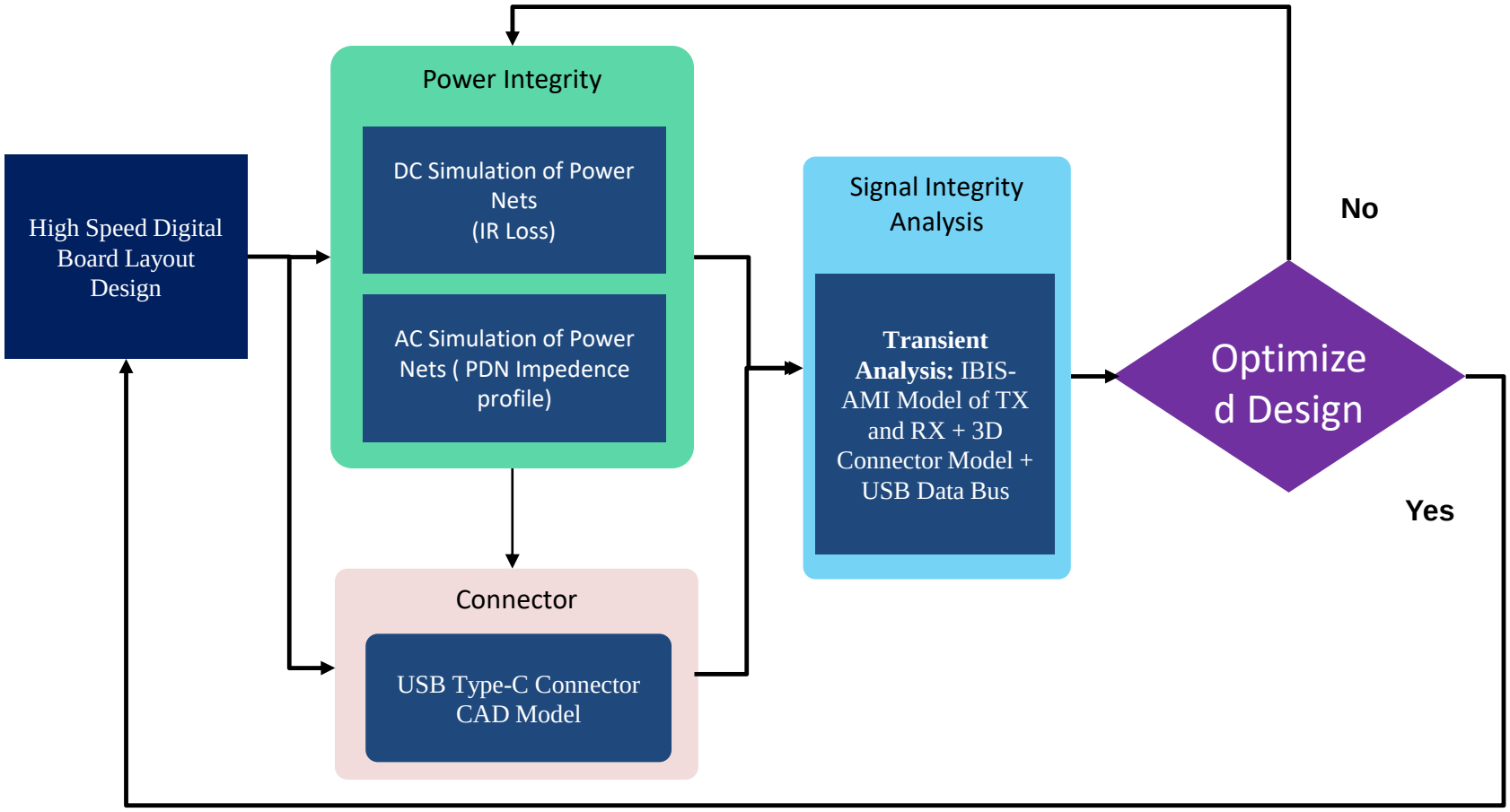


Crosstalk Noise

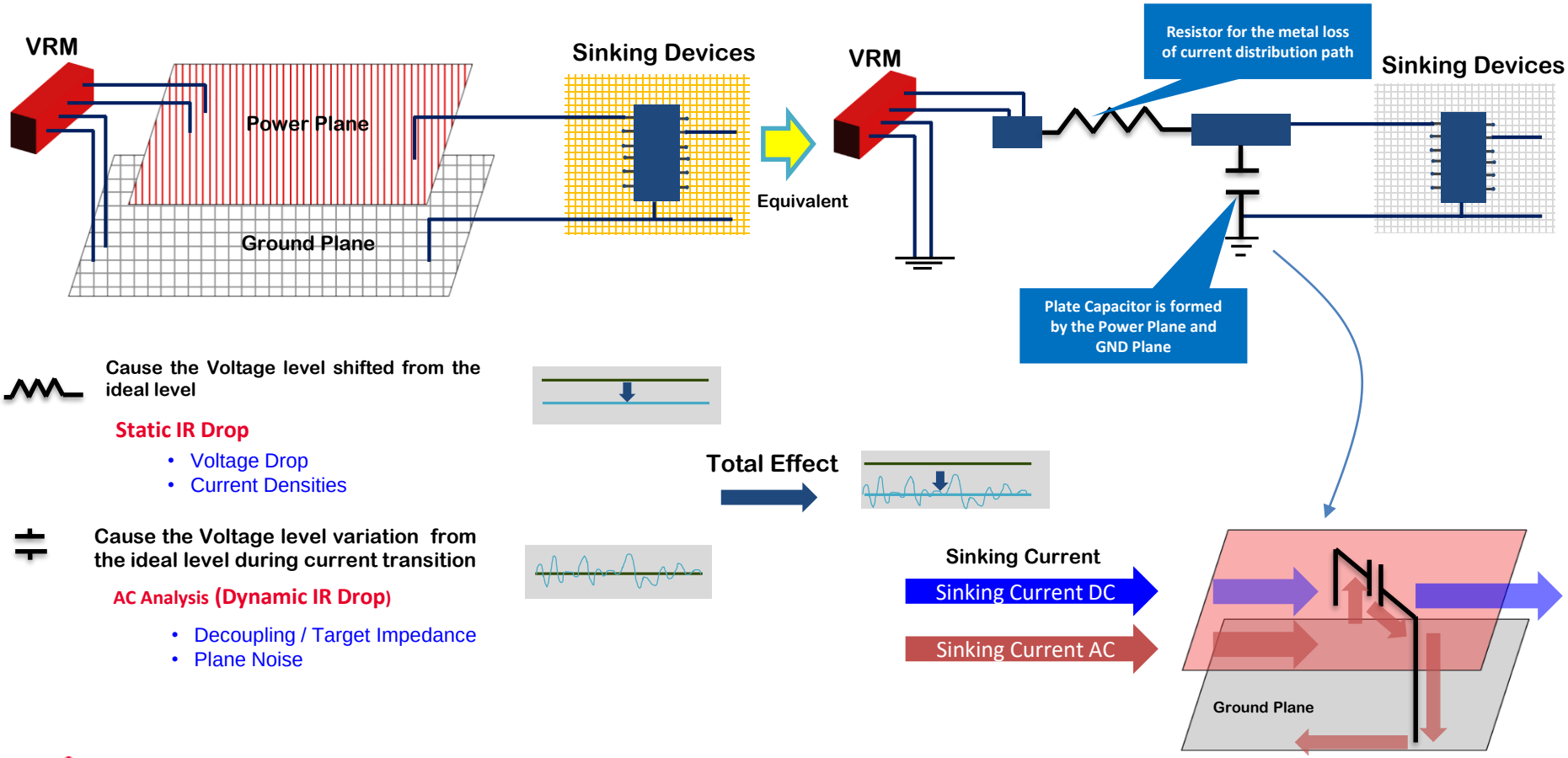
3. Jitter :

- Deviation from ideal clocking position (Power Supply Injected Jitter)

Design Flow


High Speed Digital Board Layout Design
Power Integrity
DC Simulation of Power Nets (IR Loss)
AC Simulation of Power Nets (PDN Impedence profile)
Connector
USB Type-C Connector CAD Model
Signal Integrity Analysis
Transient Analysis: IBIS-AMI Model of TX and RX + 3D Connector Model + USB Data Bus
Optimized Design
No
Yes

Address Bus Power Integrity Analysis



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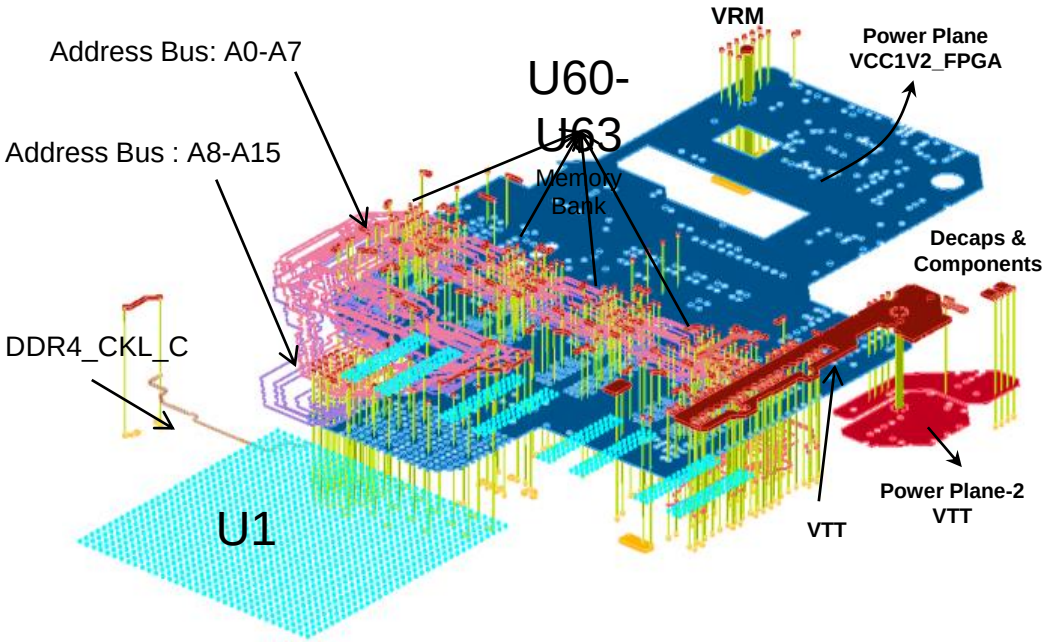
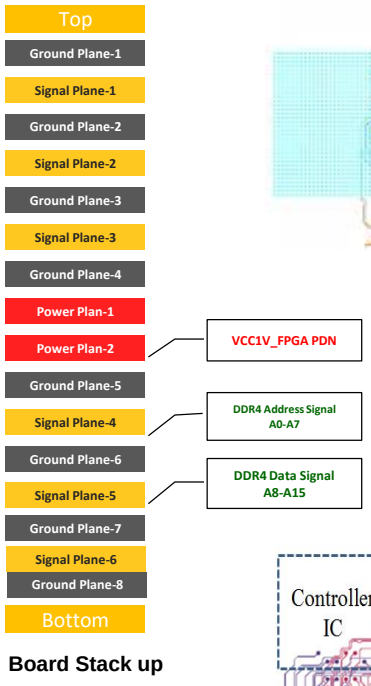
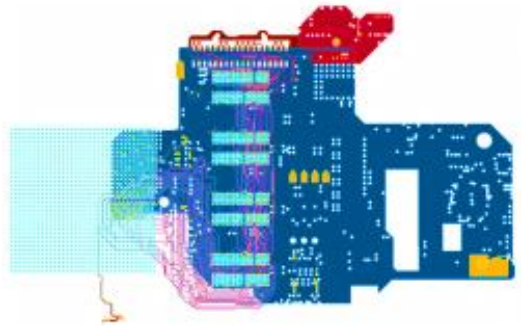
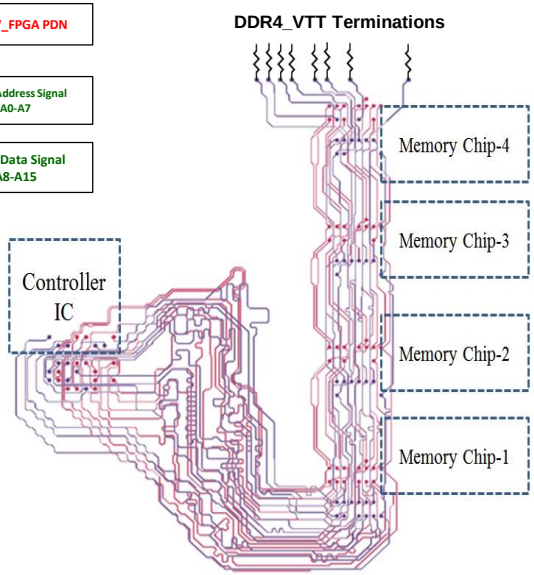
Address Bus Layout Design and Routing





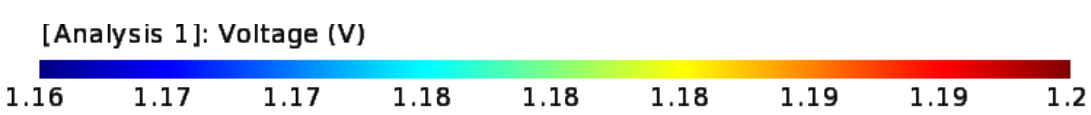
Board Stack up

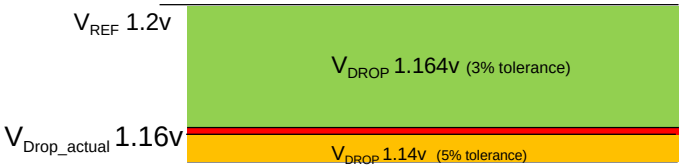


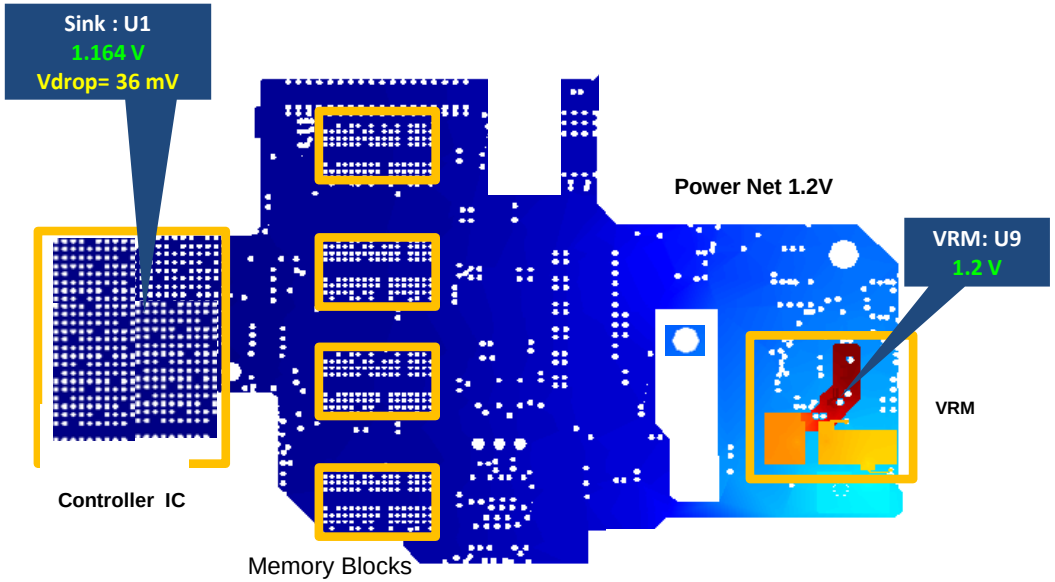


An internal channel from the CPU to memory across which the addresses of data (not the data) are transmitted. The number of lines (wires) in the address bus determines the amount of memory that can be directly addressed as each line carries one bit of the address.

DC Simulation Result – Voltage Drop (Compliance)







With 5% Margin Voltage drop is passing

Sinks | Pins | VRMs | Vias | Reports

	Name	Source Current	VRM Voltage	Input Voltage	Tolerance	Margin	Pass/Fail
1	sink_U60	0.4	1.2	1.16062	0.05	0.02062	pass
2	sink_U61	0.4	1.2	1.16053	0.05	0.02053	pass
3	sink_U62	0.4	1.2	1.16047	0.05	0.02047	pass
4	sink_U63	0.4	1.2	1.16049	0.05	0.02049	pass
5	sink_U1	0.4	1.2	1.15972	0.05	0.01972	pass

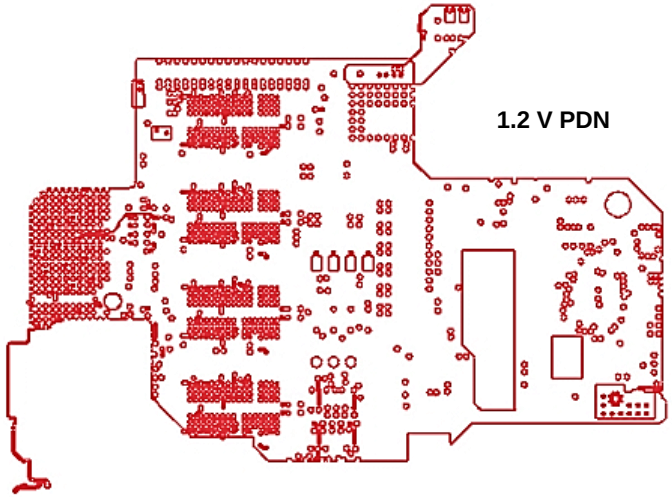
With 3% Margin Voltage drop is failing

Sinks | Pins | VRMs | Vias | Reports

	Name	Source Current	VRM Voltage	Input Voltage	Tolerance	Margin	Pass/Fail
1	sink_U60	0.4	1.2	1.16062	0.03	-0.00338	fail
2	sink_U61	0.4	1.2	1.16054	0.03	-0.00346	fail
3	sink_U62	0.4	1.2	1.16048	0.03	-0.00352	fail
4	sink_U63	0.4	1.2	1.16049	0.03	-0.00351	fail
5	sink_U1	0.4	1.2	1.15972	0.03	-0.00428	fail

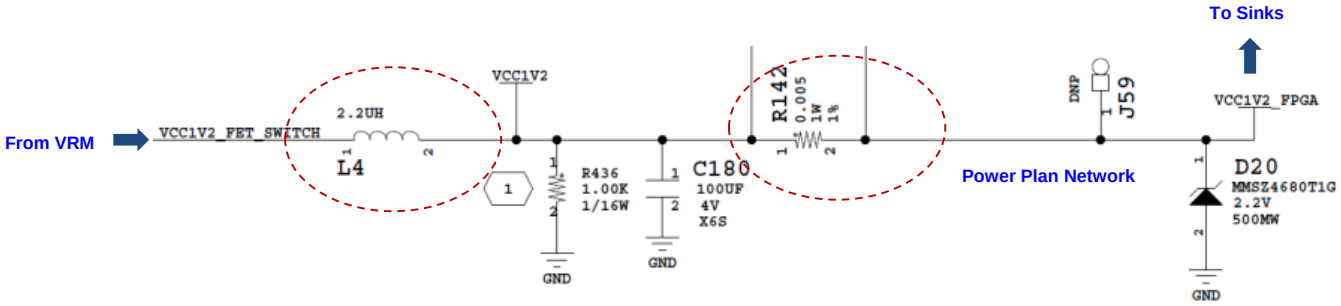
AC Simulation of Power Plane

- AC PI concerns the delivery of AC current to mounted devices to support their switching activity while meeting constraints for transient noise voltage levels within the power delivery network (PDN).
- AC PI is governed by voltage regulator modules, loop inductances, decoupling capacitors (decaps), and plane capacitance.



Target Impedance = % Ripple x VCC/ (Sink Current)$_{Max}$

$$Z_{Target} = \frac{\Delta V_{voltage\ tolerance}}{\Delta I} = \frac{Vcc * Ripple\%}{Current\ \text{Transient}}$$



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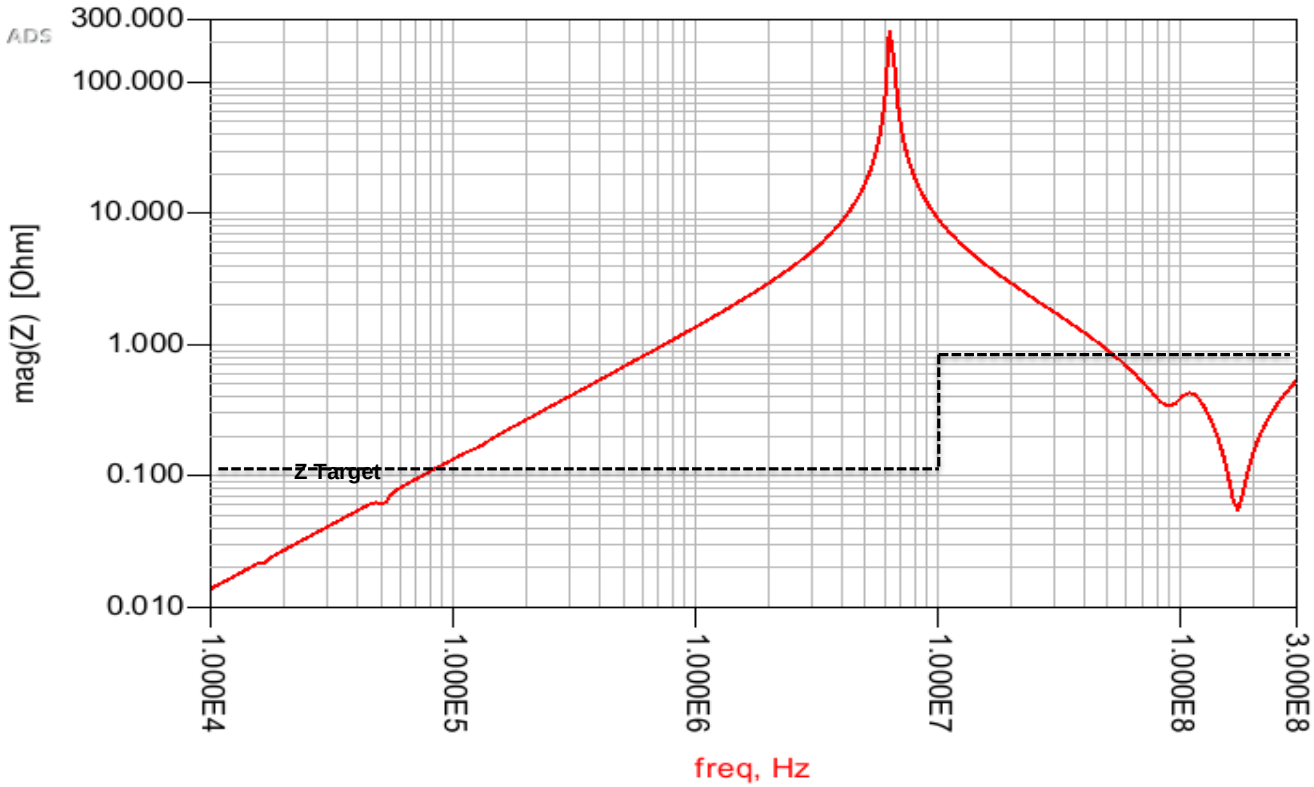
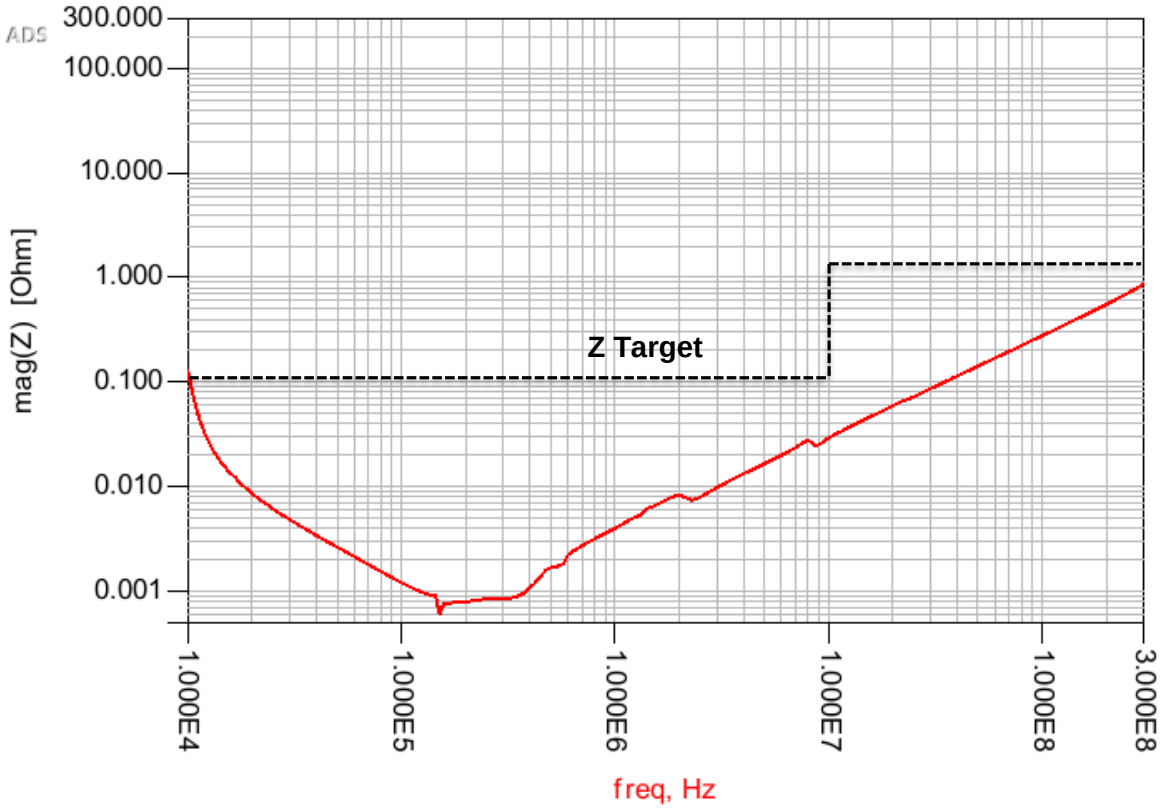
AC Simulation Result – PDN Plot without Decaps

"Target impedance" profiles are applied as PI constraints. Lower impedance corresponds to lower transient noise



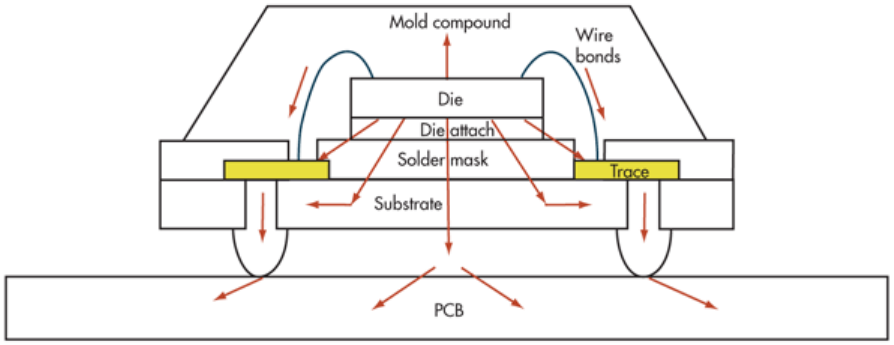
AC Simulation Result – PDN Plot with Decaps

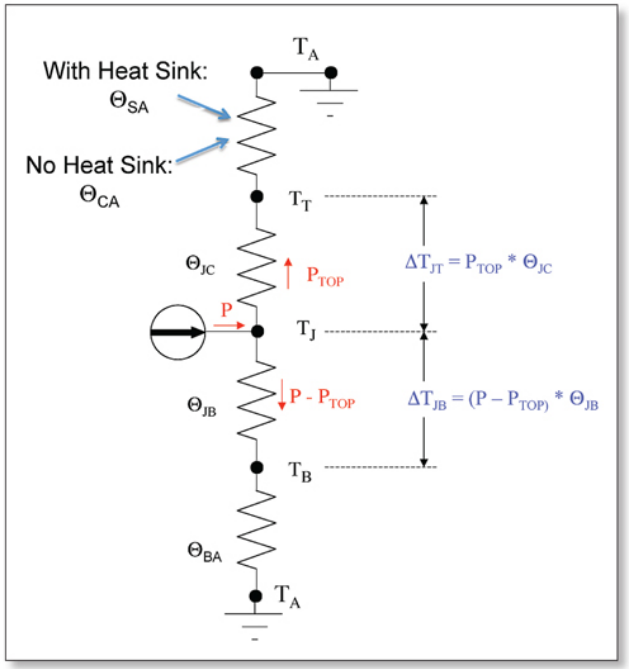


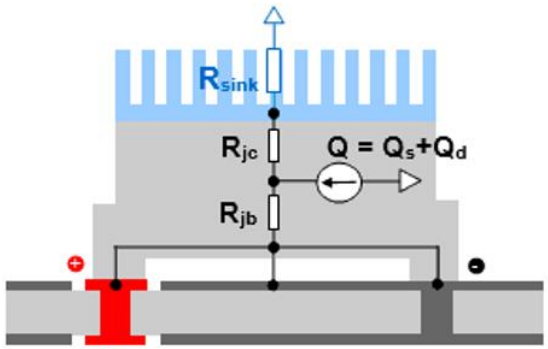
- It is difficult to get a reliable reference to capacitor quantity only by experience.
- AC simulation get an effective power solution by iterating capacitor quantity and distribution

Electro-Thermal Analysis

- The electro-thermal analysis performs a thermal aware IR Drop analysis.
- It computes the voltage, IR drop, current, power loss density, and temperature distribution in a PCB taking into account the Joule losses in the metallization and the heat generation by the components.
- The heat is transferred away from the sources to the surrounding ambient by conduction through materials, convection with surrounding air, and direct radiation.
- It leads to a temperature rise in the components and the PCB, what in turns leads to an increase in electrical resistance of the metallization.







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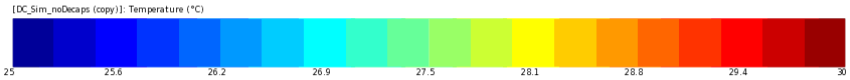
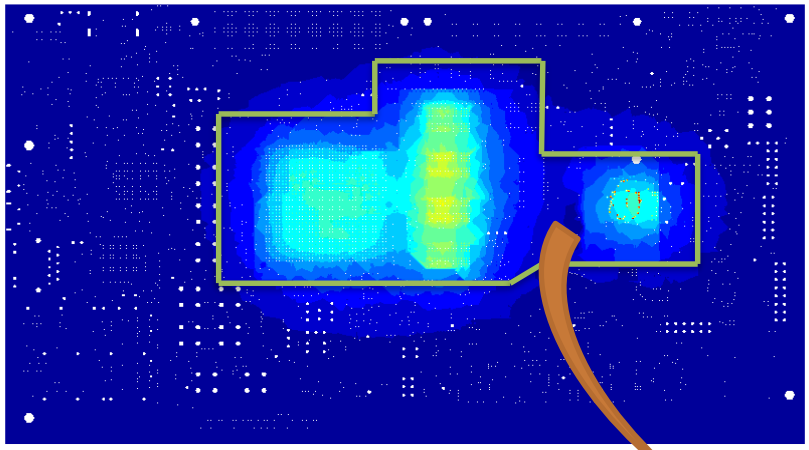
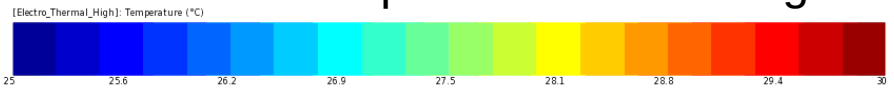
Thermal and Electro-Thermal Analysis

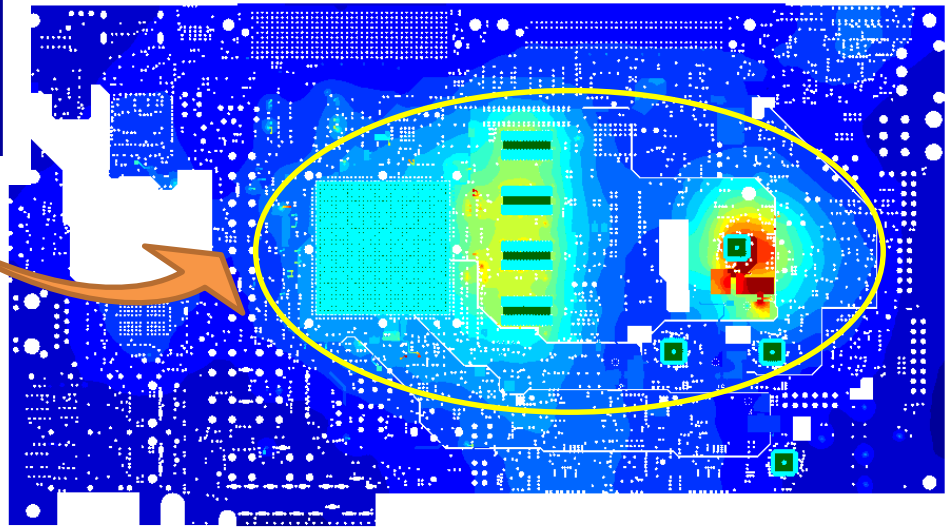


Thermal Only Analysis



Temperature rise : 5 deg C





Elctro- Thermal Only IR DropAnalysis

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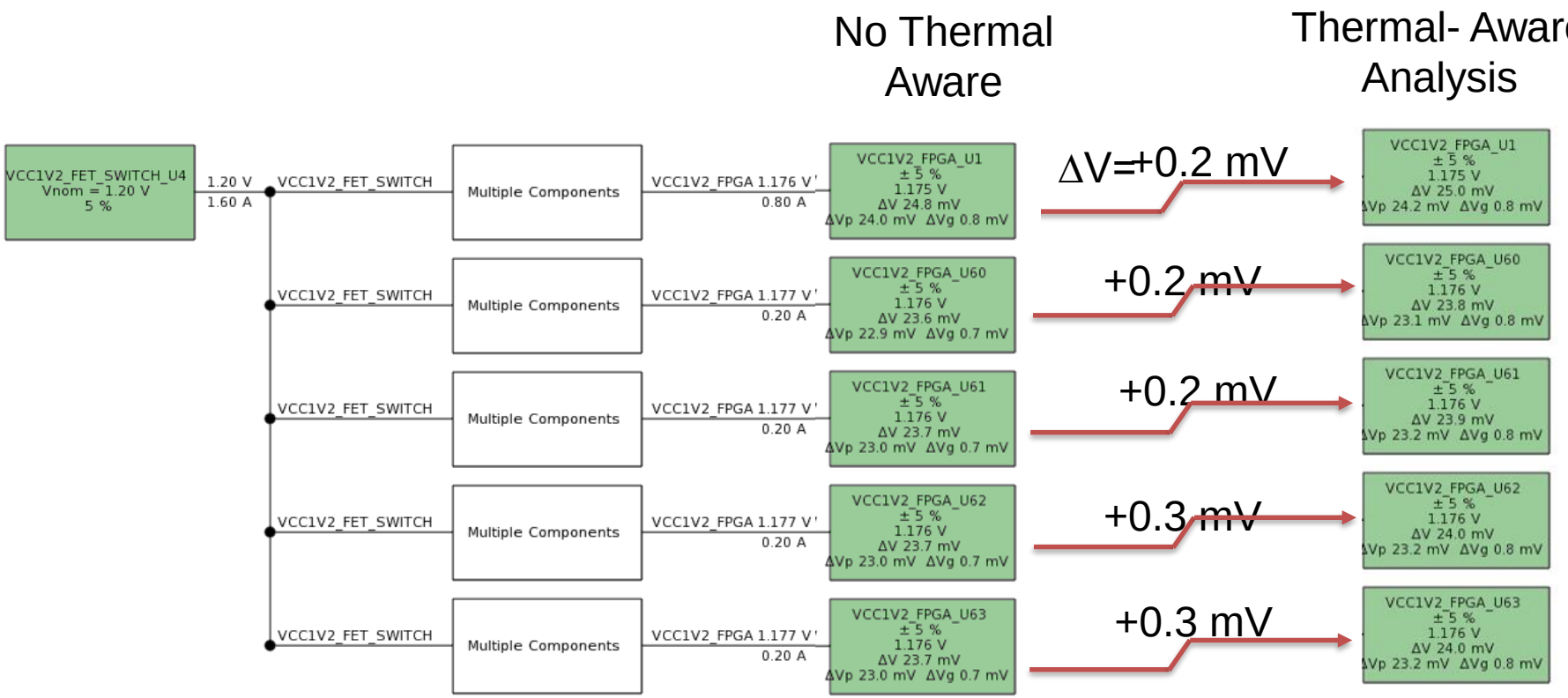
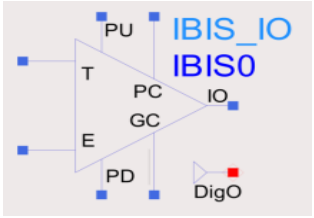
Thermal and Electro-Thermal Analysis Result



Power Aware IBIS v5.0 Models

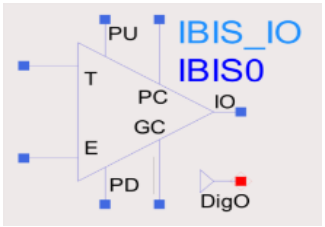
- IBIS (Input/output Buffer Information Specification) models are behavioral using I-V and V-t look-up tables that make simulations extremely fast
- There are two BIRDs related to the power awareness of the IBIS v5.0 models
  - The first power aware BIRD is 95.6 : Power Integrity Analysis using IBIS
  - The second power aware BIRD is 98.3. : Gate Modulation Effect

RX IBIS Model



EDY4016AABG-DR-F

TX IBIS Model



Kintex XCKU040-2FFVA1156E FPGA

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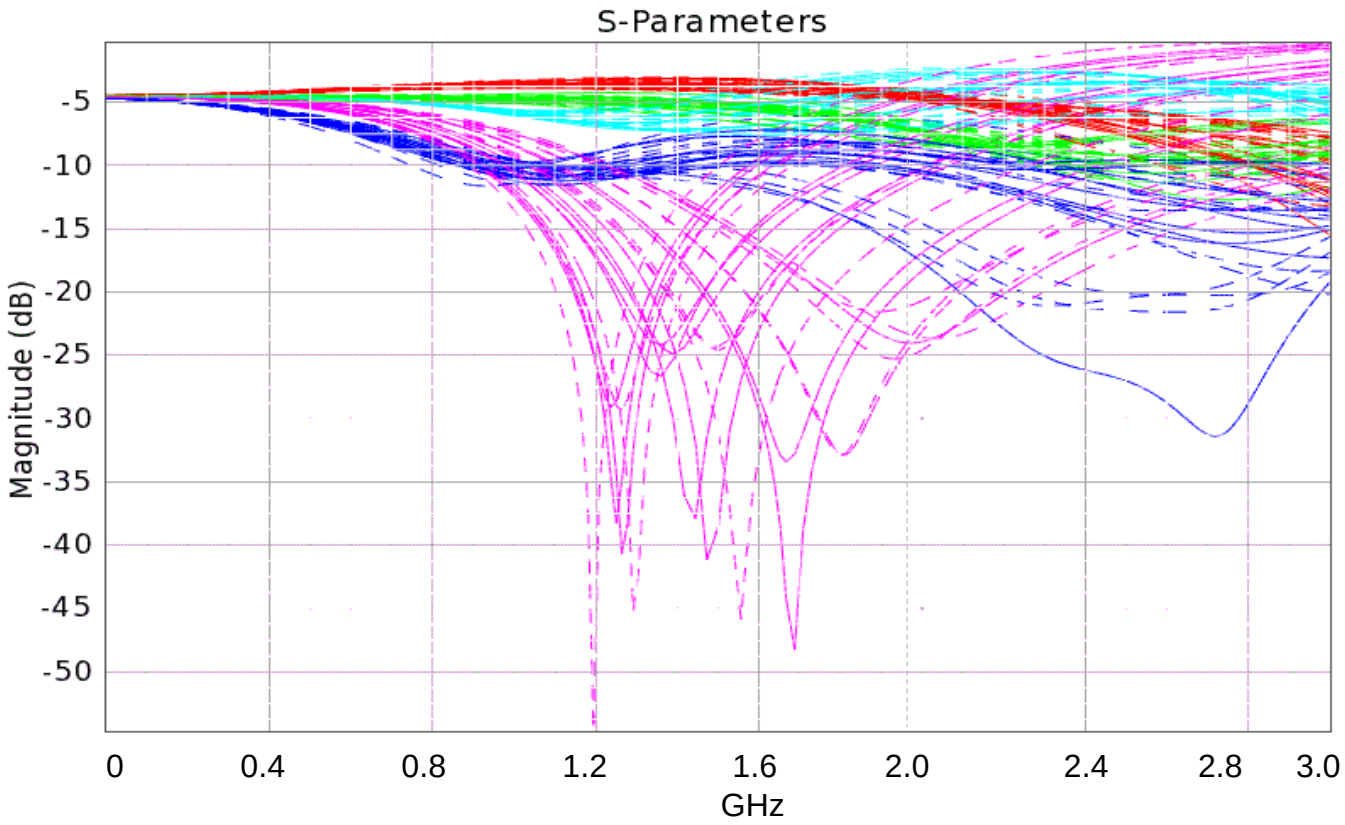
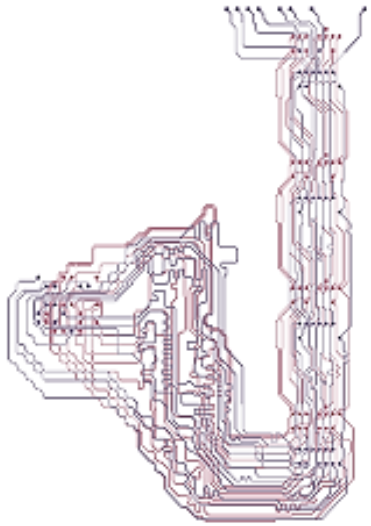
Address Bus S-Parameter Simulation Result





VRM → Sinks → Components → Simulation → Result

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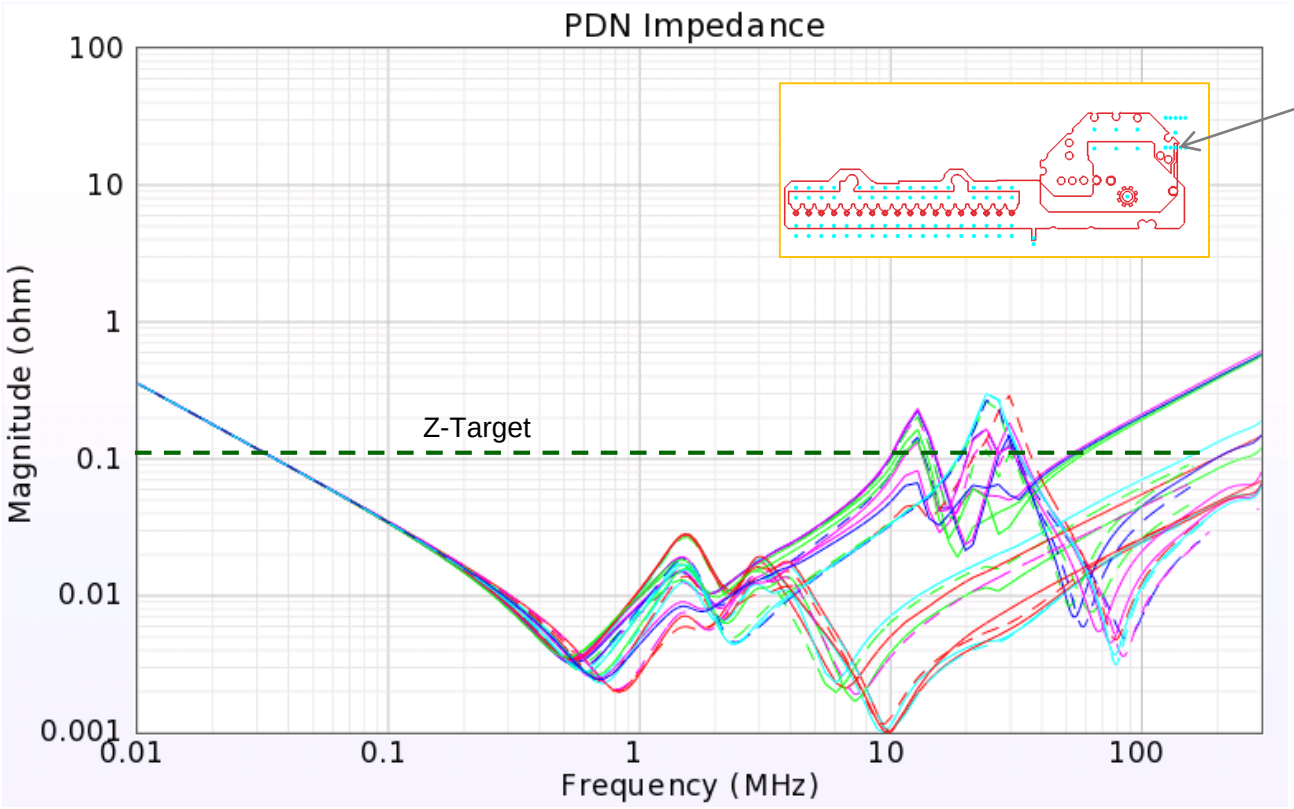
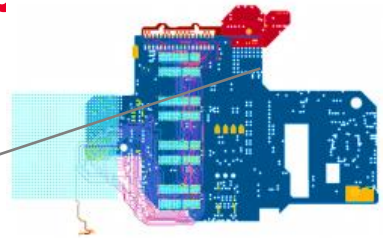
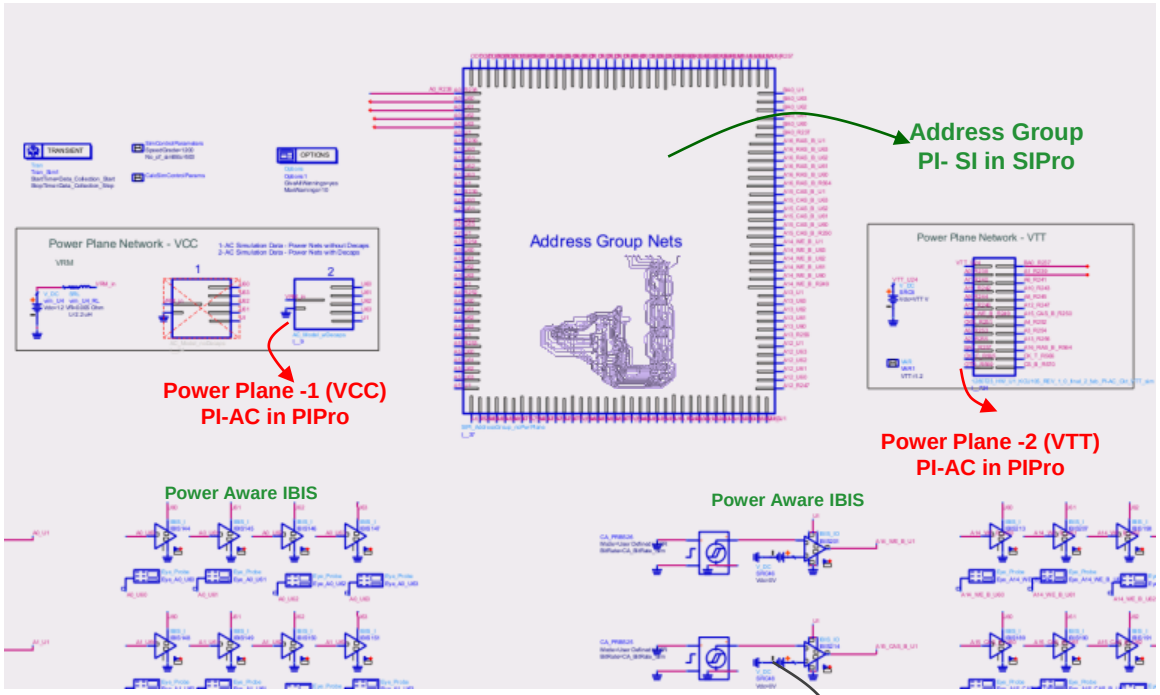
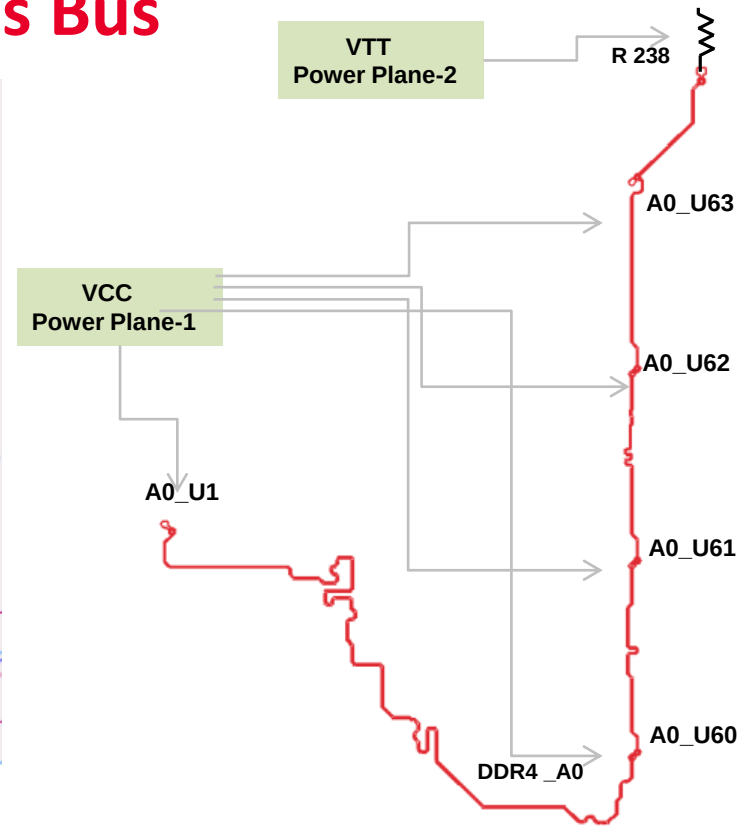
VTT Power Plane : PI-AC Simulation (With Decaps)

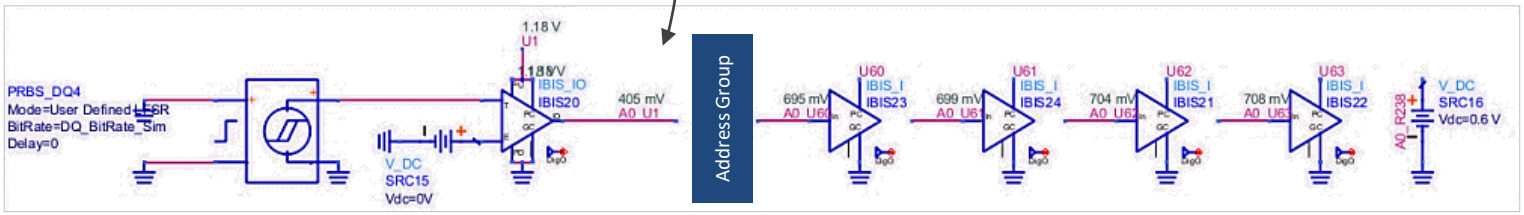




Power Aware SI Simulation of Address Bus







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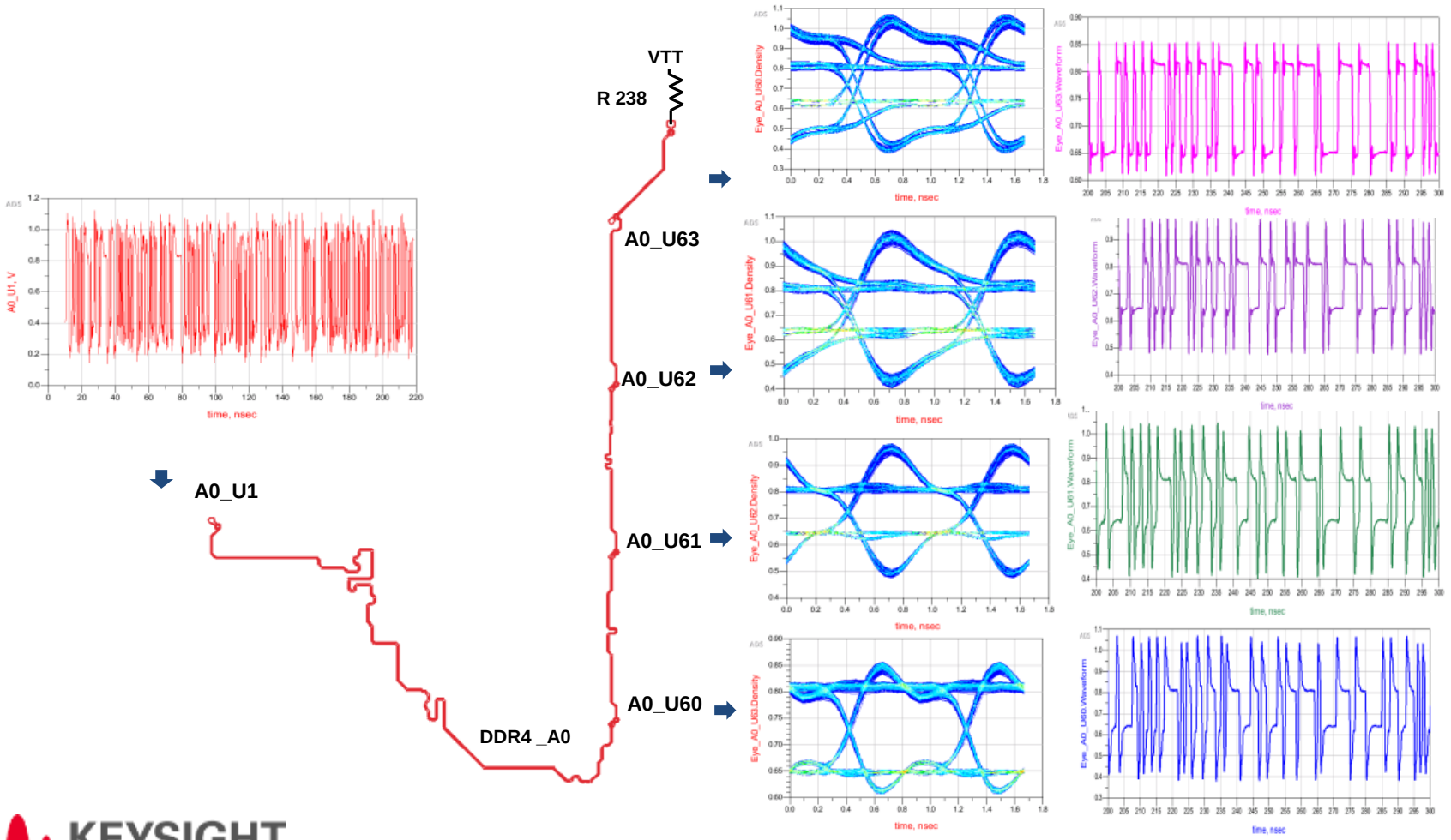
Address Bus Power Aware SI Simulation : Result



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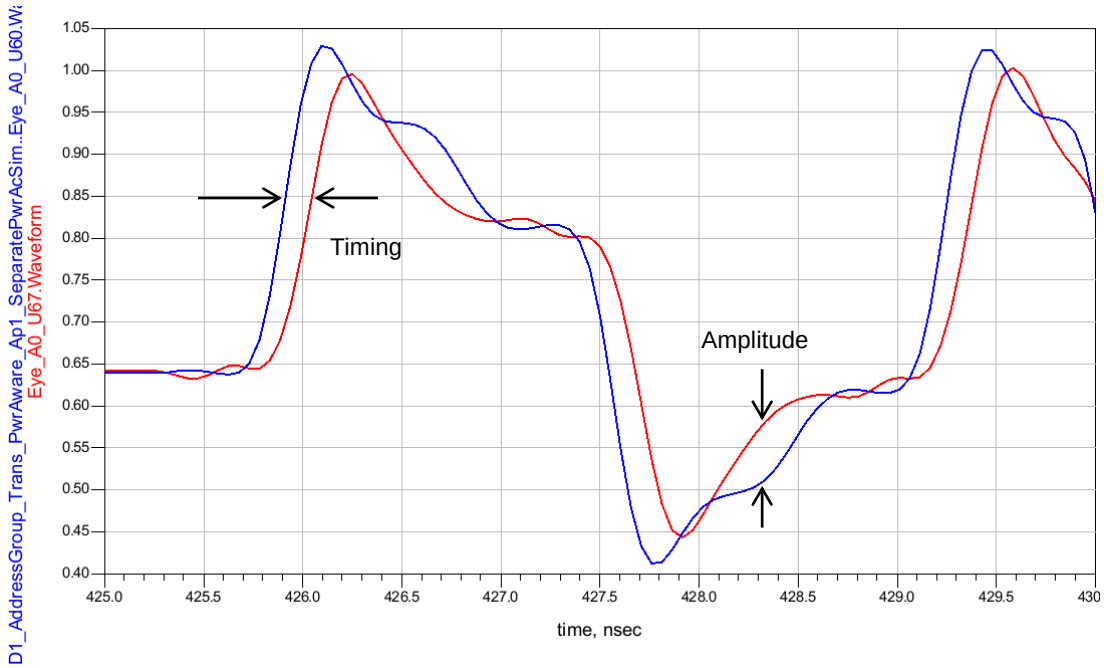
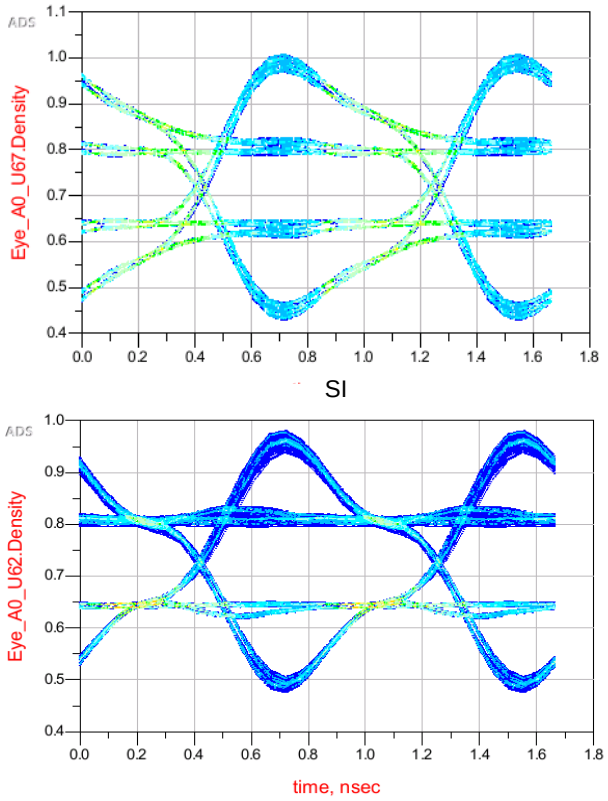
Address Bus Power Aware SI Simulation Result

(with and without Power Aware)





Blue- Without Power Plane
Red- With Power Plane (Power Aware SI)

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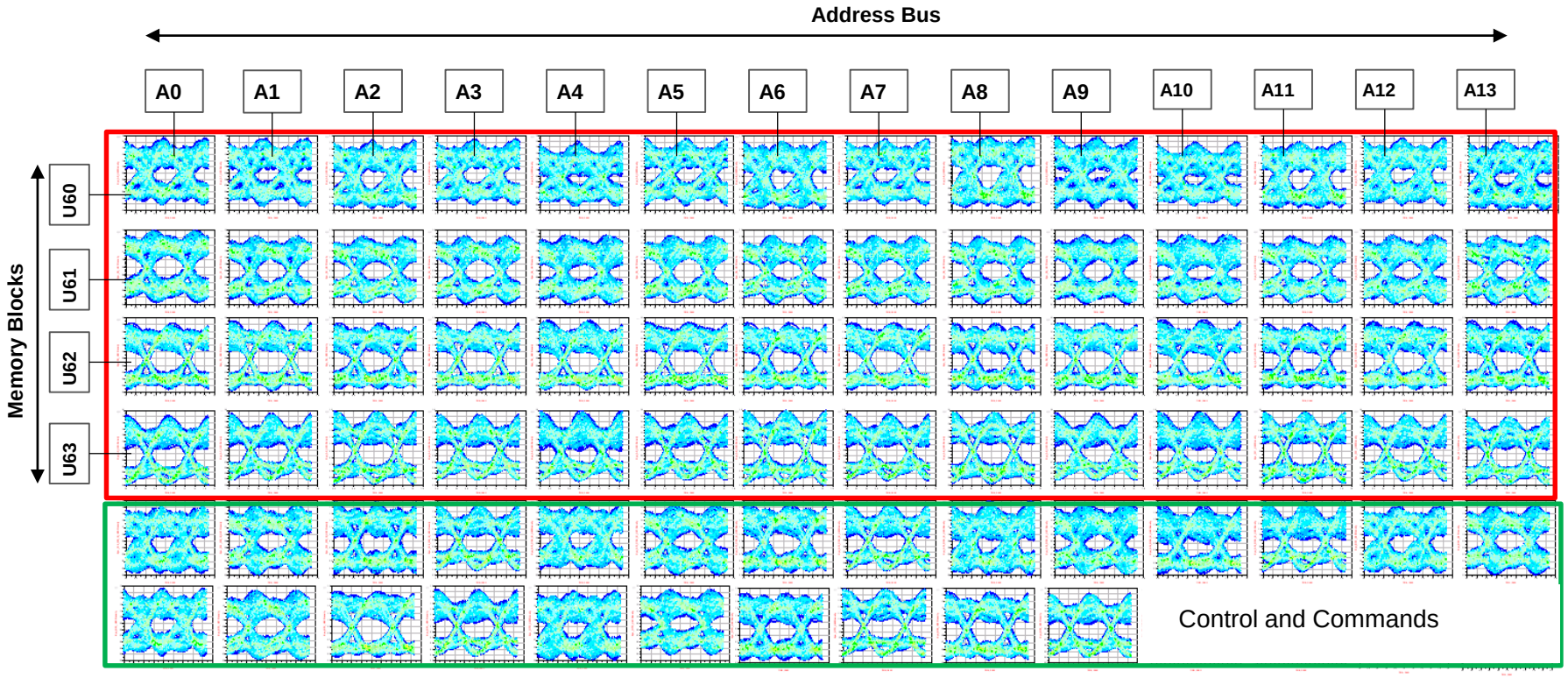
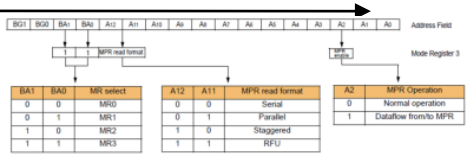
Address Bus Eye Diagram (Power Aware SI Simulation)





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Conclusion

- A transient co-simulation methodology is presented on FPGA board design to characterized DDR4 address bus based on power and thermal-aware signal integrity analysis.
- This analysis approach can be extended in high-speed SerDes designs (like PCIe, USB, HDMI) also.

Thank you