EDI CON 2019
Electronic Design Innovation Conference
电子设计创新大会
April 1-3, 2019
China National Convention Center
Beijing, China

How to Design a Reliable Power Distribution Network Through Chip/Package/PCB Co-Design

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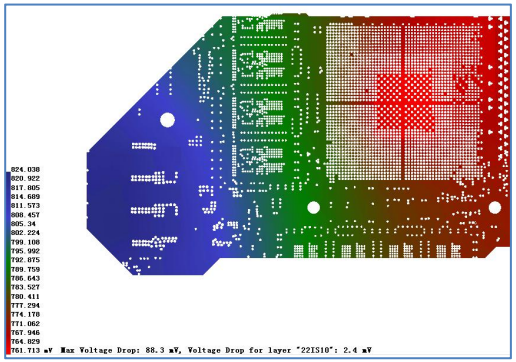
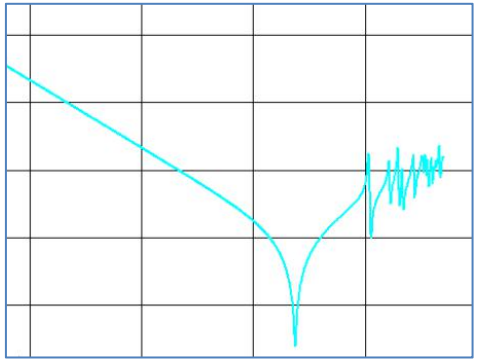
With the increase of chip rate, the decrease of core voltage and the rise of current, PCB PDN design is one of the main challenges of the PCB design. Because PDN design has its own characteristic, so one kind of power supply design scheme is generally cannot be copied to another case, EDI CON convention in March 2018 speech we mentioned it is difficult to obtain the CPM model but is something worth doing. It is very lucky, we get some model,through the Chip/package/PCB co-simulation,We optimize the performance of the power supply, reduce the cost of the product, improve the performance of the product. This paper mainly focuses on the research of the target impedance under the actual working current of the chip,introduce a method to meet the chip noise specification.

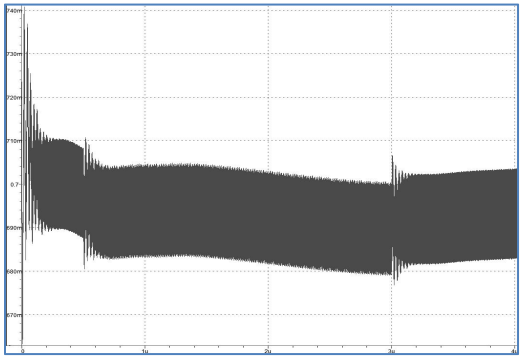
Agenda

- ✓ The Goal of PDN Designing
- ✓ General PDN Simulation Flow
- ✓ Chip Power Model
- ✓ Characteristic Impedance Simulation
- ✓ Transient Analysis
- ✓ Conclusion

The Goal of PDN Designing







DC IR DROP

Impedance for AC

Transient Analysis

Setup/Hold Margin Reduction

Bit Error Rate for serial links

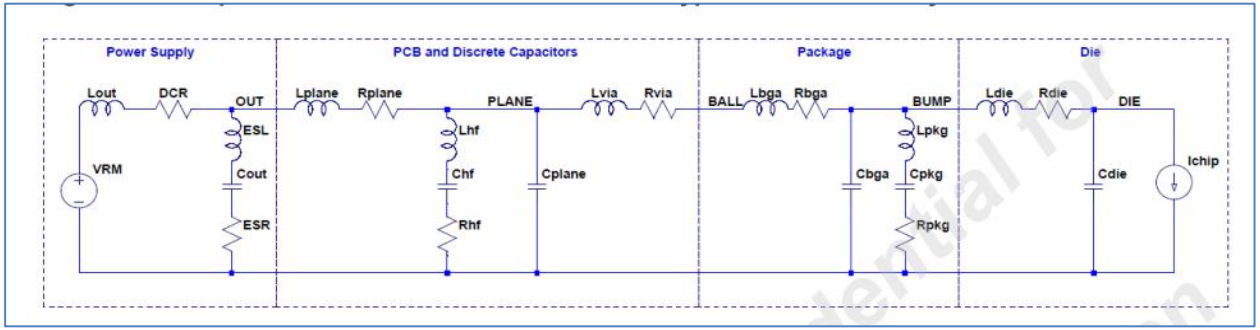
SSN

EMC Noise

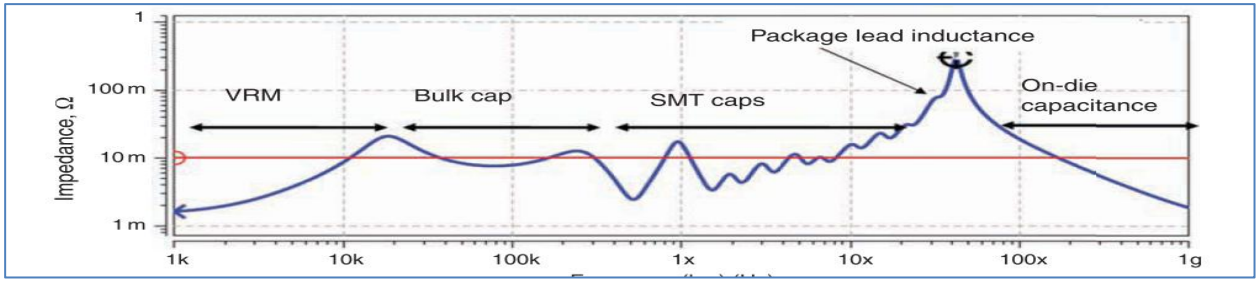
100GBASE-KR4 requires <150mUI of deterministic jitter

General PDN Simulation Process

- ✓ How much drop is ok
- ✓ What is the cutoff frequency of PCB
- ✓ What does the current waveform look like



$$Z_{target} = \frac{Vdd \times tolerance}{I_{transient}}$$



Chip Power Model

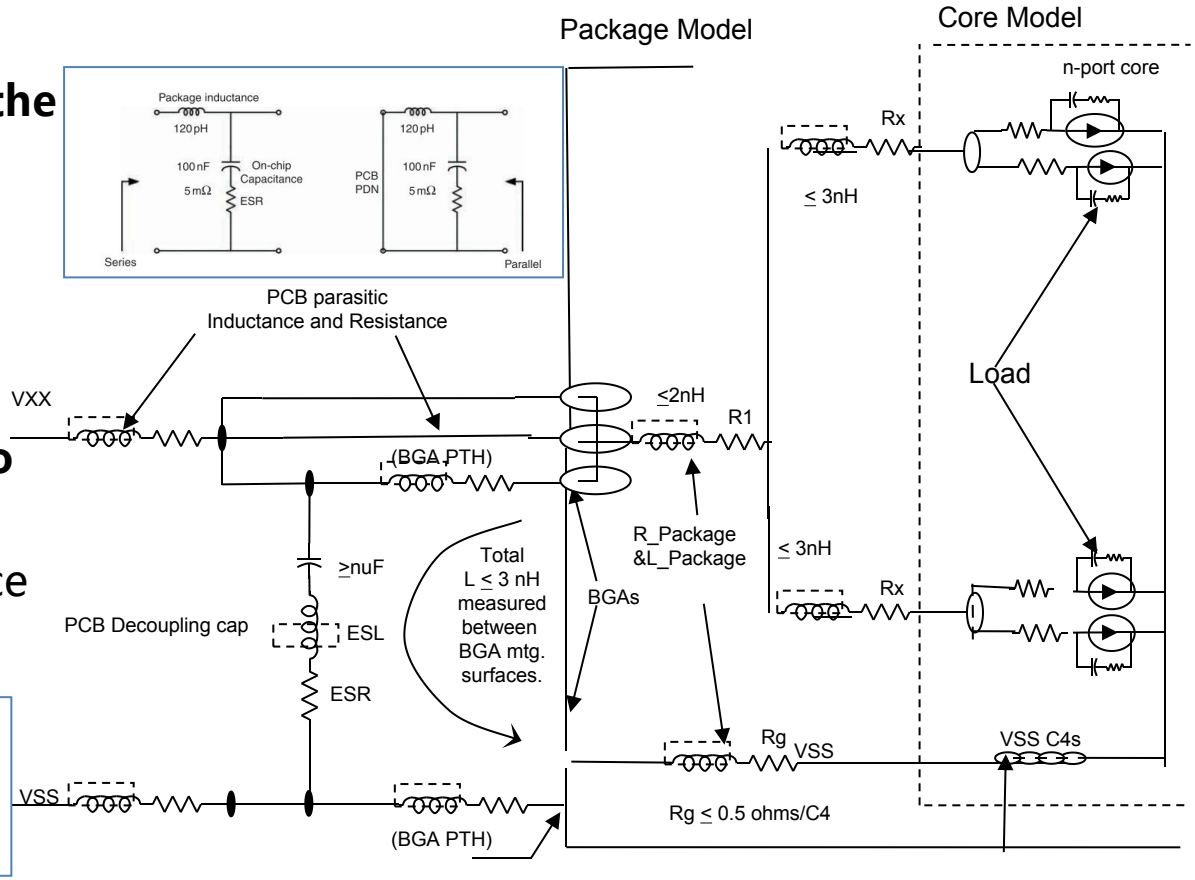
System power analysis with the CPM model can predict

- Noisy in the die
- Noise at the bumps
- Frequency resonance
- Optimize PCB decaps

Transient analysis can help to

- Find the best solutions
- Tradeoffs for die capacitance and package decaps

$$f_{Bandini}[MHz] = \frac{1}{2\pi\sqrt{L_{pkg}C_{ODC}}} = \frac{159\ MHz}{\sqrt{L_{pkg}[nH]C_{ODC}[nF]}}$$



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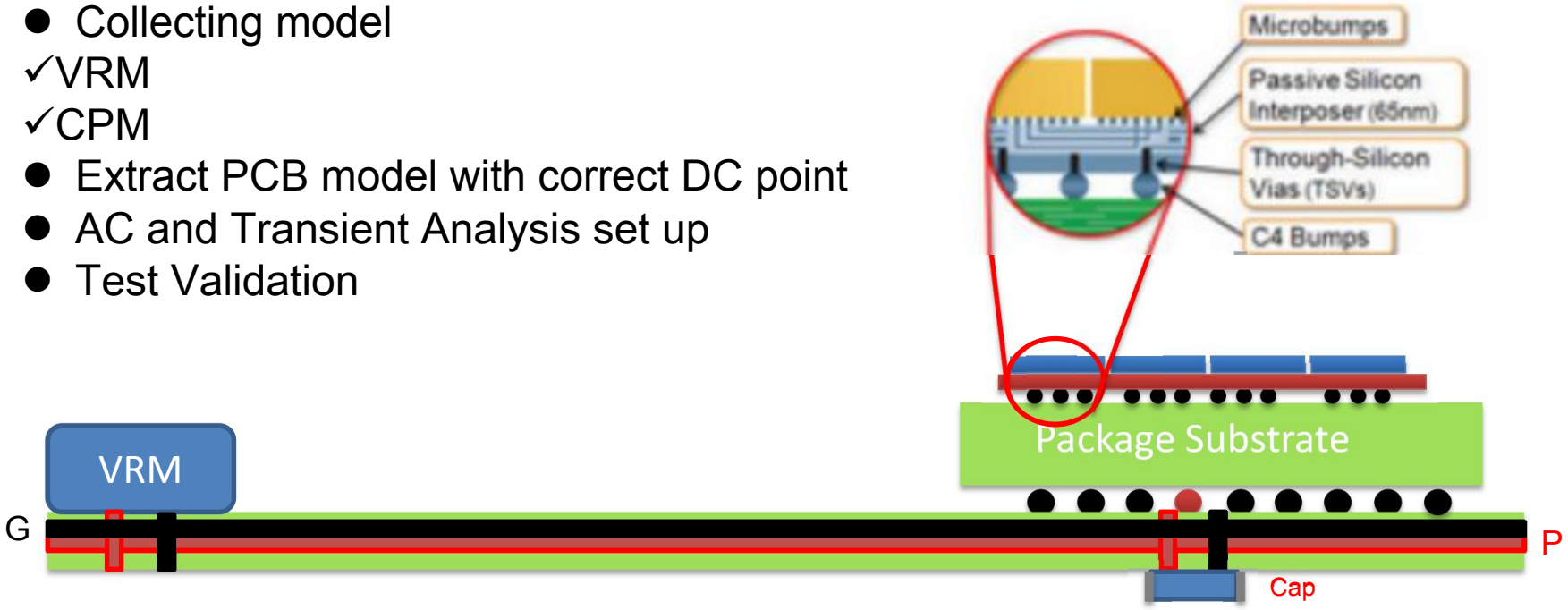
System Integrator Design Flow

- Collecting model

✓VRM

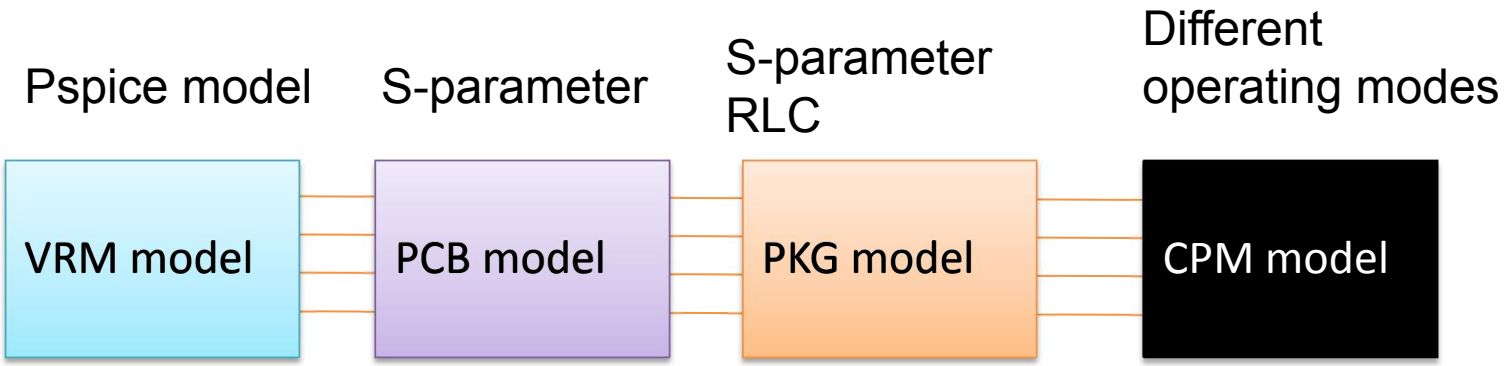
✓CPM

- Extract PCB model with correct DC point
- AC and Transient Analysis set up
- Test Validation



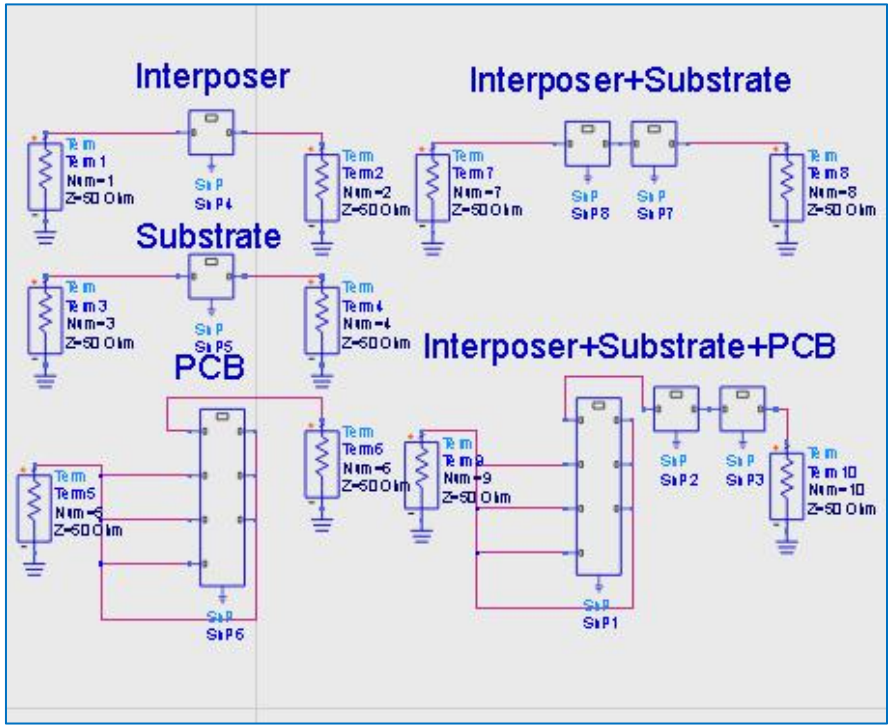
Simulation Setup

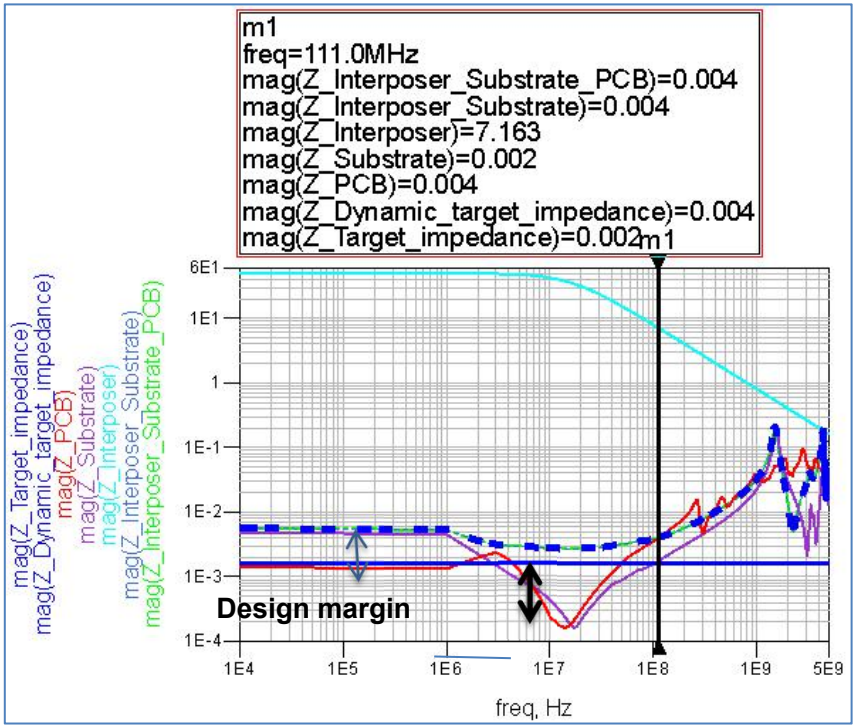
- ✓ VRM Ideal simple RLC Pspice model
- ✓ PCB Broadband SPICE or S-parameter
- ✓ PKG S-parameter or RLC model
- ✓ CPM different operating modes



System Simulation Setup for Core VDD & VDDA

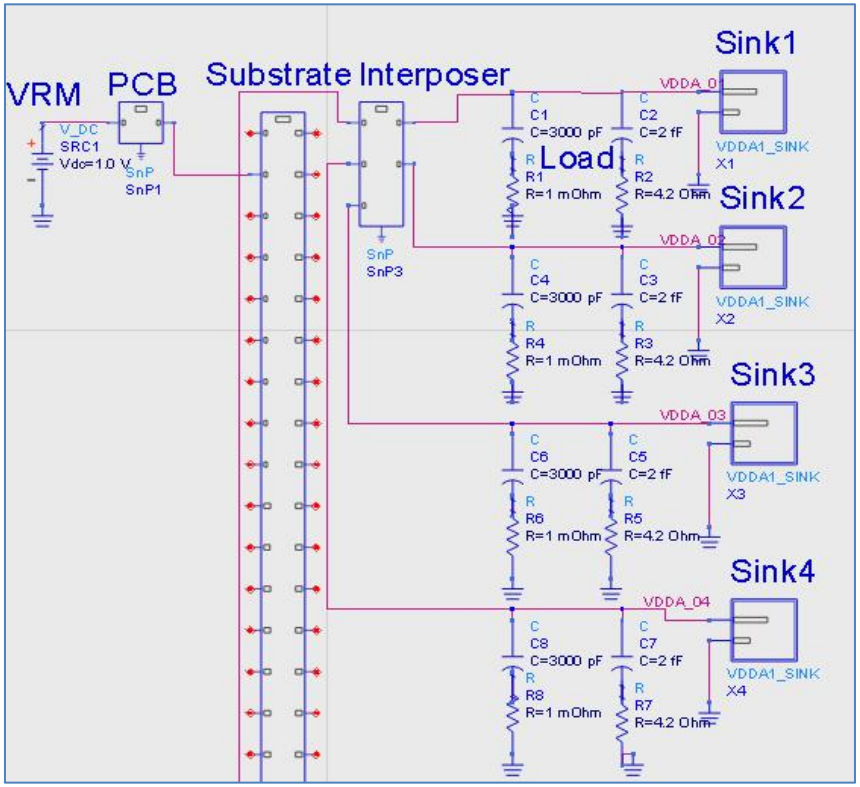
Characteristic Impedance Result



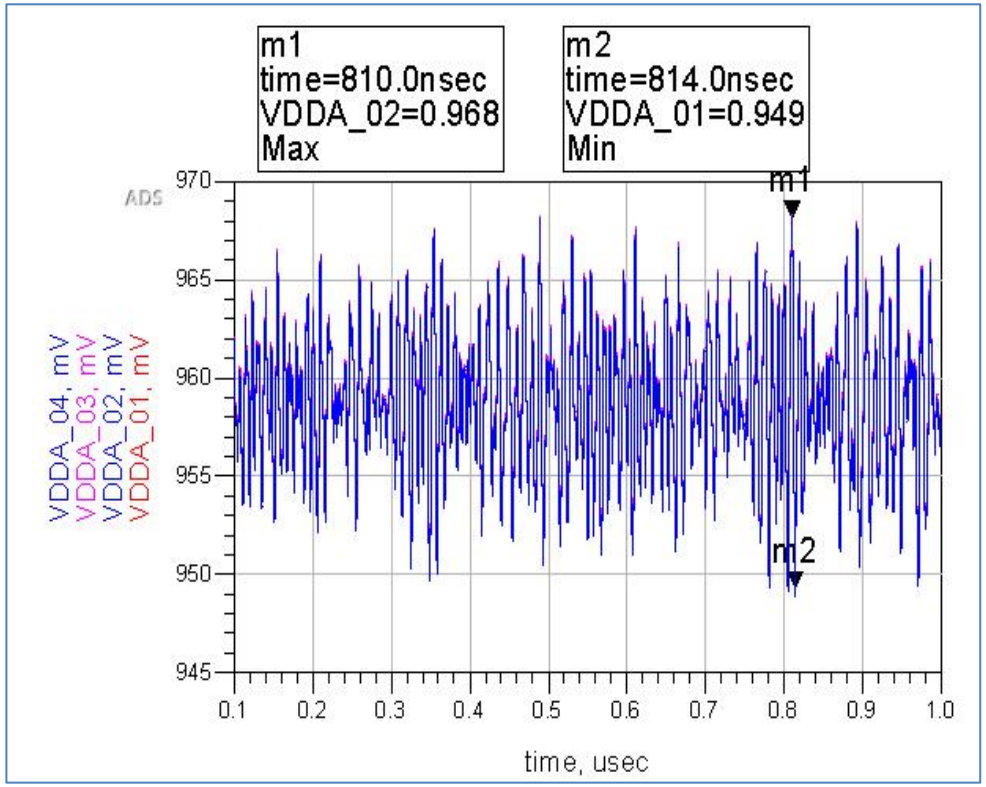


System Simulation Setup for Core power AC impedance

Transient Analysis Result

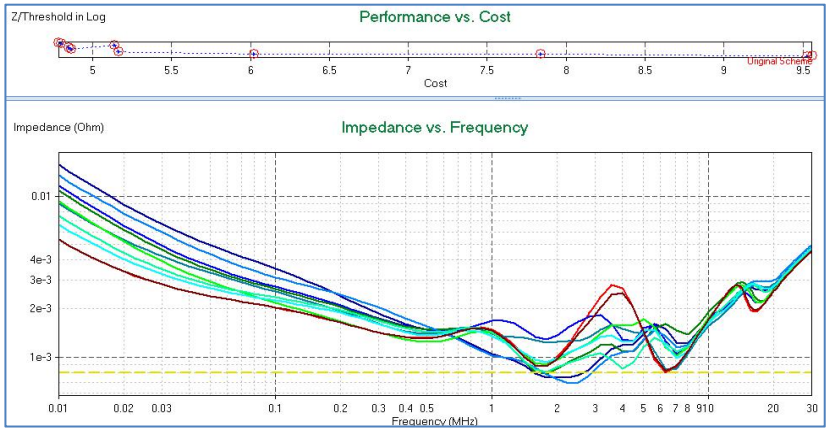


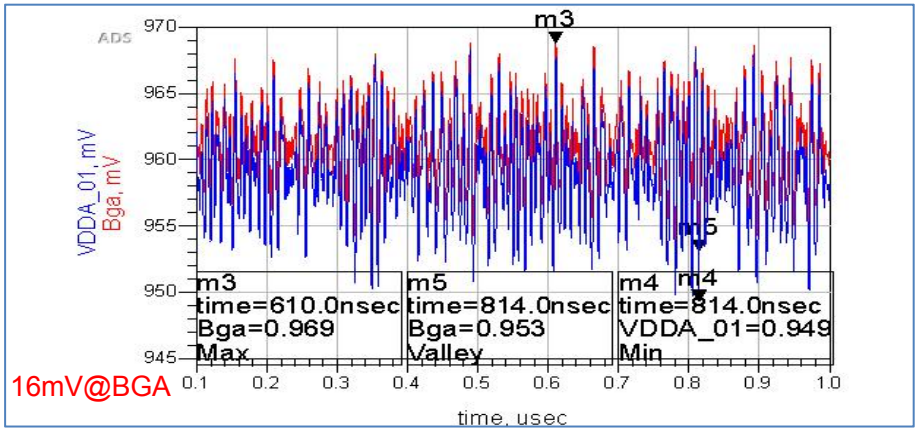
Schematic diagram

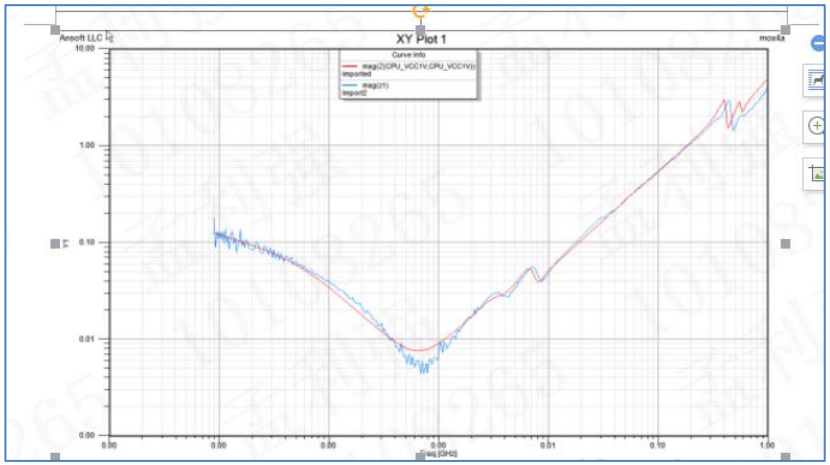


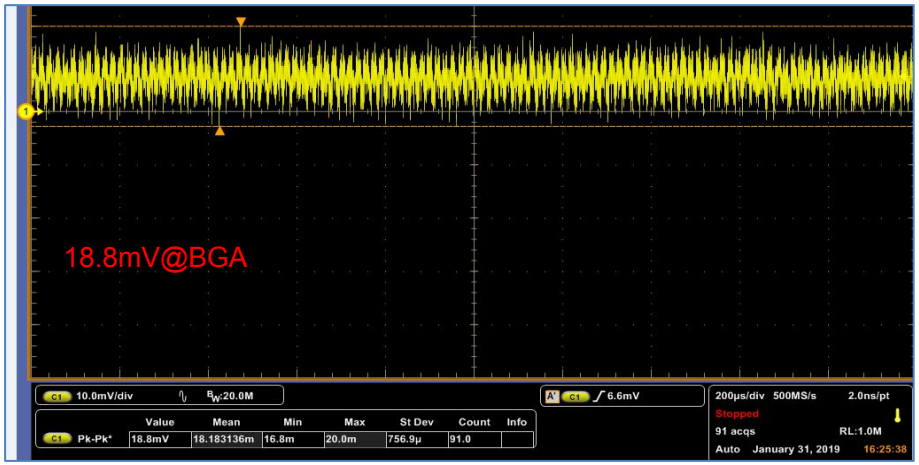
Simulation Result AC nosie 1.9% DC IR Drop 4%

Test VS Simulation









Characteristic Impedance Test vs Simulation

Transient Analysis Test vs Simulation

Summary

- Getting the CPM model is a very difficult but necessary thing to do
- CPM has accurate load current profile and complete package information
- Dynamic target impedance show that PCB have same margin compaire with traditional target impedance
- Test Vs simulation is can improve design confidence for both ac and transient
- Thermal&SI&PI co-simulation is another worth thing to do

Thank you !