EDI CON 2019
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电子设计创新大会
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PCB/高速线缆射频测试技术

RF test on PCB/High Speed cables

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ROHDE&SCHWARZ

内容

- 1 数据传输速率提高的趋势
- 2 频域测试替代时域测试
- 3 差分传输技术及平衡S参数是高速数据传输的主要方式
- 4 去嵌入与校准处理方法
- 5 眼图
- 6 PCB Dk Df测试

高速信号测试的趋势
USB速率进化

USB版本	最大传输速率	速率称号	推出时间
USB1.0	1.5Mbps	低速(Low-Speed)	1996年1月
USB1.1	12Mbps	全速(Full-Speed)	1998年9月
USB2.0	480Mbps	高速(High-Speed)	2000年4月
USB3.0	5Gbps	超高速(Super-Speed)	2008年11月
USB3.1	10Gbps	(Super-Speed+)	2013年12月

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高速信号测试的趋势
PCIe速率进化

版本	发布时间	原始数据传输带宽	有效带宽	单个Lane带宽	总带宽(x32)
PCIe1.x	2003	2.5GT/s	2Gbps	250MB/s	8GB/s
PCIe2.x	2007	5.0GT/s	4Gbps	500MB/s	16GB/s
PCIe3.0	2010	8.0GT/s	8Gbps	1GB/s	32GB/s

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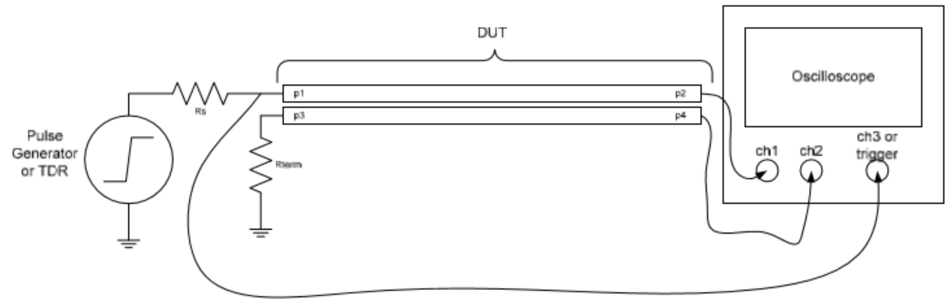
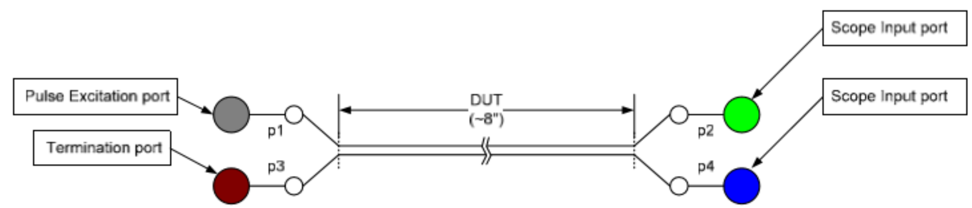
PCB与高速数据线测试的方法

- 示波器或TDR方法
- 特点： 时域方法，
- 比较直观观测时域响应曲线

- 去嵌入?
- 端口矢量校准?
- 速率要求高的时候，需要发射上升沿特别小的阶跃信号?
- 抗静电





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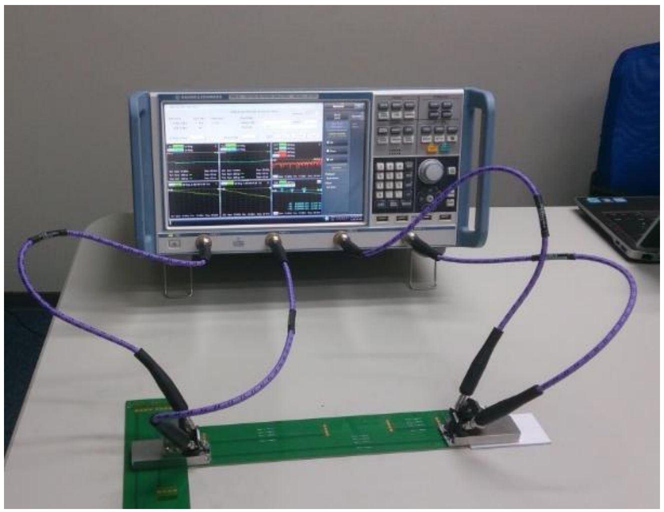
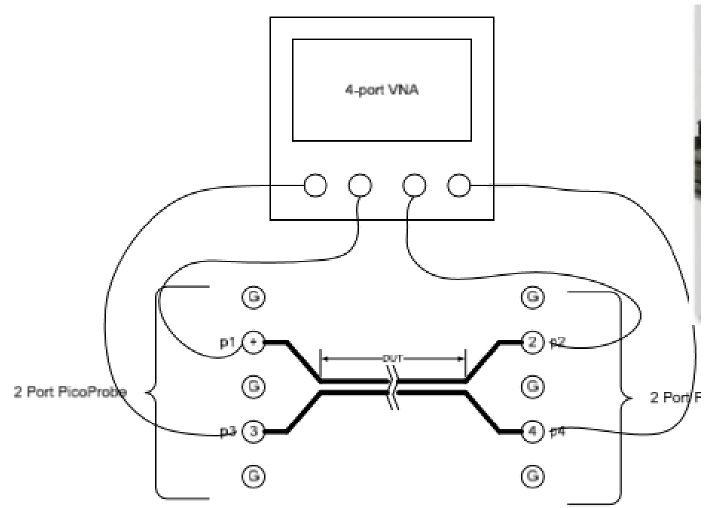
频域测试-矢量网络分析仪





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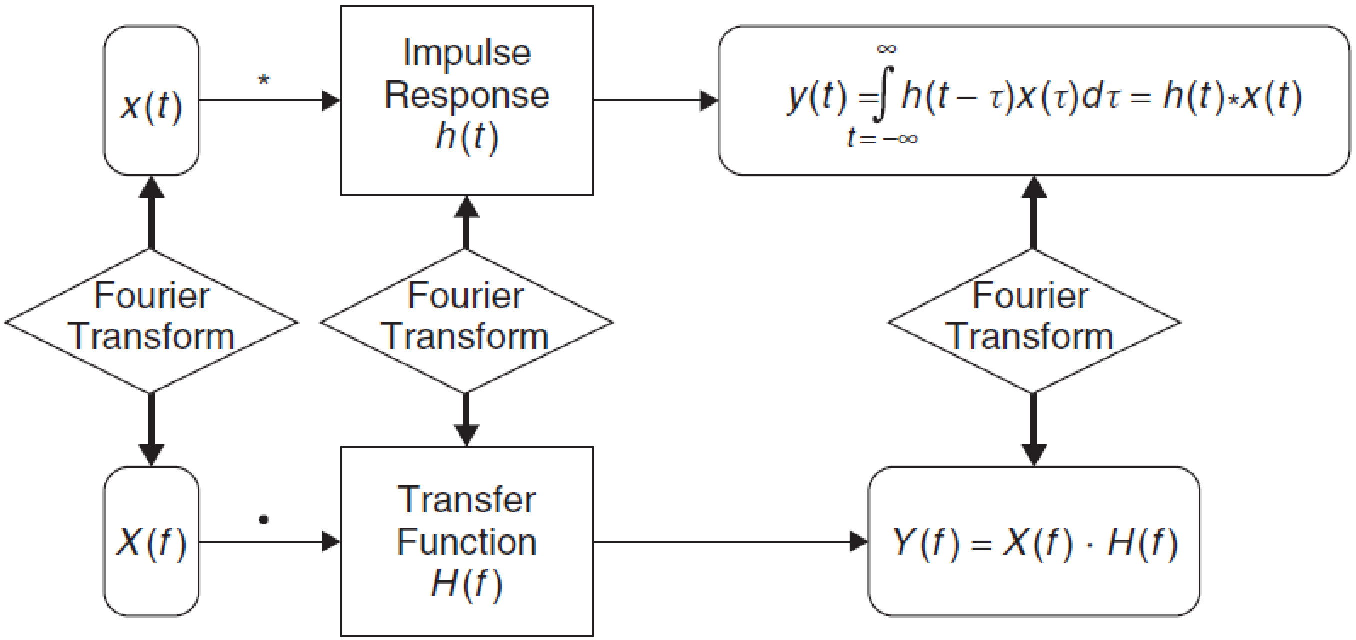
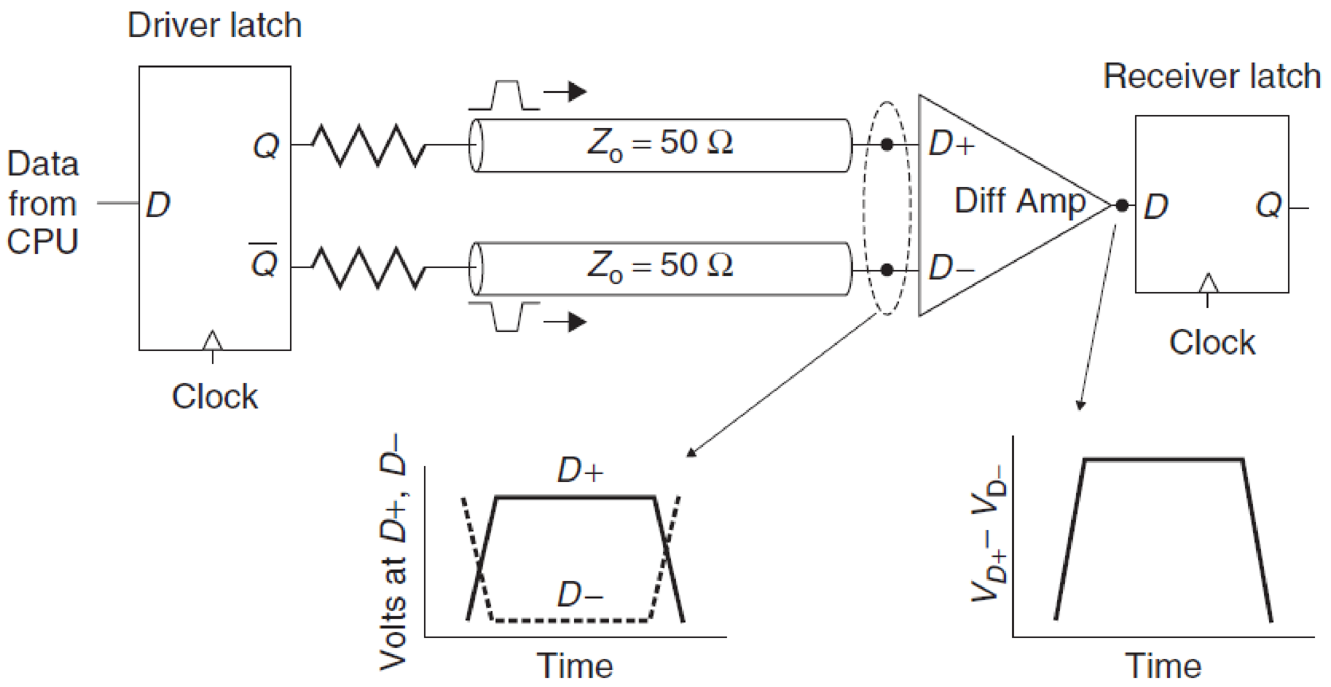
时域与频域的关系



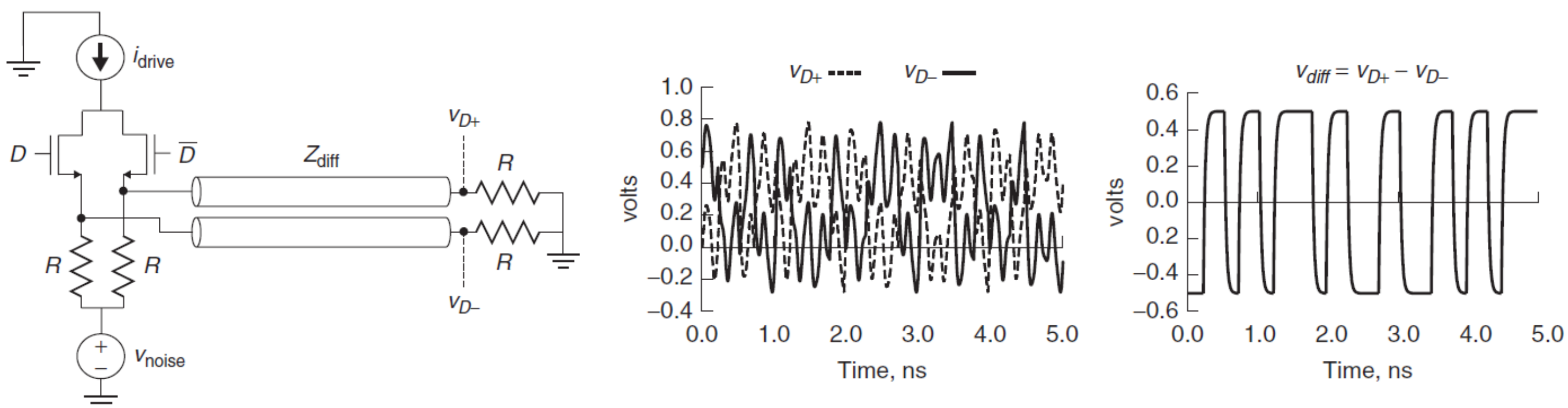
x(t)
*
Impulse Response h(t)
y(t) = ∫ h(t − τ)x(τ)dτ = h(t)*x(t)
t = −∞
∞
Fourier Transform
Fourier Transform
Fourier Transform
X(f)
•
Transfer Function H(f)
Y(f) = X(f) · H(f)

差分传输



Driver latch
Data from CPU
D
Q
$\overline{Q}$
Clock
$Z_o = 50\ \Omega$
$Z_o = 50\ \Omega$
D+
D−
Diff Amp
Receiver latch
D
Q
Clock
Volts at D+, D−
D+
D−
Time
$V_{D+} - V_{D-}$
Time

差分传输



$$v_{\text{diff}} = (v_{D+} + v_{\text{noise}}) - (v_{D-} + v_{\text{noise}}) = v_{D+} - v_{D-}$$

差分（或奇模）信号，导带之间存在一个理想虚拟参考平面。当收到共模干扰或噪声时，虚拟的参考平面 保持连续，从而保证信号完整性（SI）

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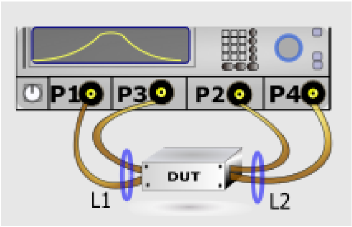
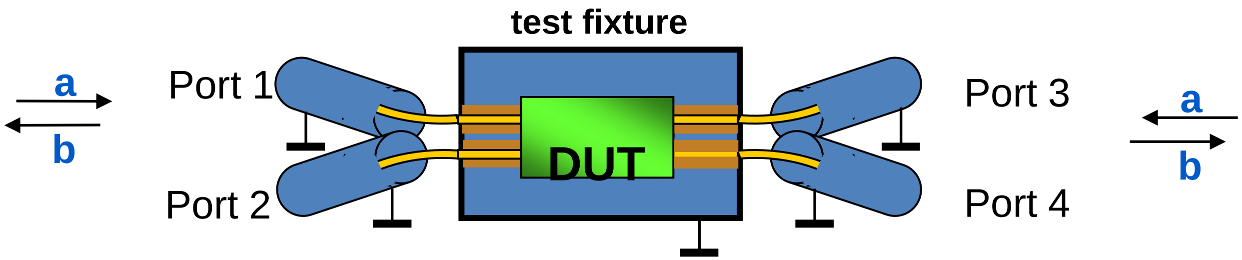
差分测试





$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} * \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

差分测试结果：混合S参数

Logical Port 1　　Logical Port 2

$$
\begin{array}{cc|cc|cc}
 & & \text{Differential-Mode Stimulus} & & \text{Common-Mode Stimulus} & \\
 & & \text{Port 1} & \text{Port 2} & \text{Port 1} & \text{Port 2} \\
\hline
\text{Differential-Mode Response} & \text{Port 1} & S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\
 & \text{Port 2} & S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\
\hline
\text{Common-Mode Response} & \text{Port 1} & S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\
 & \text{Port 2} & S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22}
\end{array}
$$

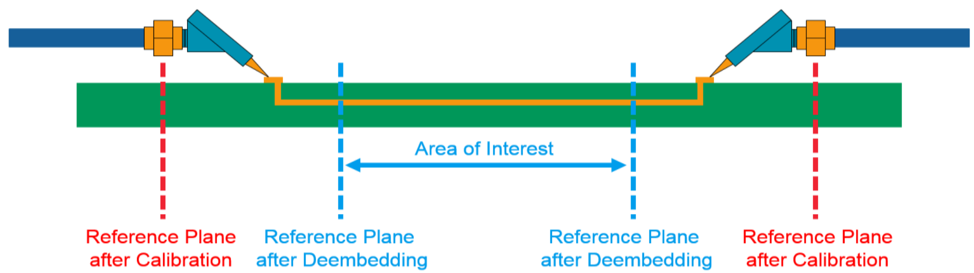
S_{ABxy}　A: mode response
B: mode stimulus
x: response port
y: stimulus port

校准与去嵌入

同轴端面：
TOSM Calkit

探针断面：
TRL（PCB）

探针+过孔+过渡：
去嵌入 De-embedding



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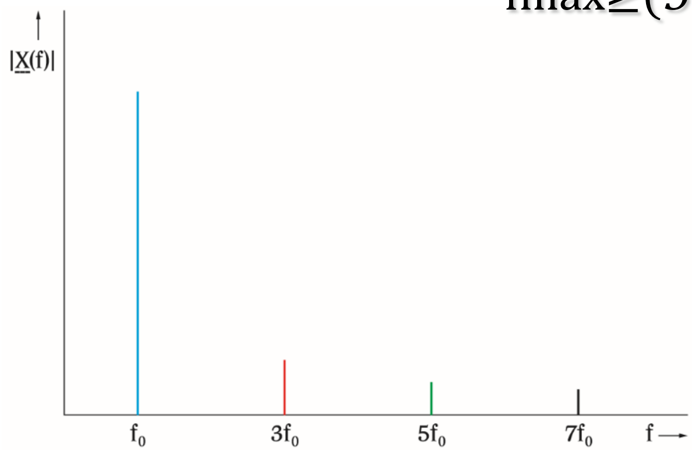
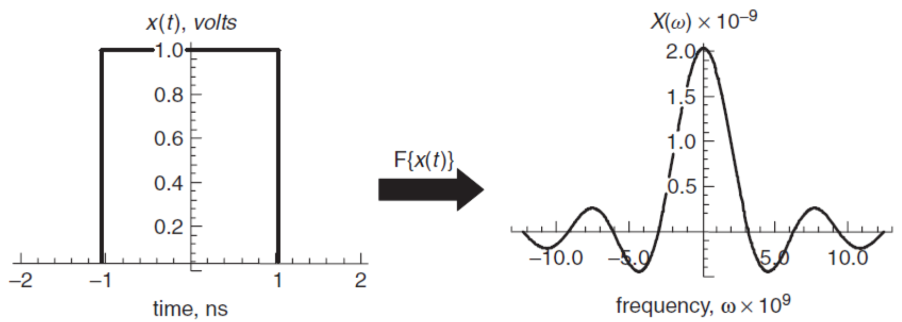
矢量网络分析仪测试

VNA 测试频率要求与码速率的关系

$$f_{max} \geq (3\sim5)/2 * Bitrate$$





因果系统

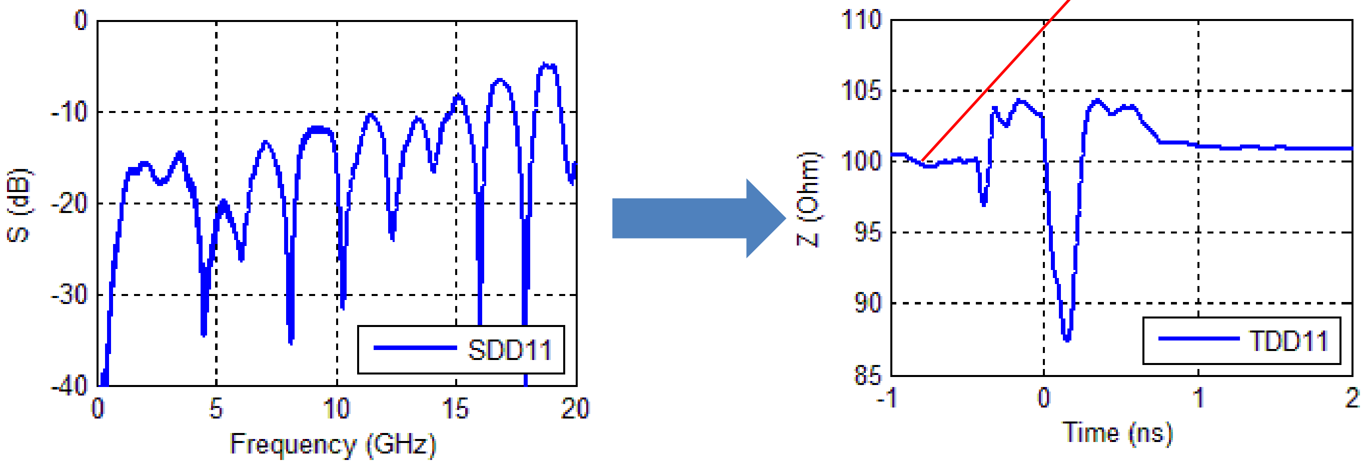
- 因果系统是指当且仅当输入信号激励系统时，才会出现输出（响应）的系统。即因果系统的（响应）不会出现在输入信号激励系统的以前时刻；也就是说系统的输出仅与当前与过去的输入有关，而与将来的输入无关的系统。

- Can not get something from nothing.

非因果S参数

在零时刻之前有
响应，非因果性

把S参数数据转换为TDR/TDT



产生非因果S参数的原因

- 测量误差(de-embedding)
-
- 仿真误差(材料的特性)

- 有限的带宽

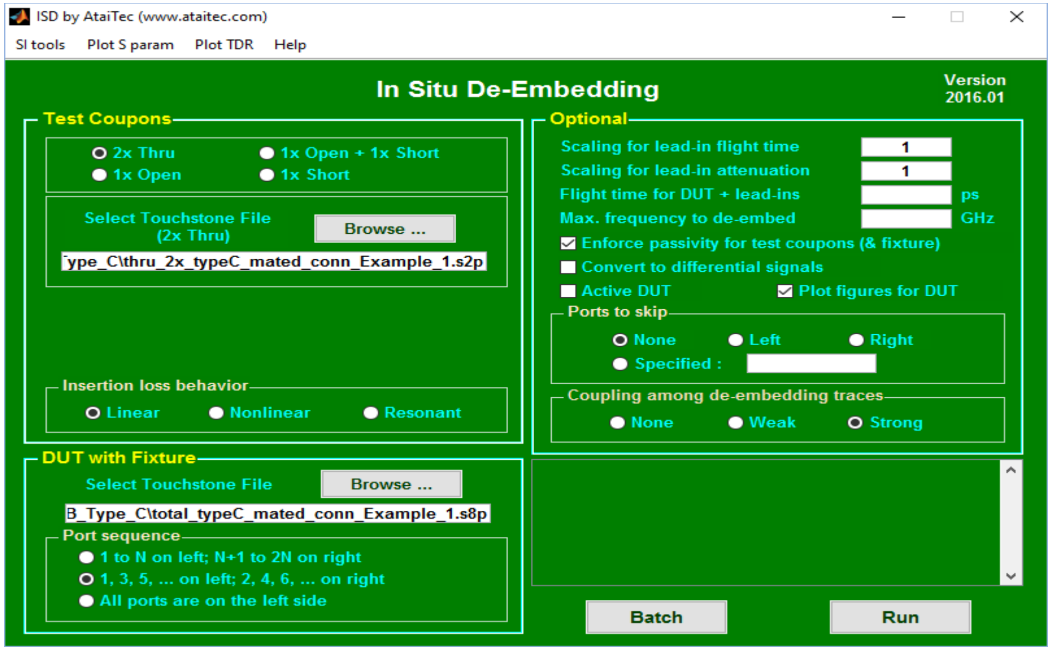
- In-Situ De-embedding (ISD)会给出因果关系的去嵌入结果，根据有限带宽的S参数，给出具有因果相应的系统函数。

板子间的接头去嵌入

- TRL 对这种板级间链接器的去嵌入很复杂，不使用。ISD可以很高精度的提取参数

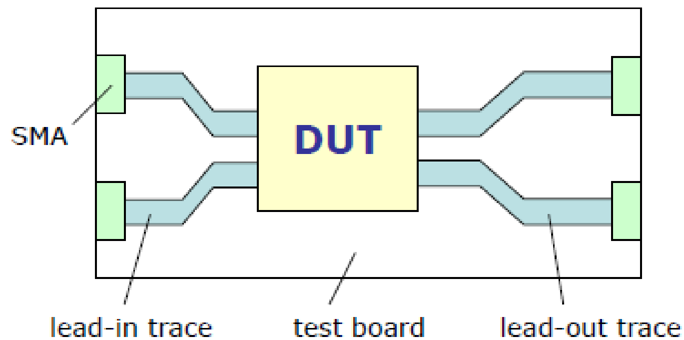
Ataitek ISD 去嵌入方法

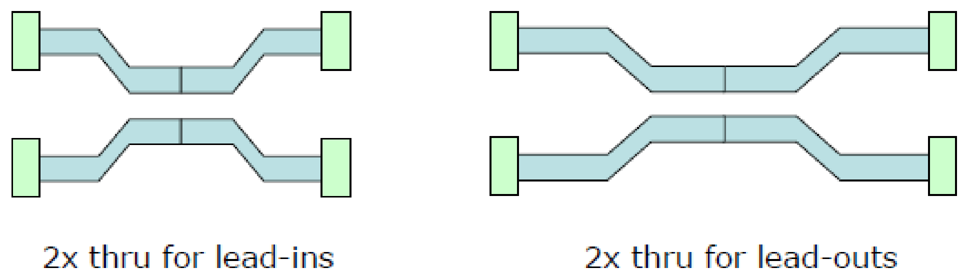
- 通过 “2x thru” 或者 “1x open / 1x short” 作为参考，通过去嵌入和优化算法，得到夹具的真实响应。



什么是“2x thru” 去嵌入

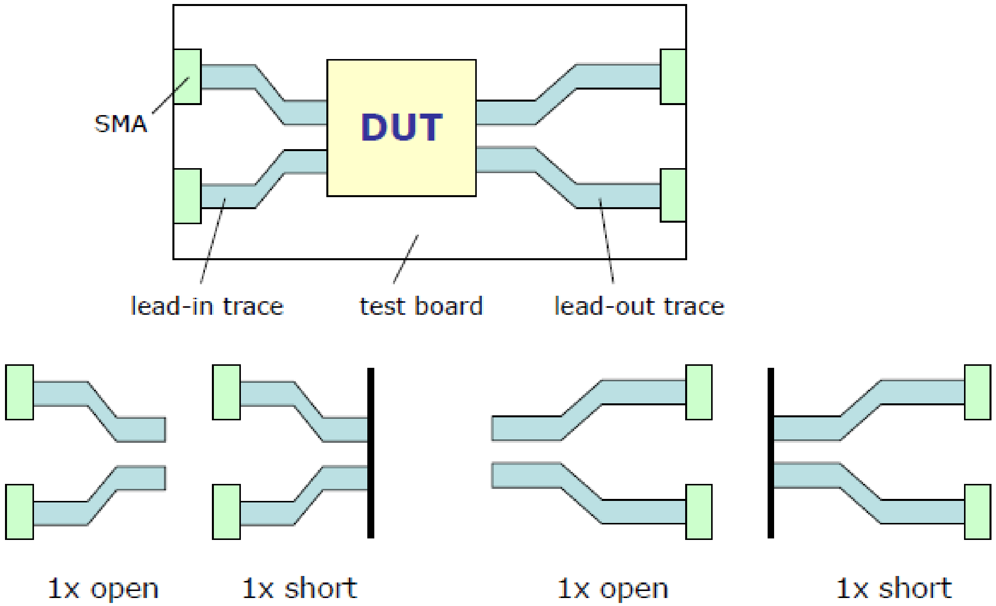
- “2x thru” 是





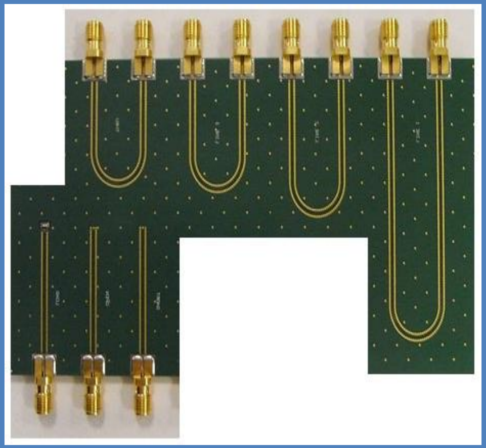
“1x open / 1x short” 去嵌入

- “2x thru”不易实现的时候（例如 接头， 通孔)， “1x open / 1x short”可以作为参考计算依据。



Ataitek ISD去嵌入方法与传统TRL校准

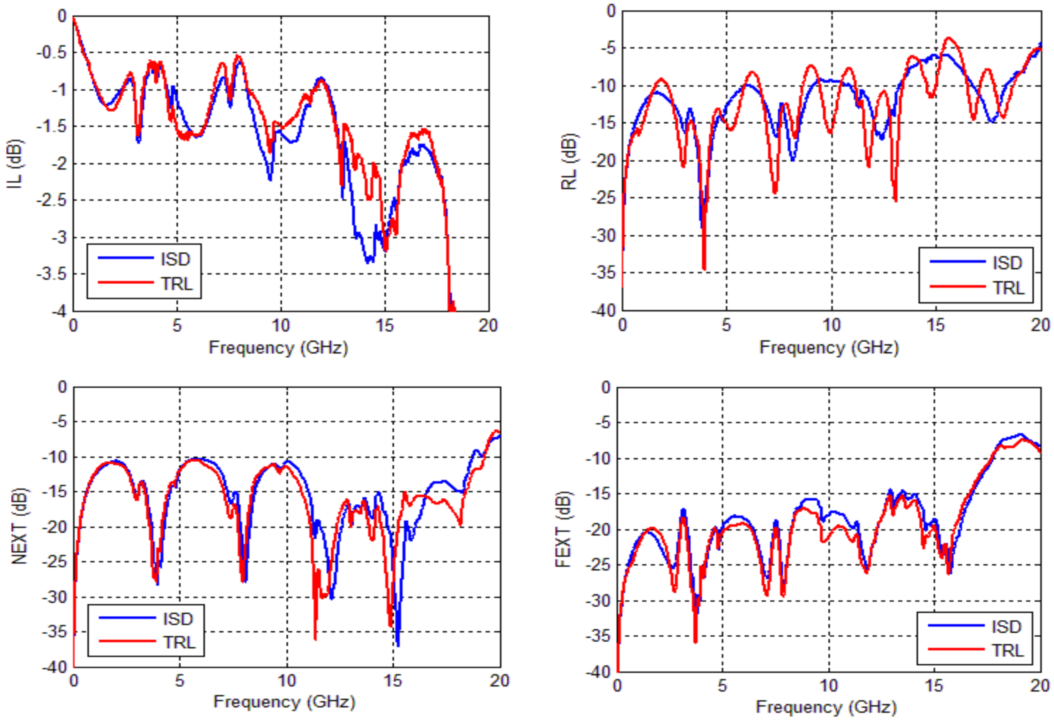
TRL 校准板



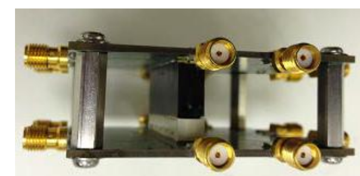
ISD 去嵌入板

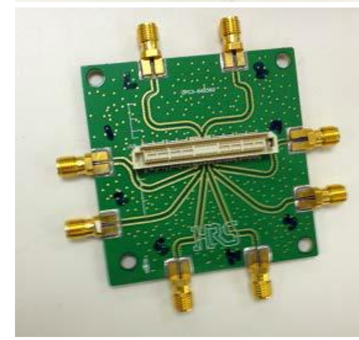
1.2x thru 长度的线
2.板子面积，材质，接头数量少
3. 精度高

高速连接器去嵌入 *ISD vs. TRL*

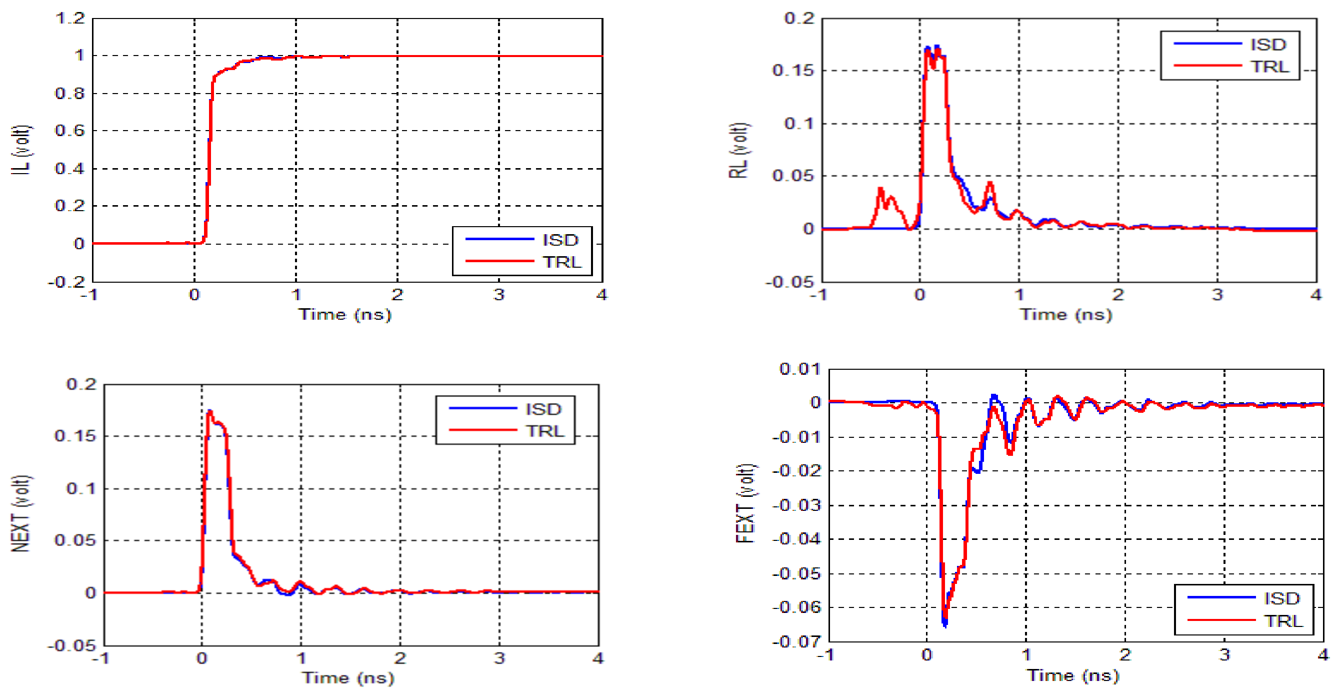


对于这种小的DUT,TRL校准后测试结果会有些波动和毛刺





高速连接器去嵌入 *ISD vs. TRL*



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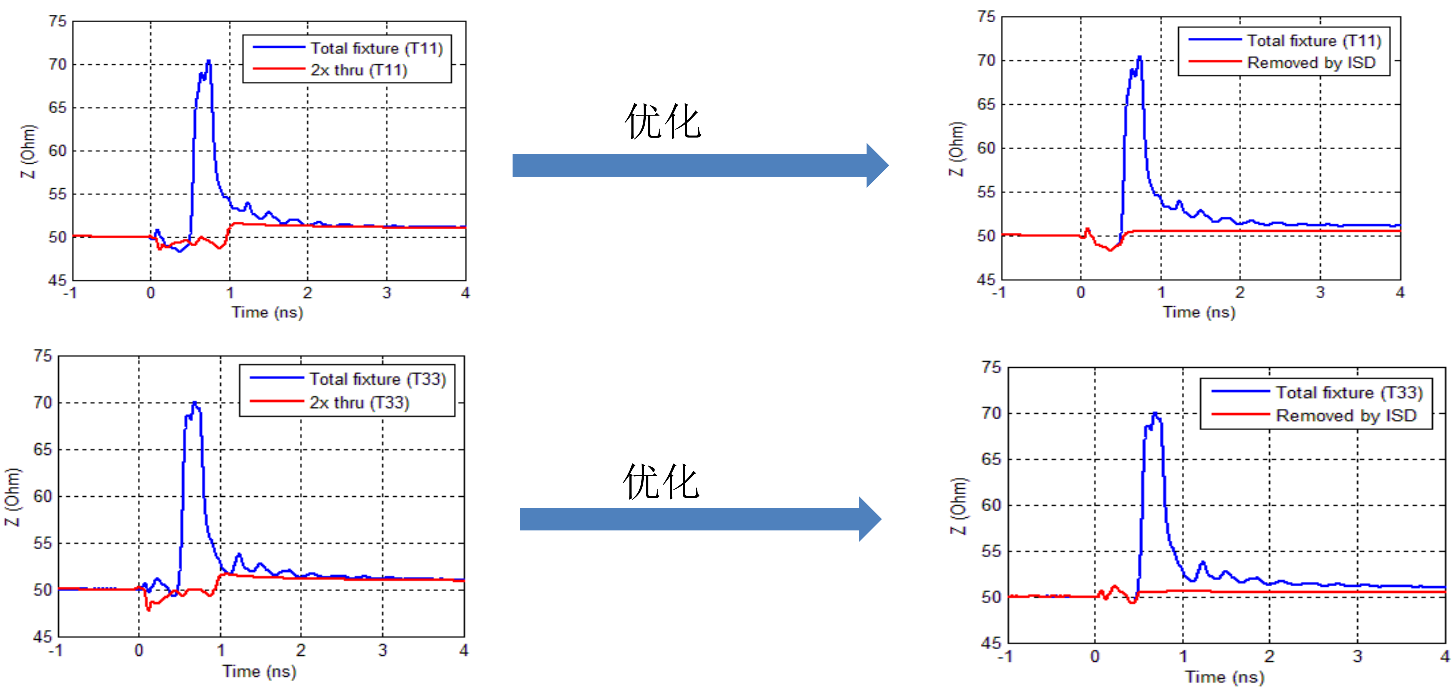
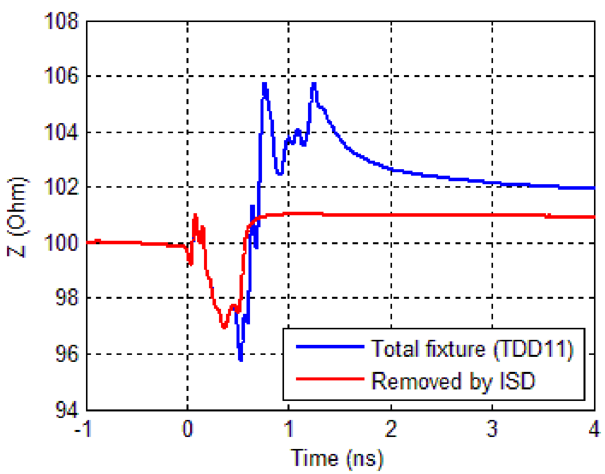
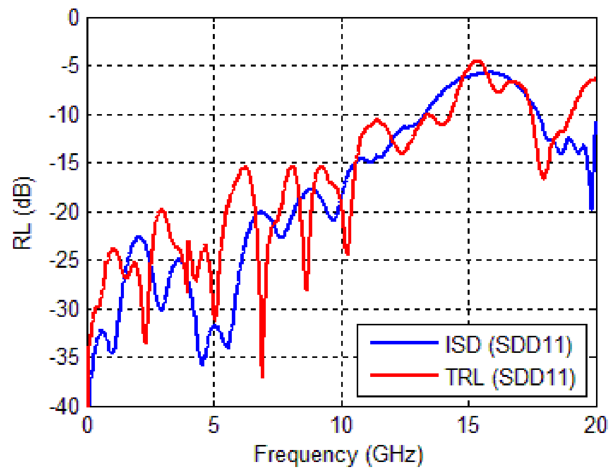
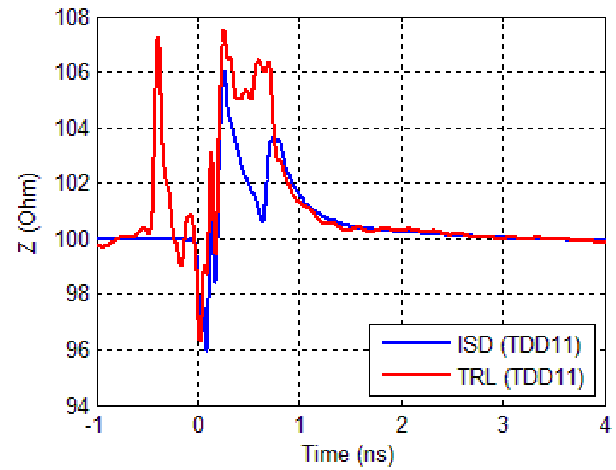
ISD怎么做到去嵌入优化的



差分测试：TRL的误差项目更大

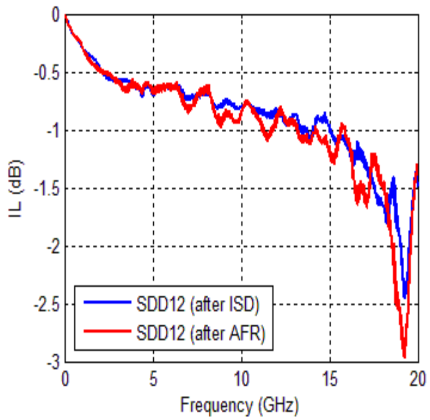


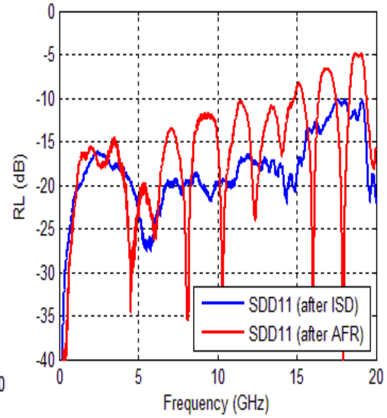


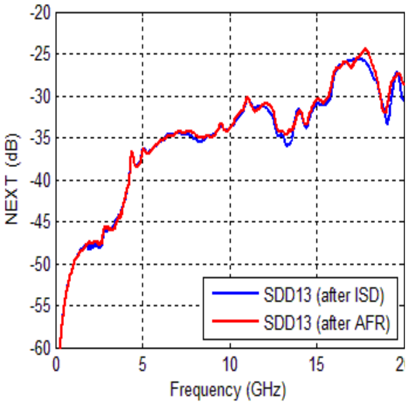


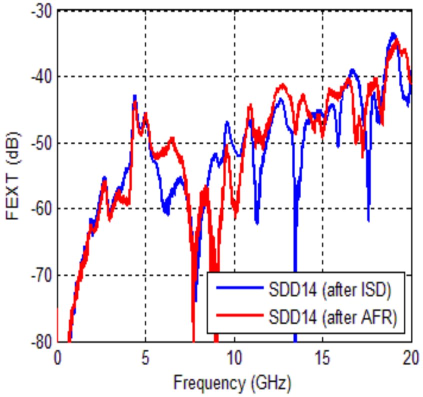
USB type C 连接器测试 *ISD vs. AFR*

- 在反射测试中，AFR有很多震荡









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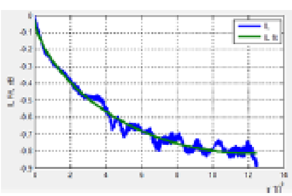
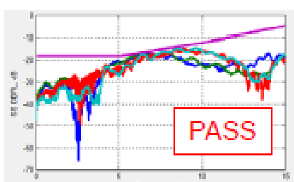
对IMR和IRL有优势

ISD

	Value (Pass/Fail)
ILfit@2.5GHz	-0.4
ILfit@5.0 GHz	-0.6
ILfit@10.0GHz	-0.8
IMR	-45.1
IRL	-23.2
INEXT	-41.5
IFEXT	-49.2
SCD12/SCD21	-23



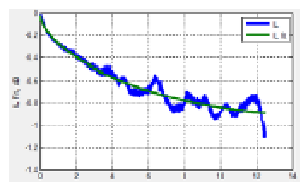
IL



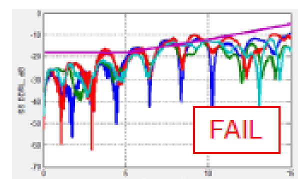
RL

AFR

	Value (Pass/Fail)	Spec
ILfit@2.5GHz	-0.4	-0.6
ILfit@5.0 GHz	-0.6	-0.8
ILfit@10.0GHz	-0.9	-1.0
IMR	-43.7	-40
IRL	-20.8	-18
INEXT	-41.5	-44
IFEXT	-49.3	-44
SCD12/SCD21	-23.2	



IL



RL

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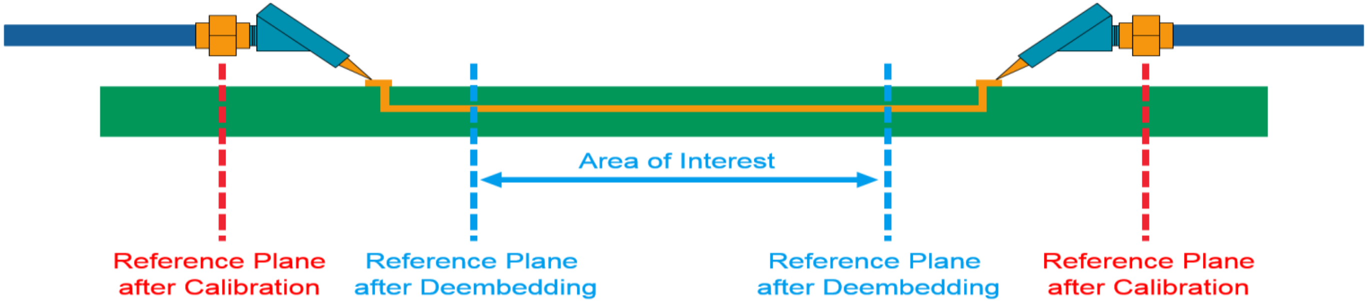
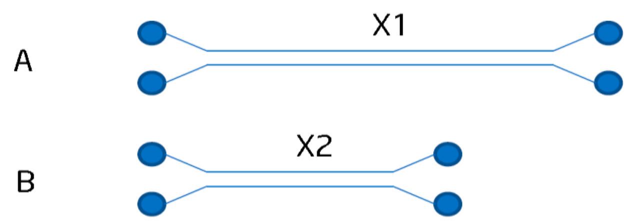
SFD Delta L和Eigenvalue Delta L

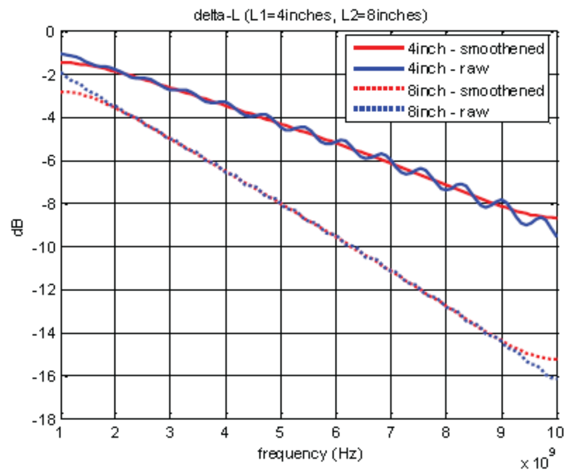


Delta L 测试原理

Eigenvalue Delta L是一种针对PCB，线缆，连接器等的插损测试技术

- A的插损　　A: IL(A) --- {X1 inch + vias}
- B的插损　　B: IL(B) --- {X2 inch + vias}
- dB/inch loss=[IL(A)-IL(B)] / (X1-X2)





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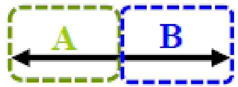
Eigenvalue Delta L 测试原理

- 通过 T 矩阵解方程
- 2X Thru, L1: 

- 2X Thru+DUT, L2: 

$$T_{L1}=T_A \times T_B$$

$$T_{L2}=T_A \times T_{\mathrm{DUT}} \times T_B$$

$$T_{L2} \times T_{L1}^{-1}=T_A \times T_{\mathrm{DUT}} \times T_B \times T_B^{-1} \times T_A^{-1}$$

$$\boxed{T_{L2} \times T_{L1}^{-1}} = T_A \times \boxed{T_{\mathrm{DUT}}} \times T_A^{-1}$$

$$B = P^{-1} \times A \times P$$

Matrix similarity: matrix A and B have the same eigenvalues

Eigenvalue Delta L 测试原理

- 根据矩阵的相似性，
-

$T_{L2} \times T_{L1}^{-1}$ T_{DUT}

$$T_{DUT}=\begin{bmatrix} e^{\gamma(L_2-L_1)} & 0 \\ 0 & e^{-\gamma(L_2-L_1)} \end{bmatrix}$$

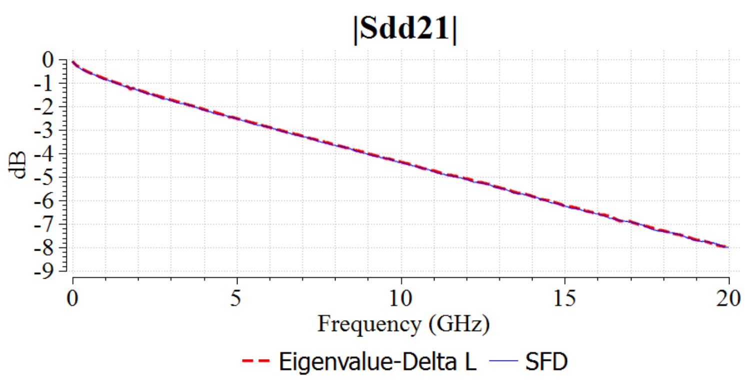
Eigenvalues of T_{DUT}: $e^{-\gamma(L_2-L_1)}$ and $e^{+\gamma(L_2-L_1)}$ $\gamma = \alpha + j\beta$

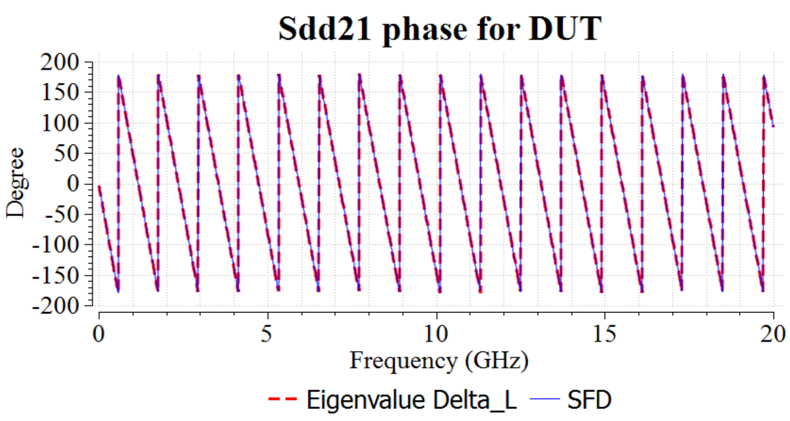
$$\begin{cases} S21_{DUT} = e^{-\gamma(L_2-L_1)} \\ |S21_{DUT}| = e^{-\alpha(L_2-L_1)} = |e^{-\gamma(L_2-L_1)}| \\ loss\ per\ inch = |S21_{DUT}|/\Delta\mathrm{length} \end{cases}$$

normalized to the trace characteristic impedance

不同方法结果的比较-插损

- 用同样的S参数，从Eigenvalue-Delta L Delta L 和 SFD得到近似的结果，一致性比较好





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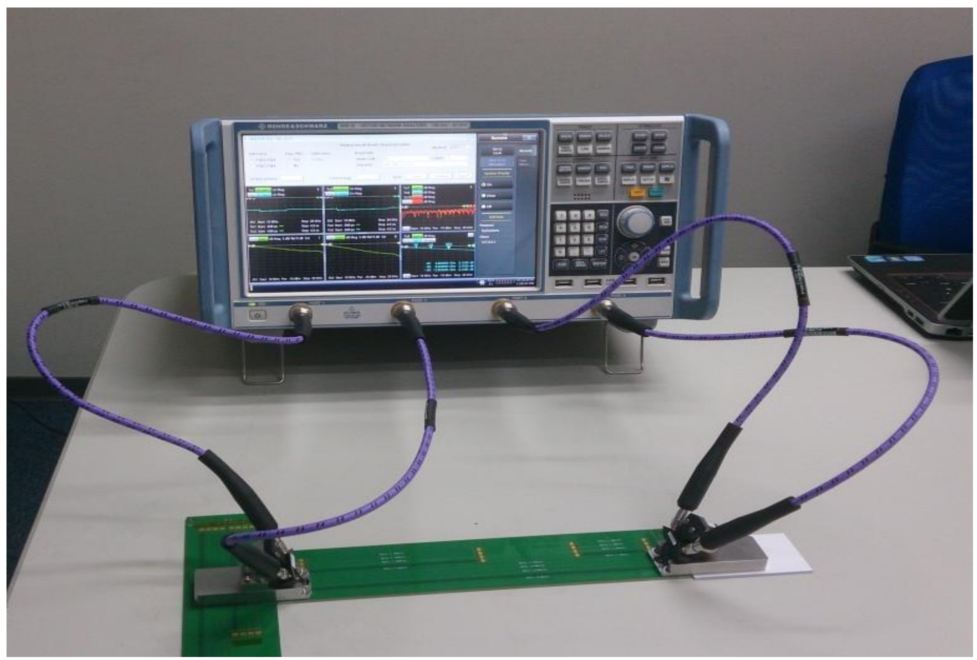
ZNB集成不同算法测试环境

- 下图为R&S公司的矢量网络分析仪ZNB集成不同算法的测试平台搭建，简单，易操作



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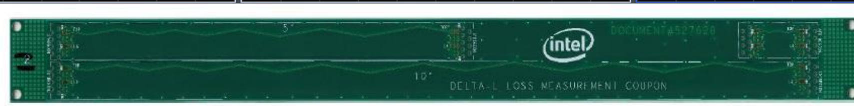
ZNB集成不同算法测试环境

- 此图为用SFD测试的结果



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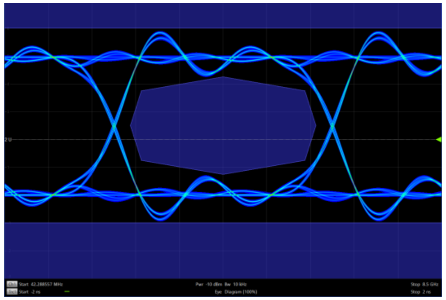
时域分析功能-眼图

- 眼图的由来

Measured frequency domain data → Inverse DFT → Calculated time domain data → Convolution Bit sequence → Calculated eye diagram



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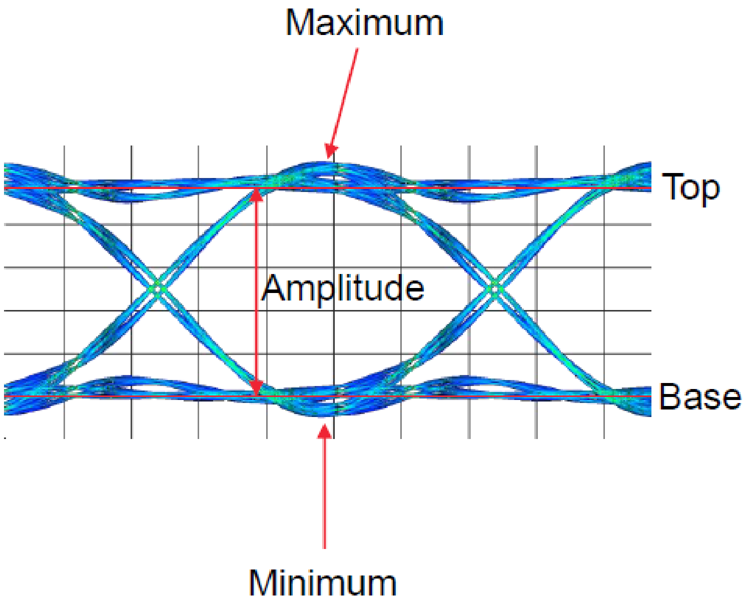
时域分析功能-眼图

Eye Minimum	Minimum outputs of eye diagram processing
Eye Maximum	Maximum outputs of eye diagram processing
Eye Base	Average values for logical zero of eye processing
Eye Top	Average values for logical one of eye processing
Eye Mean	(Eye Top + Eye Base)/2
Eye Amplitude	Eye Top minus Eye Base
Eye Height	Measures effects of noise in reducing the vertical eye opening
Eye Width	Includes the effects of jitter in reducing the horizontal eye opening (i.e. the set Bit Period)



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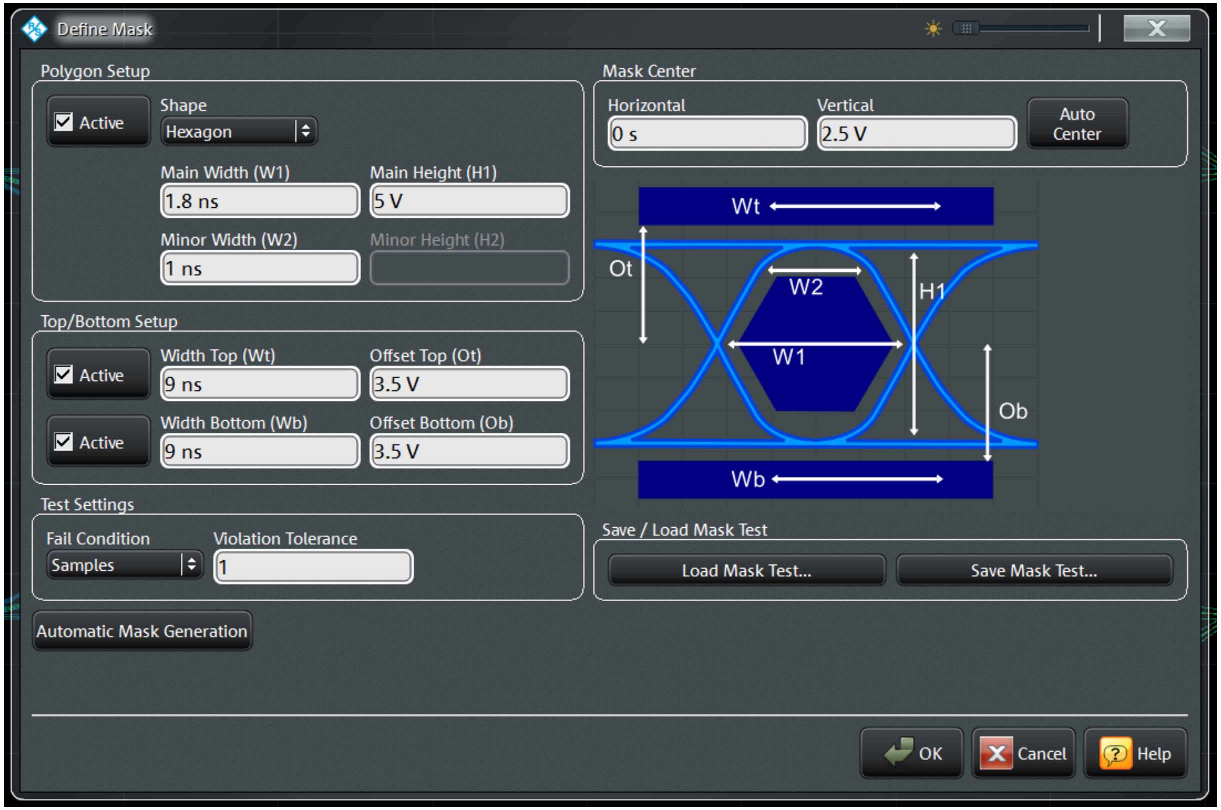
时域分析功能-眼图

眼图设置



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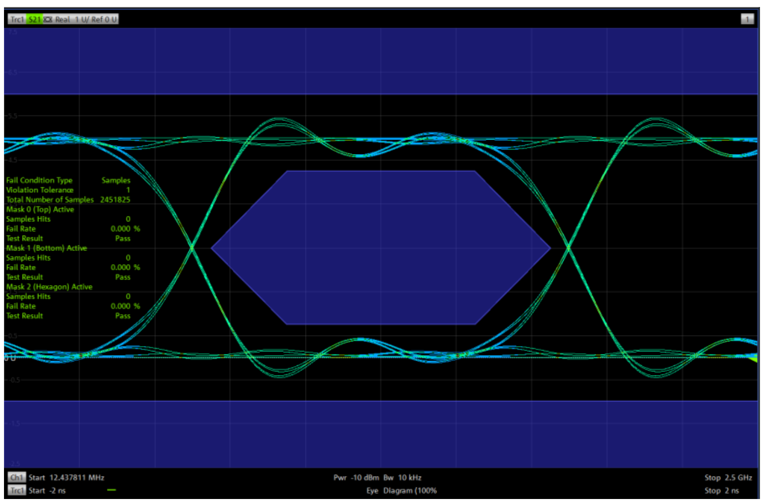
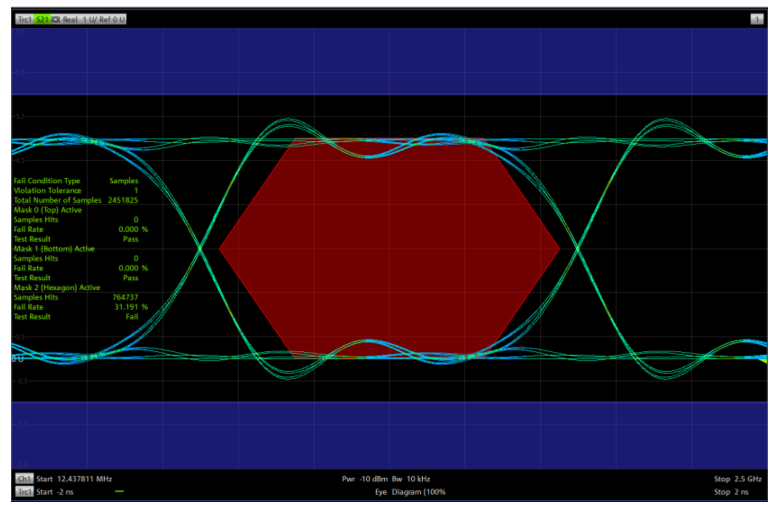
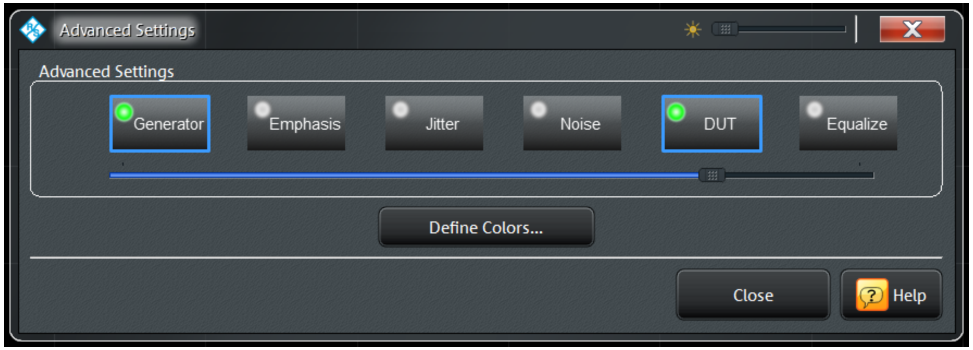
时域分析功能-眼图

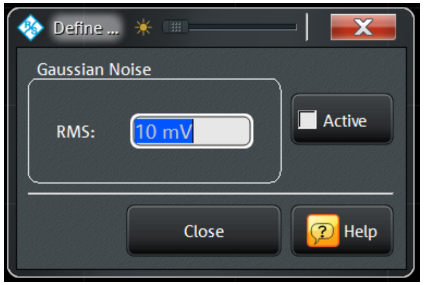
- 定义眼图模板

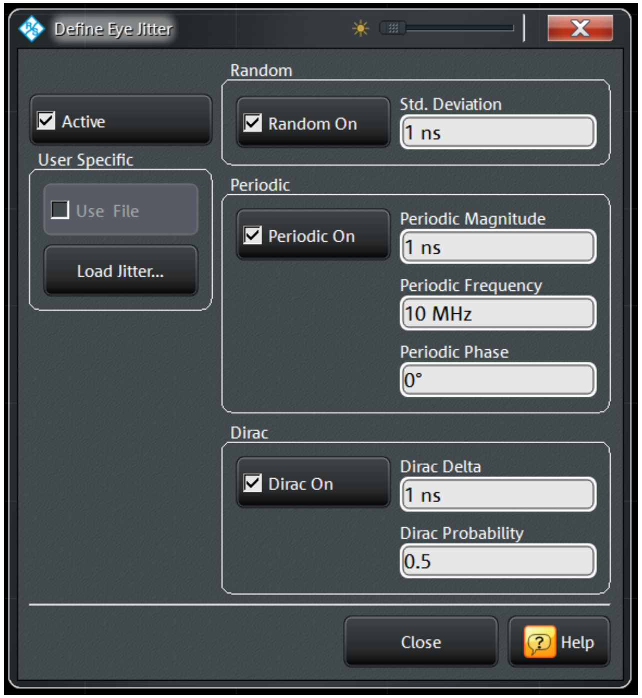




眼图高级设置

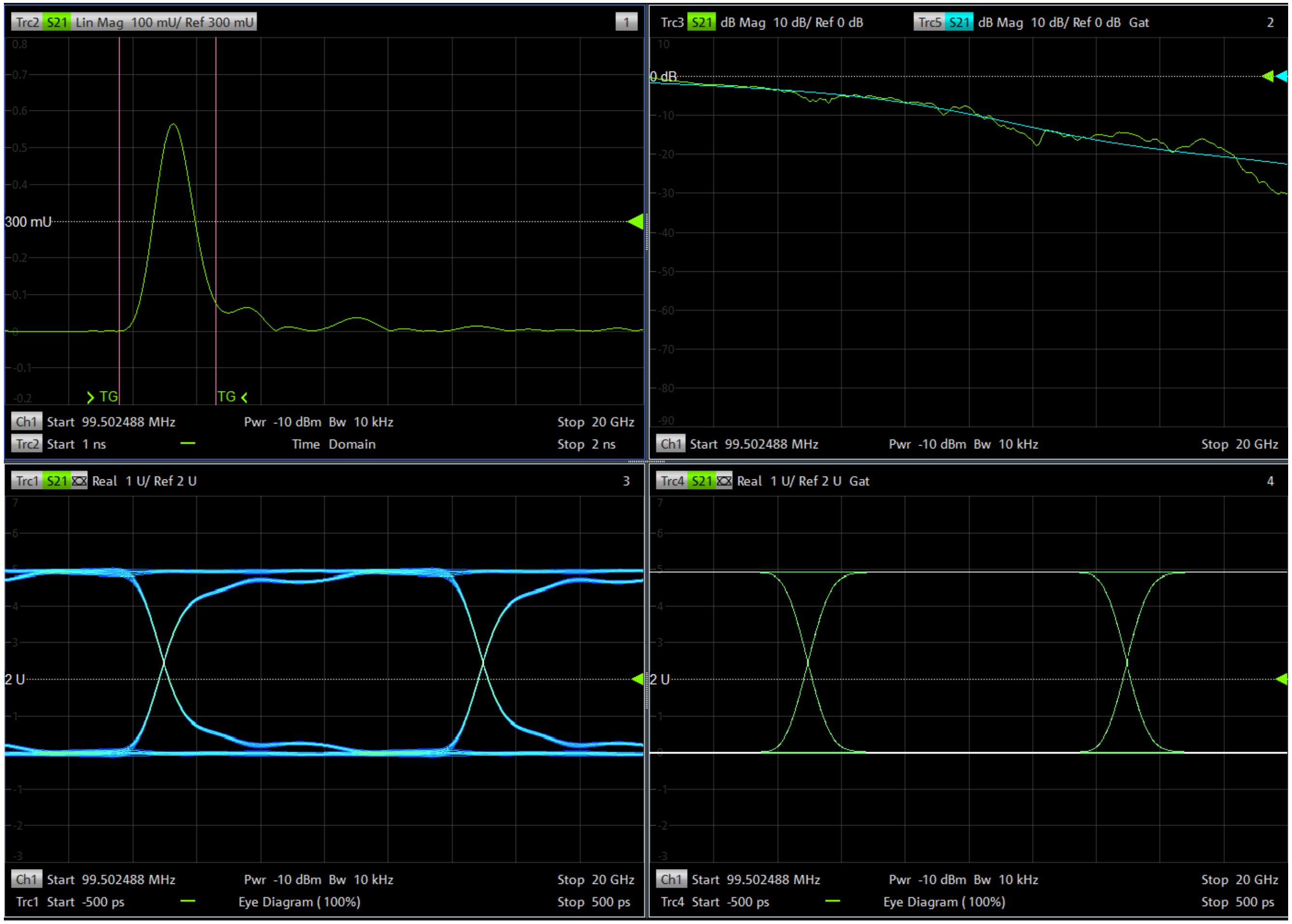






均衡 加重 加噪声 抖动

眼图-时域加门选通



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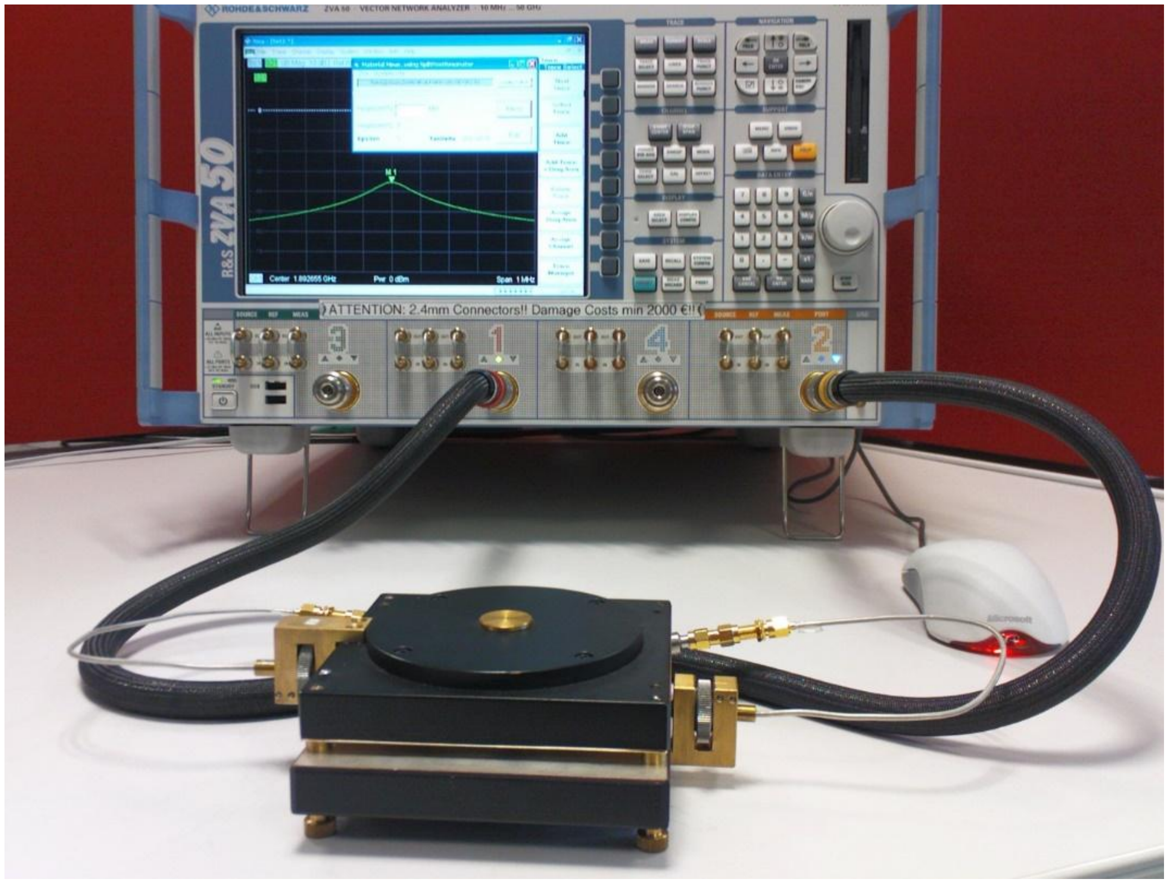
PCB Dk Df测试



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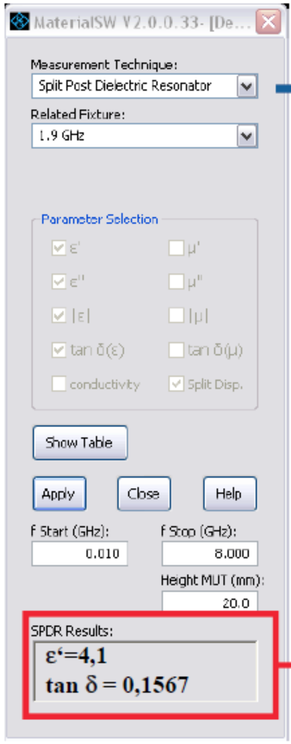
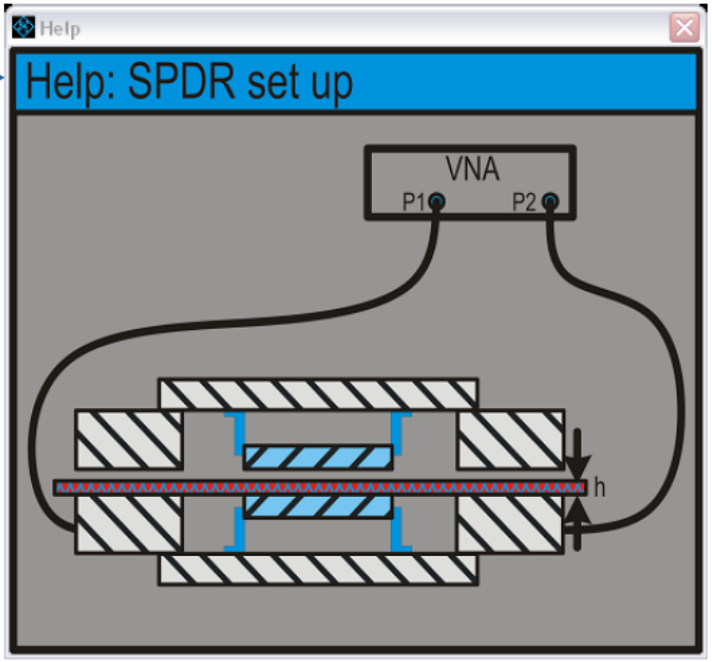
PCB Dk Df测试



- The help is related to the used method



- Results are directly shown

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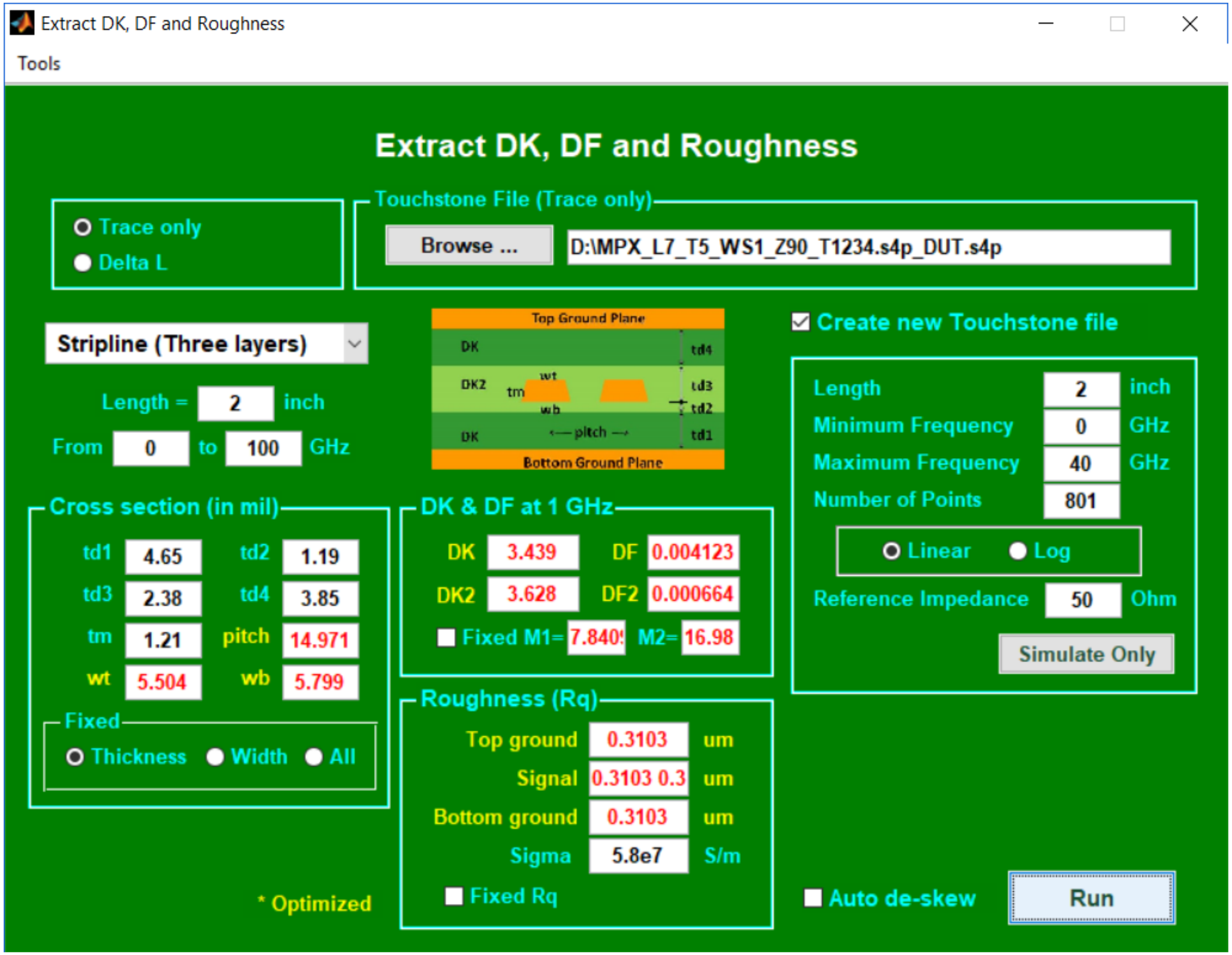
PCB Dk Df 参数提取



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- Thanks for your time！
- Questions？

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