



AMCAD Engineering

Advanced Modeling for Computer-Aided Design

GaN HEMTS Device Modeling Using ASM Standard-Extraction Flow and Validation

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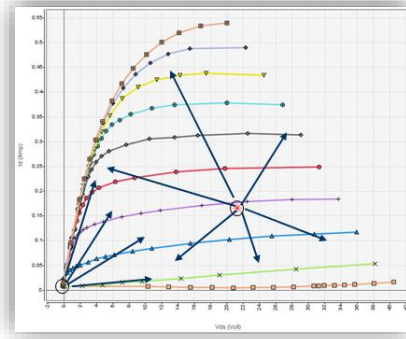
Helping our customers to design smart and safe communication systems !

- **Hardware Requirements**
- **Model Extraction flow**
 - Small Signal FET modeling
 - Output Current Source
 - Diodes
 - Non-linear capacitances
 - Thermal & trapping effects
- **Large Signal Model Validation**

Hardware Requirements

Measurement System

- Short pulse : Quasi-isothermal conditions
- Low duty cycle : Constant mean temperature
- Quiescent bias point :
Thermal conditions fixed
Traps conditions fixed

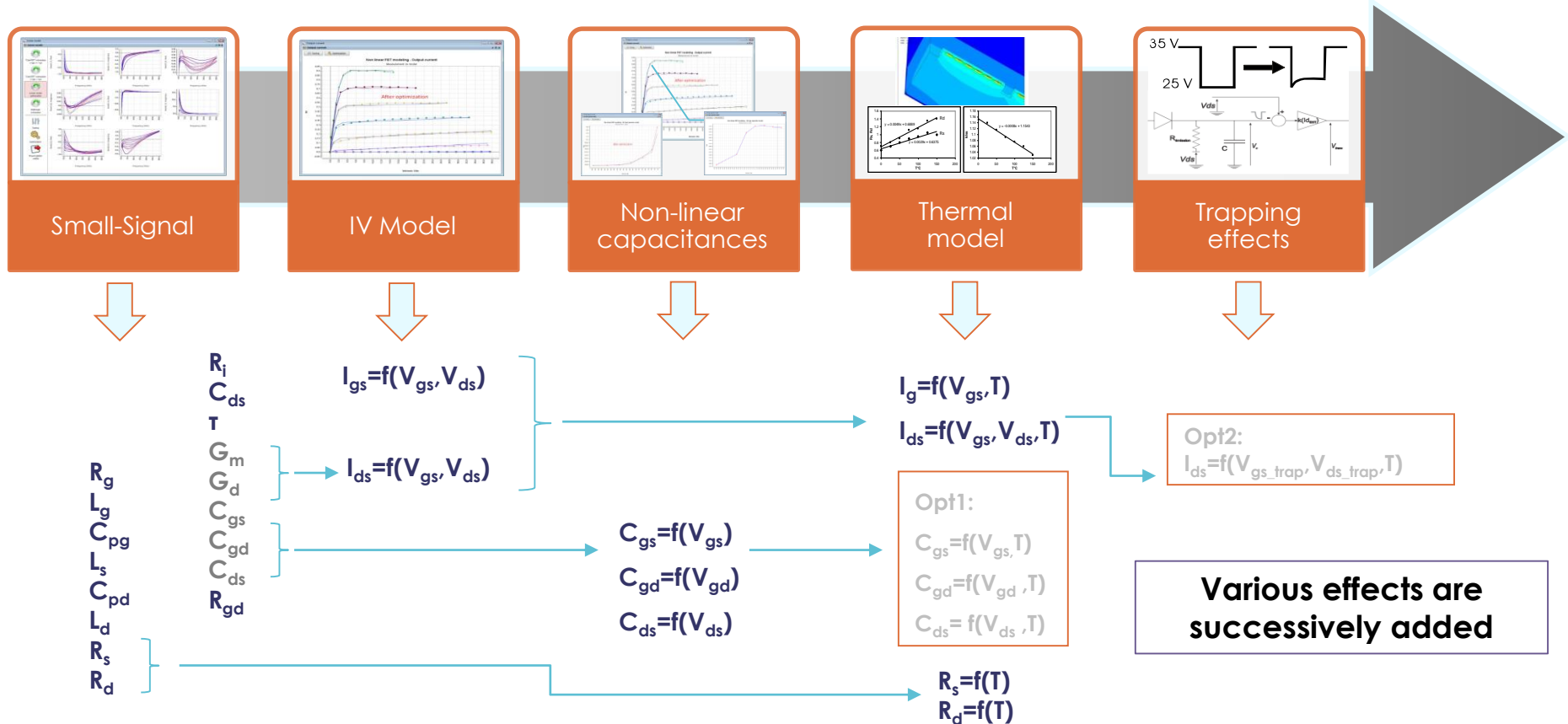


Advantages

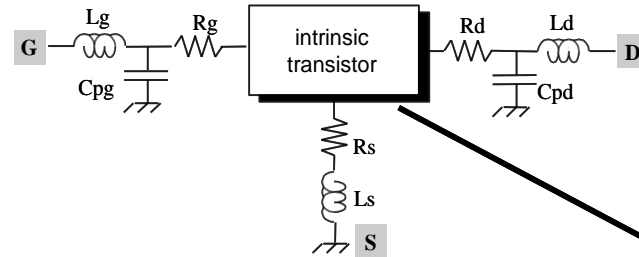
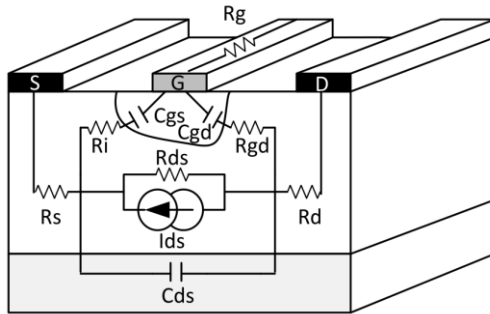
- ✓ High power dissipated areas // safe operating conditions
- ✓ Thermal effects : influence of QP on I_{dss}
- ✓ Trapping effects (gate-lag & drain-lag)
- ✓ Precious modeling data inputs



Model Extraction flow



Small Signal FET modeling

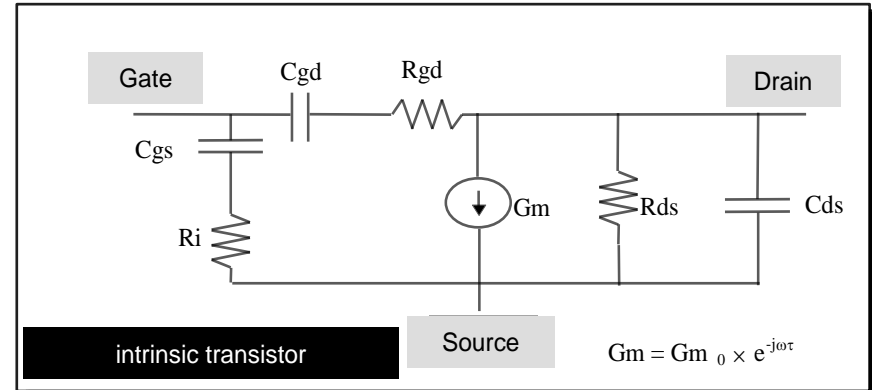


- **Extrinsic parameters**

- pad capacitances C_{pg} , C_{pd}
- port metallization inductances L_g , L_d , L_s
- port ohmic resistances R_g , R_d , R_s

- **Intrinsic parameters**

- channel capacitances C_{gs} , C_{gd}
- voltage-controlled current source with transconductance g_m and transit time delay τ
- ohmic resistances R_i , R_{gd}
- output capacitance C_{ds} and resistance R_{ds}



Small Signal FET modeling

- Extraction of extrinsic and intrinsic parameters:

Four steps

Step 1 (optional) - Extrinsic parameters initialization with cold FET measurements using foundry parameters : Rc

$$Z_{11} = Rg + Rs + \frac{Rc}{3} + \frac{nkT}{qIg} + j\omega(Ls + Lg)$$

$$Z_{21} = Z_{12} = Rs + \frac{Rc}{2} + j\omega Ls$$

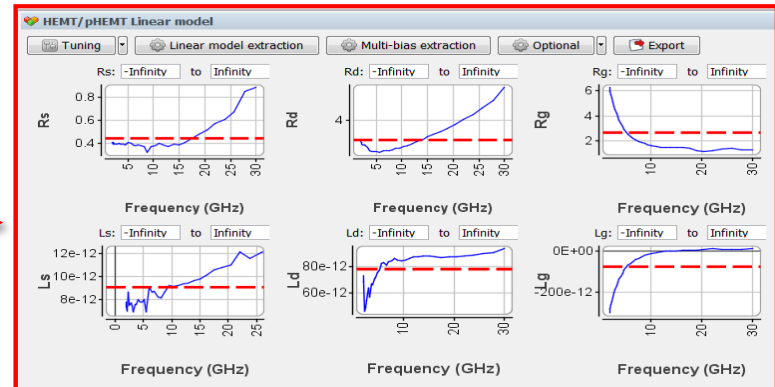
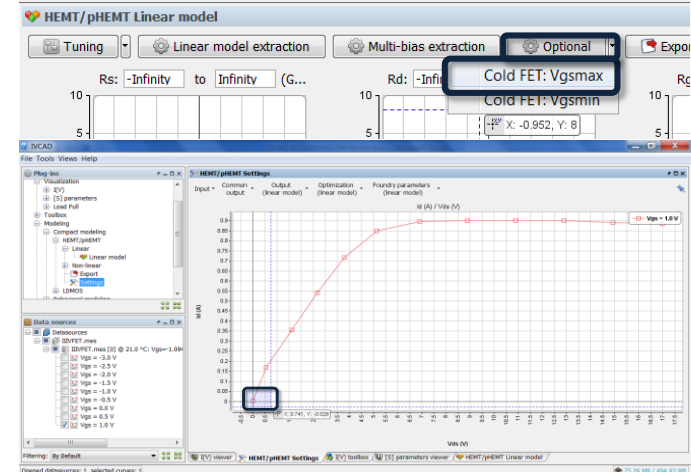
$$Z_{22} = Rd + Rs + Rc + j\omega(Ls + Ld)$$

=> Direct calculus of extrinsic parameters without optimization

$V_{ds} = 0$ V
Channel open $V_{gs} \gg V_p$

$$\begin{aligned} Rs &= \text{real}(Z_{21}) - Rc/2 \\ Rd &= \text{real}(Z_{22}) - \text{real}(Z_{21}) - Rc/2 \\ Rg &\approx \text{real}(Z_{11}) - \text{real}(Z_{21}) + Rc/6 \end{aligned}$$

$$\begin{aligned} Ls &= \text{Im}(Z_{21})/W \\ Ld &= (\text{Im}(Z_{22}) - \text{Im}(Z_{21}))/W \\ Lg &= (\text{Im}(Z_{11}) - \text{Im}(Z_{21}))/W \end{aligned}$$



Small Signal FET modeling

- Step 2 (optional)** : Extrinsic parameters initialization with cold FET measurements

$$\text{Im}(Y_{11}) = j\omega.(Cpg + 2Cb)$$

$$\text{Im}(Y_{21}) = \text{Im}(Y_{12}) = -j\omega.Cb$$

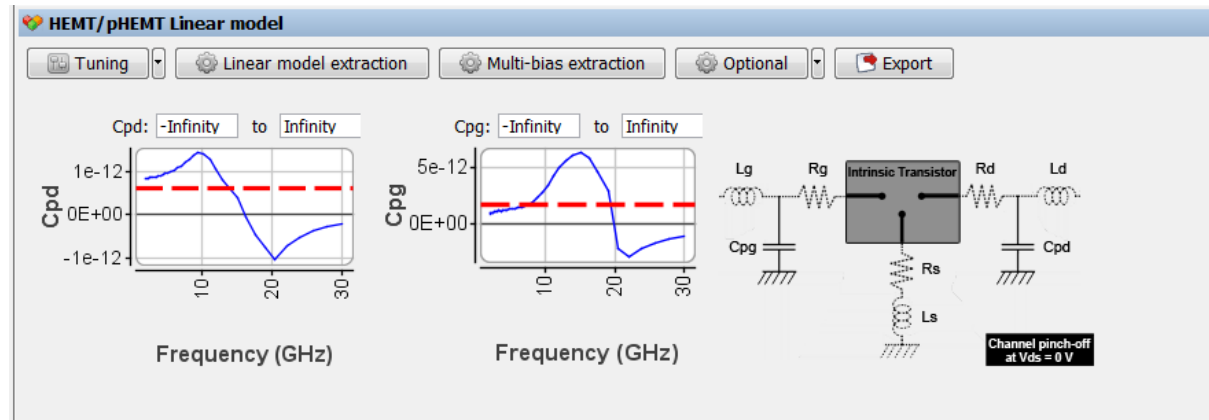
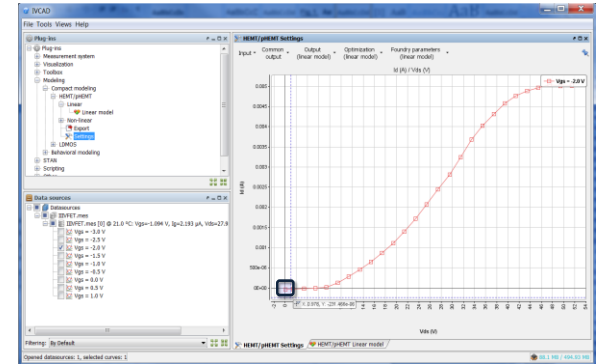
$$\text{Im}(Y_{22}) = j\omega.(Cb + Cpd)$$

=> Direct calculus of extrinsic parameters without optimization

$$Cpd = (\text{Im}(Y_{22}) + \text{Im}(Y_{21}))/W$$

$$Cpg = ((\text{Im}(Y_{11}) + 2 * \text{Im}(Y_{21}))/W$$

$V_{ds} = 0 \text{ V}$
Channel pinch-off $V_{gs} < V_p$

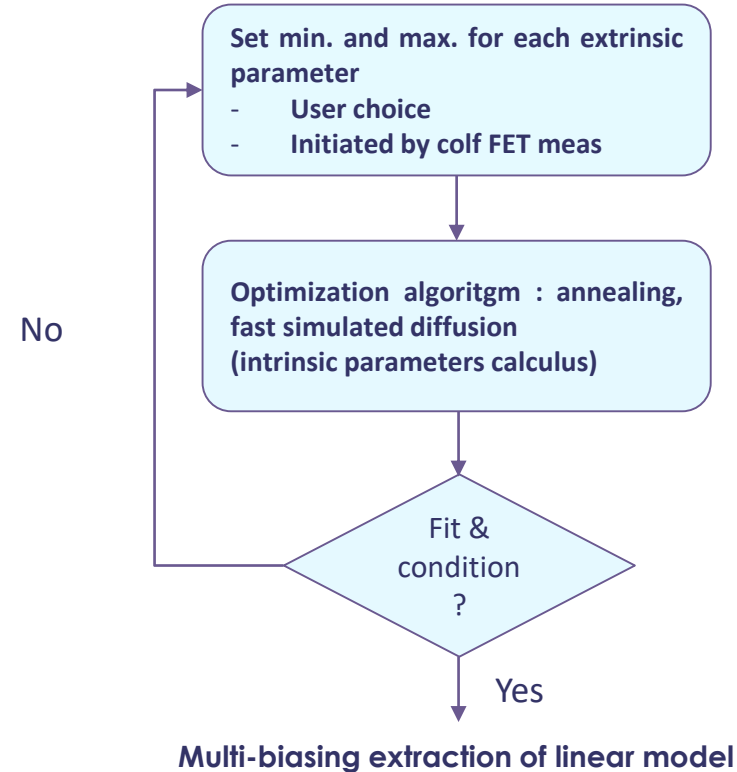


Small Signal FET modeling

- **Extraction of extrinsic and intrinsic parameters:**

For a given set of extrinsic parameters, intrinsic admittance matrix of the device is extracted from measured [S] parameters

Condition : There is only one set of extrinsic parameters for which intrinsic parameters are frequency independent.



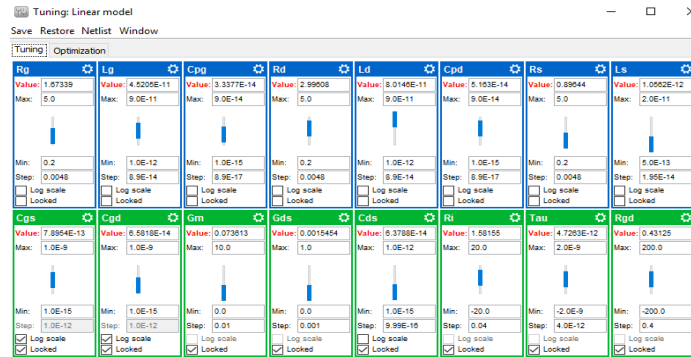
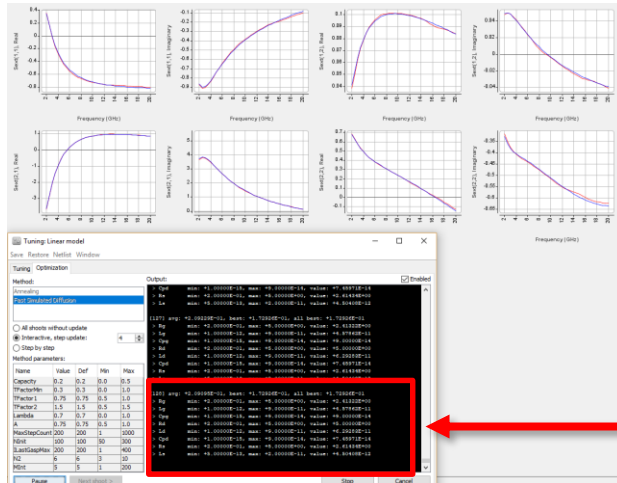
Small Signal FET modeling

• Step 3 : Linear model optimization

Comparison and optimization between calculus and measurement can be done for [S], [Y] or [Z] parameters.



After selecting Linear Model, tuning and optimization are accessible.

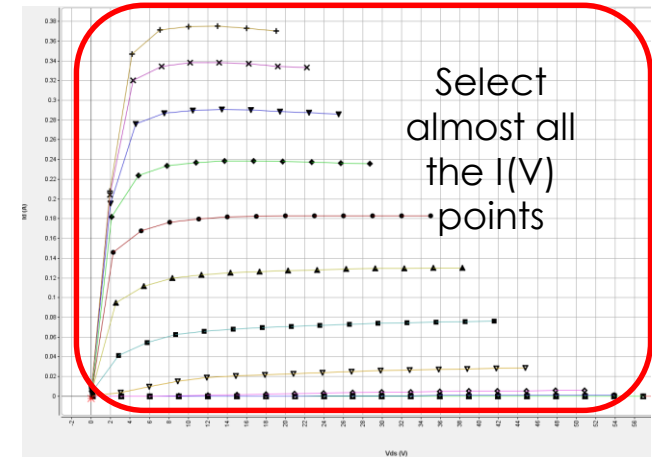
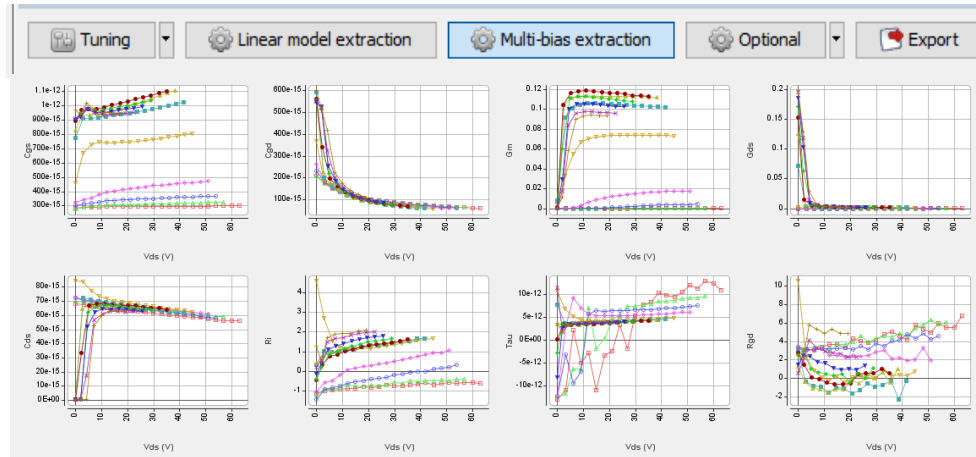


The final and optimized set of parameters. During the optimization, the updated data are displayed in real time.

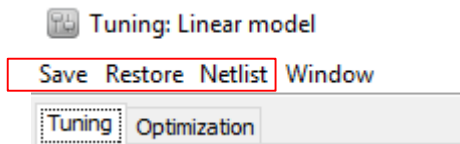
Small Signal FET modeling

• Step 4 : Multi-bias extraction

To check the good behavior of the linear model with the optimized set of parameters, visualize the intrinsic parameters in multi-bias conditions.

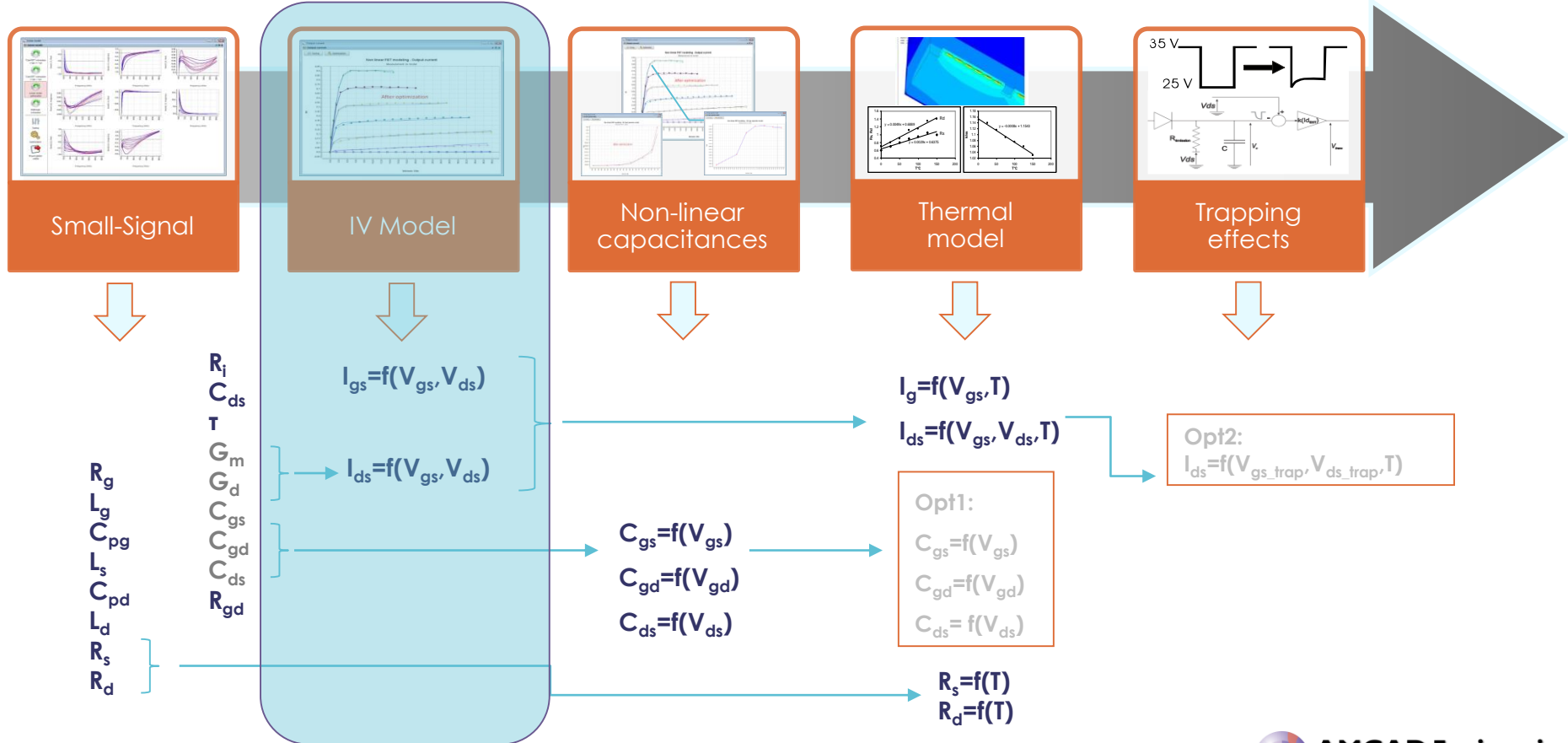


If the intrinsic curves have a good trend, all these parameters can be stored into a buffer or in Netlist file .



Settings : model output, intrinsic parameters;
-> linear model extraction

Model Extraction flow

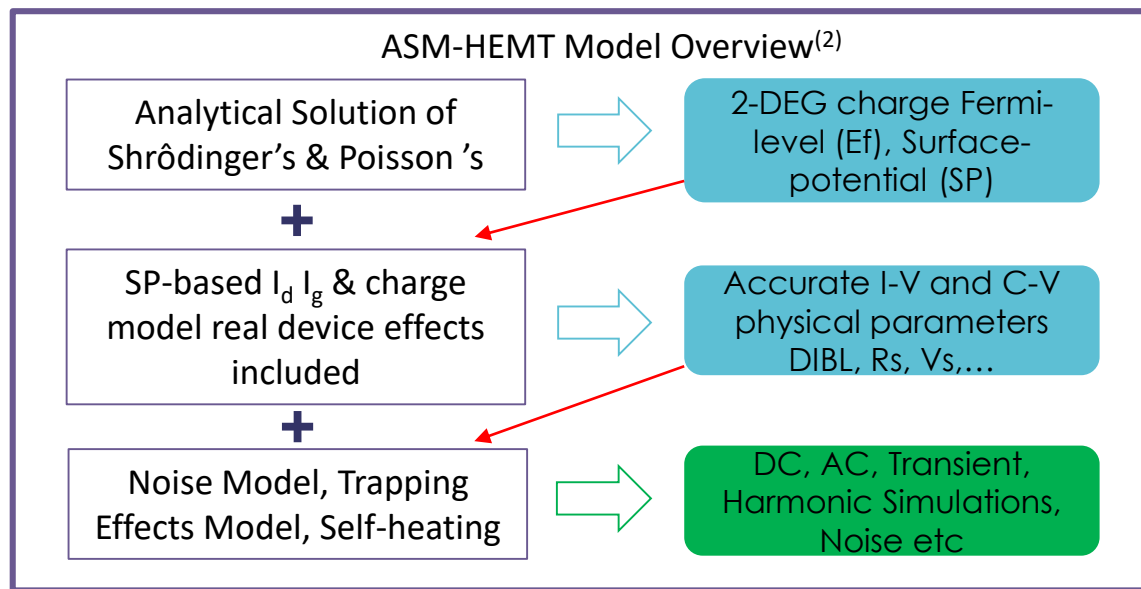


GaN HEMT modeling

ASM linear model is based on extrinsic parameter AMCAD extraction flow in IVCAD

Advanced Spice Model⁽¹⁾ is a CMC candidate models for industry standardization in 2018

ASM is one of the 2 candidates for the Compact Model Coalition with MIT model (MVSG)



ASM
=
Physics based-model

Surface
potential
calculus

Current
& traps

Model for
real device
effets

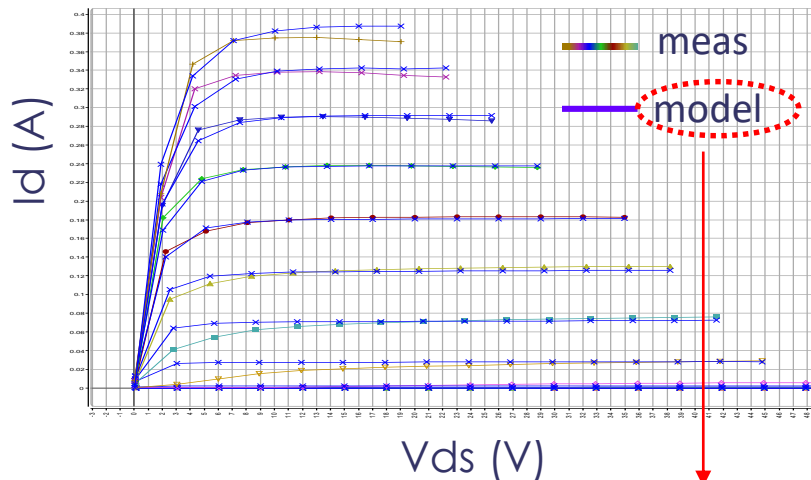
- The variation of E_f (Fermi-level) is divided in function of the gate voltage
- A rigorous charge model for all the terminal charge in the device is present

Real Device Effects Incorporated into the model :

- velocity saturation effect
- mobility field dependance
- subthreshold-slope degradation
- NL series résistances
- flicker noise
- channel lentgh modulation
- drain-induced barrier lowering
- self-heating effect
- temperature dependance ...

Output current source : NEW OPTION → ASM

- In addition to the existing AMCAD current source model, the ASM (3) model has just been added in IVCAD.



```

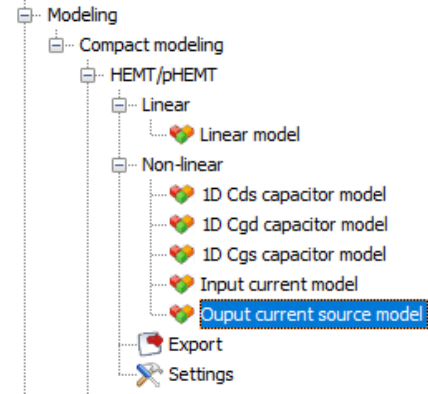
/*Function for Vg0 calculation */
Vdsx =sqrt(Vdsi.*Vdsi.+0.01).-0.1;
Voff_dibl=voff-(eta0).*(Vdsx.*vdscale)./sqrt(Vdsx.*Vdsx.+vdscale.*vdscale);
Voff_dibl_temp = Voff_dibl-(Tdev/Tnom-1)*ktl;
cdsc =1.0.+nfactor.+(cdscd).*Vdsx;
Vtv=KboQ.*Tdev.*cdsc;
t0=1./(2.0.*w.*P_Q.*DOS.*Vtv.*Vtv);
vgmin=Voff_dibl_temp.+Vtv.*log(t0.*imin);
vggmin=0.5.*((Vgsi.-vgmin).+sqrt((Vgsi.-vgmin).*(Vgsi.-vgmin).+1.0e-4)).+vgmin;
Vg0= vggmin.-Voff_dibl_temp;

/*Function for PSIS Calculation*/
vgop=0.5.*Vg0 .+ 0.5.*sqrt(Vg0.*Vg0 .+ 4.0.*ep_psi.*ep_psi);
beta=Cg./(P_Q.*DOS.*Vtv);
ALPHAN=exp(1)./beta;
ALPHAD = 1.0./beta;
vgon = vgop.*ALPHAN./ (sqrt(vgop.*vgop .+ ALPHAN.*ALPHAN));
vgod = vgop.*ALPHAD./ (sqrt(vgop.*vgop .+ ALPHAD.*ALPHAD));
Rx=(vgop .+ Vtv.*(1.0-log(beta.*vgon)).-(GAMMA0Ival./3.0).*(Cch.*vgop)**(2/3))
    
```

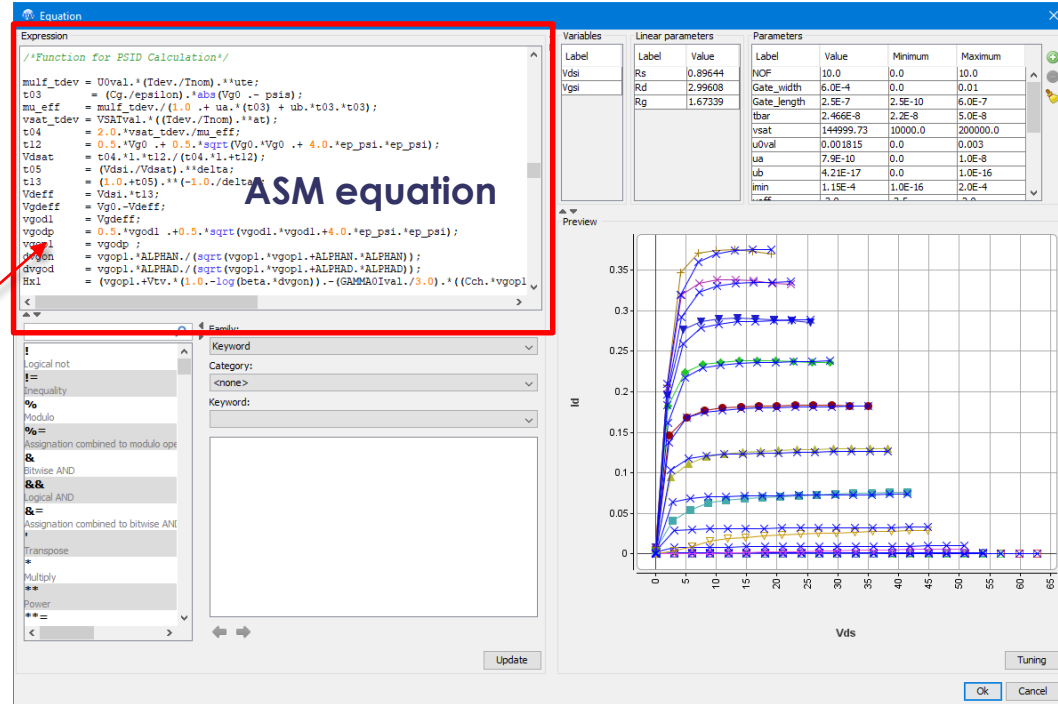
Name	Definition	Units	Default
NOF	Number of fingers	none	3.00
Gate_width	Gate width	m	2.00E-4
Gate_length	Gate length	m	2.50E-7
tbar	Barrier layer thickness	m	2.72E-8
vsat	Saturation velocity	m/s	4,20E6
at	Temperature dependence coefficient for saturation velocity	none	0.0
u0val	Low field mobility	m ² /(V*s)	0.18
ua	Mobility degradation coefficient first order	V-1	4.40E-9
ub	Mobility degradation coefficient second order	V-2	1.00E-16
ute	Temperature dependence coefficient of mobility	none	1.00
imin	Minimum drain current	A	1.00E-15
voff	Pinch off voltage	V	-2.608
lambda	Channel length modulation coefficient	V-1	-3.5E-3
delta	Exponent for Vdeff coefficient	none	0.67
thesat	Velocity saturation parameter	V-2	1.37
nfactor	Sub-voff slope parameters	none	4.64
cdscd	Sub-voff slope change due to drain voltage	None	0.19
epsilon	Dielectric Permittivity of AlGaIn layer	F/m	10.66E-11
eta0	DIBL Parameter	none	1E-9
vdscale	DIBL Scaling VDS	V	5
gdsmin	Convergence parameter	S	1.0E-12

Output Current Source

The extrinsic parameters values are common to the linear and non-linear model.



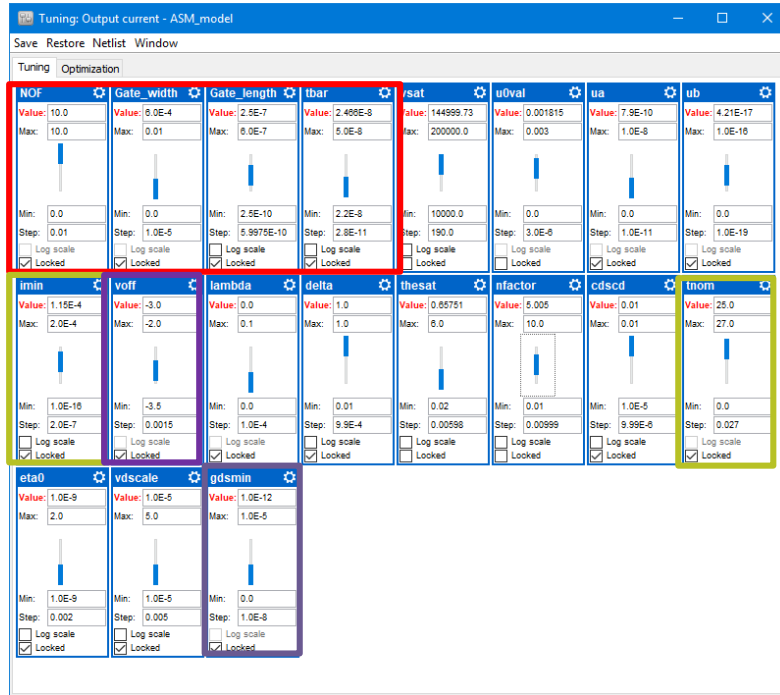
For the nonlinear part it is possible to use the AMCAD model or a custom model.



Equation editor is implemented to allow the customer to build his custom model.

Output Current Source

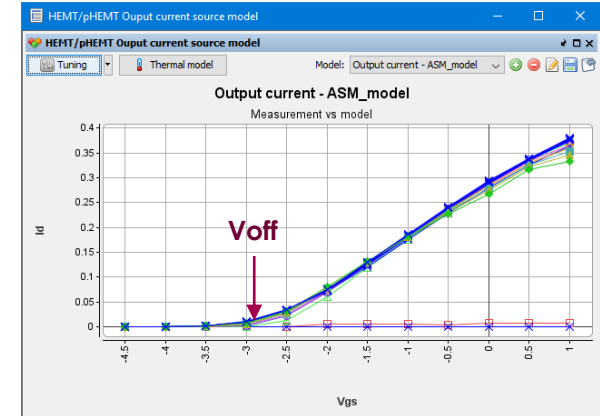
Model optimization methodology



Locked Parameters

- Physical parameters
- Nominal T° measurements
- Convergence parameters
- Imin : Pinch off Current
- Voff : Pinch off Voltage

...



Diodes : NEW OPTION → ASM

- Gate-drain and gate-source diode equations :

$$I_{gs} = w * l * nf * |t_3| * (exp^{t_0} - 1)$$

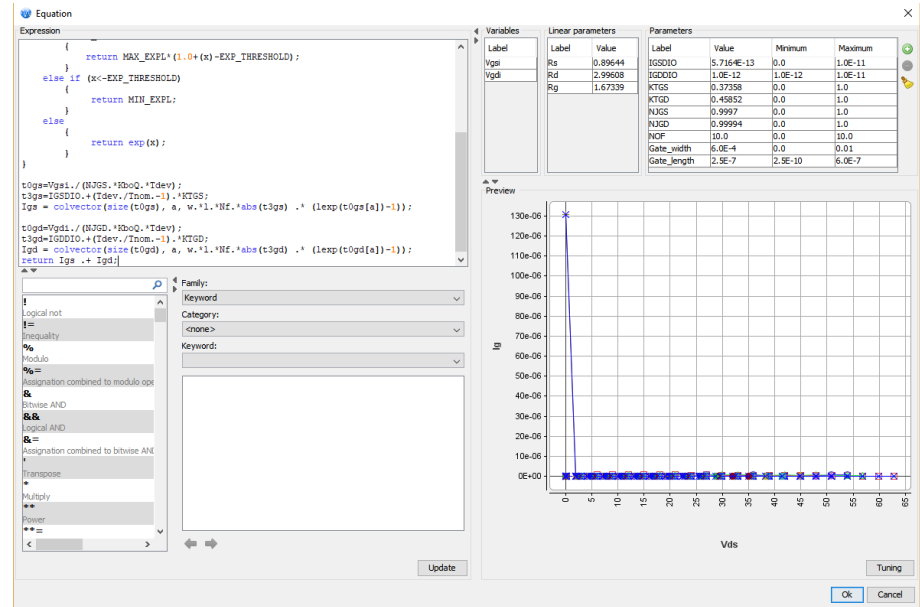
$$t_0 = \frac{V_{gsi}}{njgs * KboQ * T_{dev}}$$

$$t_3 = igstdio + \left(\frac{T_{dev}}{T_{nom}} - 1 \right) * ktgs$$

$$I_{gd} = w * l * nf * |t_3| * (exp^{t_0} - 1)$$

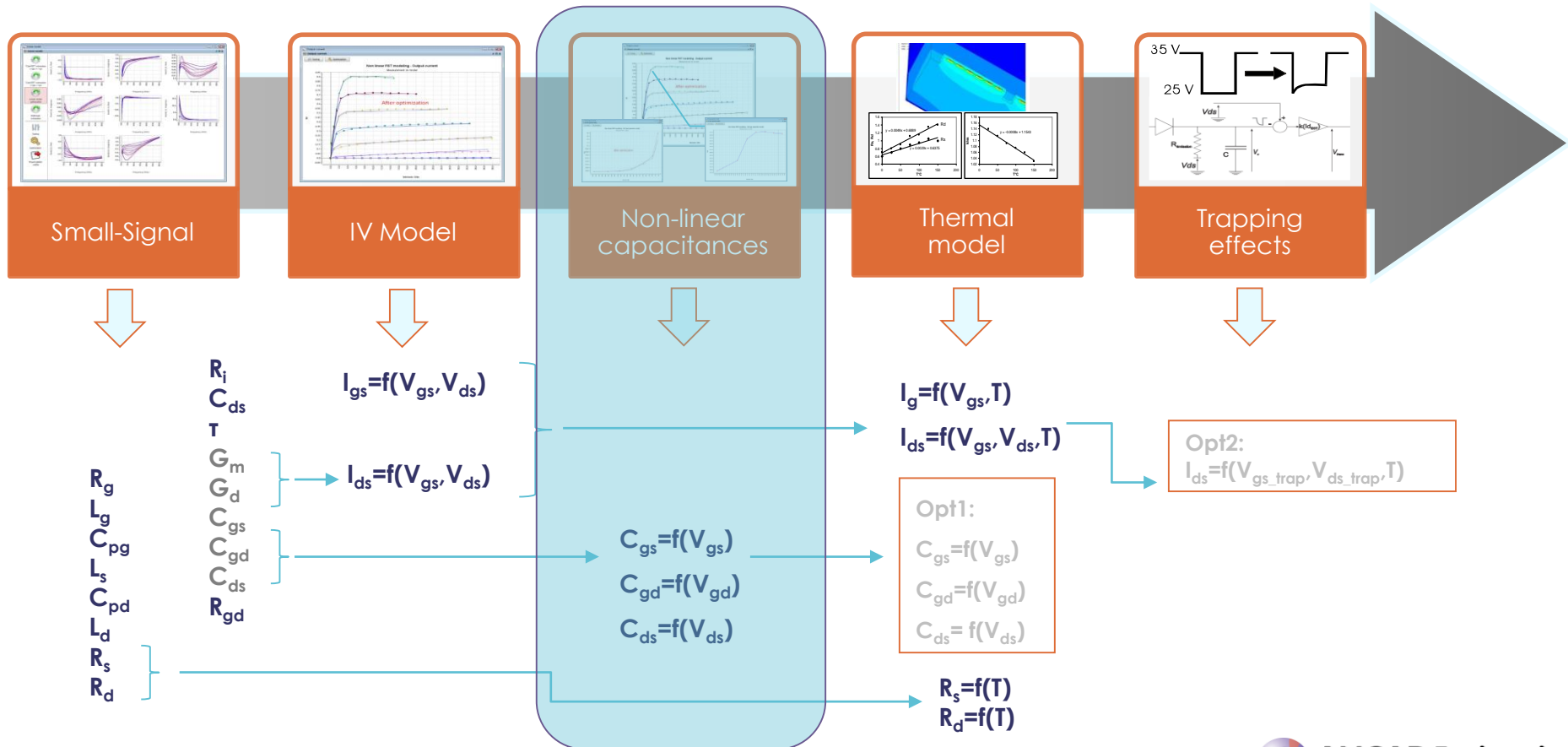
$$t_0 = \frac{V_{gsi}}{njgd * KboQ * T_{dev}}$$

$$t_3 = igddio + \left(\frac{T_{dev}}{T_{nom}} - 1 \right) * ktgd$$



Name	Definition	Units	Default
igstdio	Gate-source junction diode saturation current	A/m^2	1
njgs	Gate-source junction diode current ideality factor	None	2.5
igddio	Gate-drain junction diode saturation current	A/m^2	1
njgd	Gate-drain junction diode current ideality factor	None	2.5
ktgs	Temperature co-efficient of gate-source junction diode current	None	0
ktgd	Temperature coefficient of gate-drain junction diode current	None	0

Model Extraction Flow

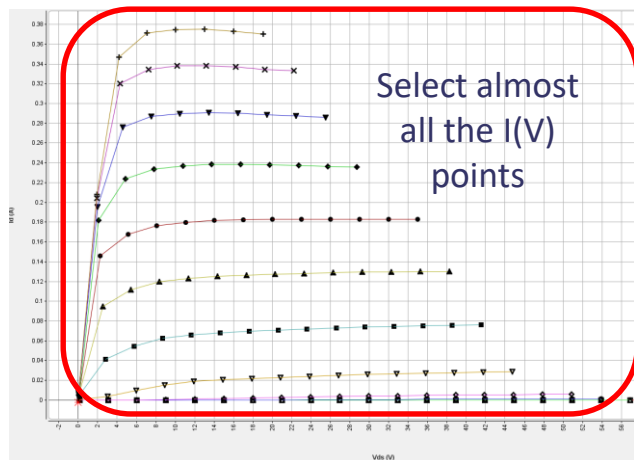


Non-linear capacitances : NEW OPTION → ASM

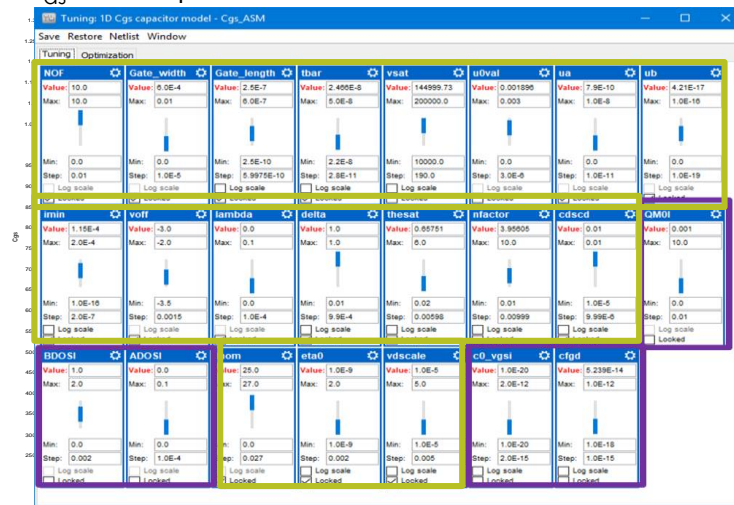
C_{gs}

- Input capacitance C_{gs} is strongly influenced by V_{gs} and weakly influenced by V_{ds} .

In ASM model the C_{gs} capacitance depends on both V_{gs} & V_{ds} , 2D capacitance.



Reuse of the current source parameters



```
/*QGI_gate_charge_calculation*/
```

```
tlg = psid - psis;
t2g = Vg0 + Vtv - psim;
t3g = (Cg.*W.*Nf.*1).*(Vg0.-psim.+0.5.*tlg./(6.0.*t2g));
T0g = 1e+26.*(t3g./QM0I);
Tlg = 1.0 + (T0g.*BDOSI);
XDCinv = ADOSI./Tlg;
Cg_qme = epsilon./ (tbar + XDCinv);
qgint = (Cg_qme.*W.*Nf.*1).*(Vg0.-psim.+0.5.*tlg./(6.0.*t2g)).+c0_vgsi.*Vgsi.+cfgd.*Vgsi;
```

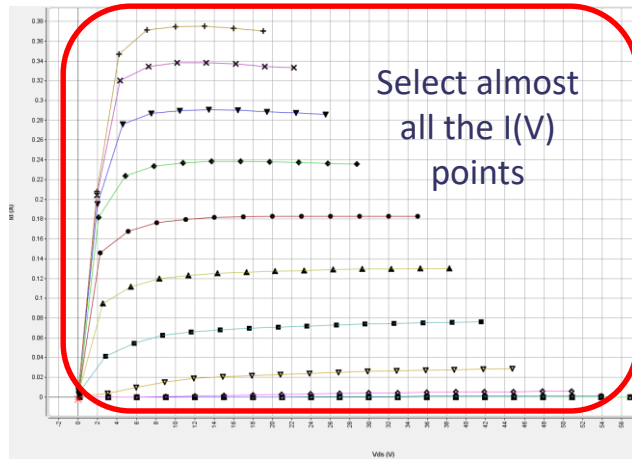
Name	Definition	Units	Default
QM0I	Charge centroid parameter - starting point for QME in inversion	none	1E-3
BDOSI	Charge centroid parameter - slope of CV curve under QME in inversion	none	1
ADOSI	Quantum mechanical effect pre-factor cum switch in inversion	none	0
cgso	Gate-source overlap capacitance	F	0.0E-18
cfgd	Fringing capacitance parameter	F	1E-13

Non-linear capacitances : **NEW OPTION → ASM**

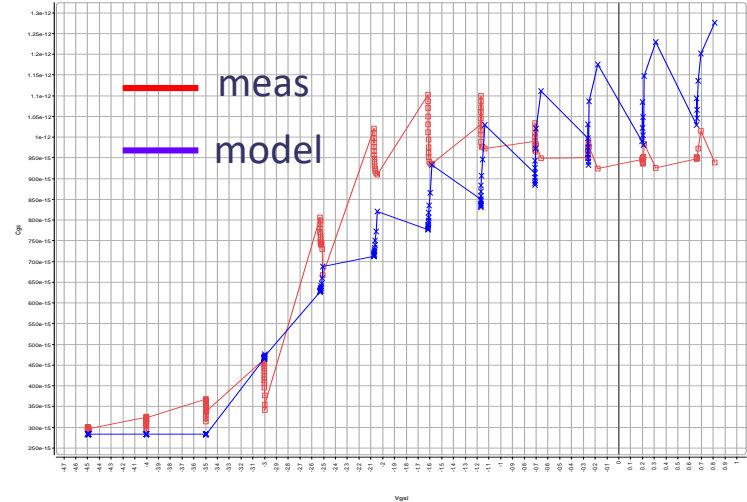
C_{gs}

- Input capacitance C_{gs} is strongly influenced by V_{gs} and weakly influenced by V_{ds} .

In ASM model the C_{gs} capacitance depends on both V_{gs} & V_{ds} , 2D capacitance.



C_{gs}
capacitance
extracted on
the entire I(V)
network



```
/*QGI_gate_charge_calculation*/
```

```
tlg = psid .- psis;  
t2g = Vg0 .+ Vtv .- psim;  
t3g = (Cg.*w.*Nf.*1).*(Vg0.-psim.+0.5.*tlg.*tlg./(6.0.*t2g));  
T0g = 1e+26.*(t3g./QM0I);  
Tlg = 1.0 .+ (T0g.*BDOSI);  
XDCinv = ADOSI./Tlg;  
Cg_qme = epsilon./(tbar .+ XDCinv);  
qgint = (Cg_qme.*w.*Nf.*1).*(Vg0.-psim.+0.5.*tlg.*tlg./(6.0.*t2g)).+c0_vgsi.*Vgsi.+cfgd.*Vgsi;
```

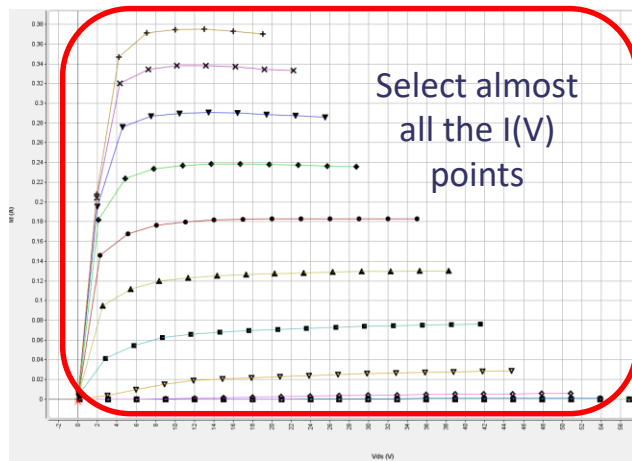
Name	Definition	Units	Default
QM0I	Charge centroid parameter - starting point for QME in inversion	none	1E-3
BDOSI	Charge centroid parameter - slope of CV curve under QME in inversion	none	1
ADOSI	Quantum mechanical effect pre-factor cum switch in inversion	none	0
cgso	Gate-source overlap capacitance	F	0.0E-18
cfgd	Fringing capacitance parameter	F	1E-13

Non-linear capacitances : NEW OPTION → ASM

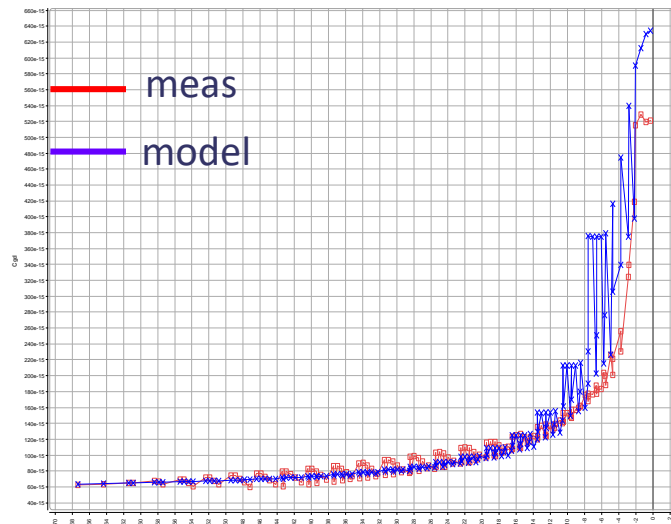
C_{gd}

- Feedback capacitance C_{gd} is a strong function of drain voltage.

Inclusion of this effect is necessary to fit large-signal data.



C_{gd}
capacitance
extracted on
the entire I(V)
network



Name	Definition	Units	Default
vdsatcv	Saturation voltage on drain side in CV Model	V	100
cgdo	Gate-drain overlap capacitance	F	0.0E-18
cgdl	Vds bias dependence of parasitic gate drain overlap capacitance	F	0.0E-15
cfgd	Fringing capacitance parameter	F	1E-12
ktcfgd	Temperature dependence of Fringing capacitance	F	0
cfgdsm	Capacitance smoothing parameter	F	1E-24

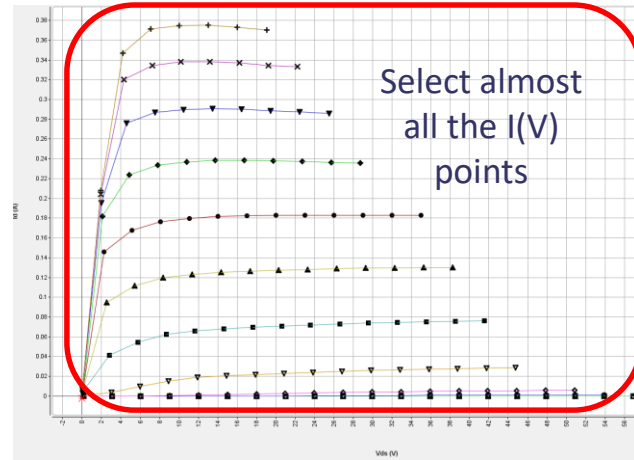
```
VdeffCV = (Vdsi.*vdsatcv)./sqrt(Vdsi.*Vdsi.+vdsatcv.*vdsatcv);
cgdvar = cgdo.-cgdl.*VdeffCV;
qfrl = cfgd0.-(cfgd.+(Idev./Inom.-1).*ktcfgd).*Vdsi;
qfr = 1e-25.+qfrl.-0.5.*(1e-25.+qfrl.-sqrt((qfrl.-1e-25).*(qfrl.-1e-25).+cfgdsm)).
qgdo = cgdvar.*Vgdi;
```

Reuse of C_{gs} capacitance
parameter

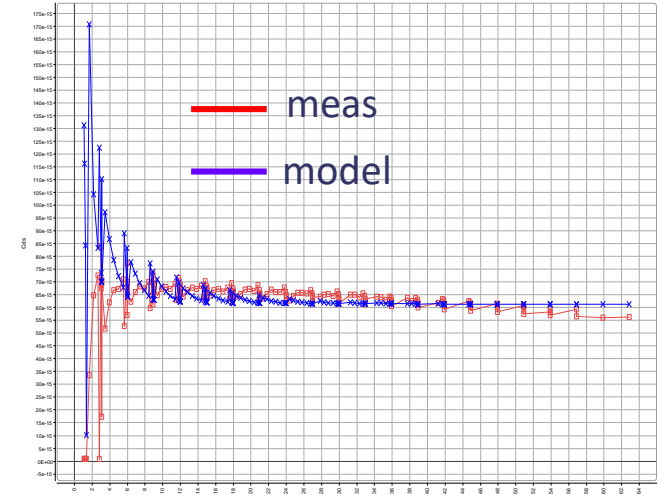
Non-linear capacitances : NEW OPTION → ASM

C_{ds}

- It is possible to have a C_{ds} capacitance function of the V_{ds} voltage.



C_{ds}
capacitance
extracted on
the entire I(V)
network



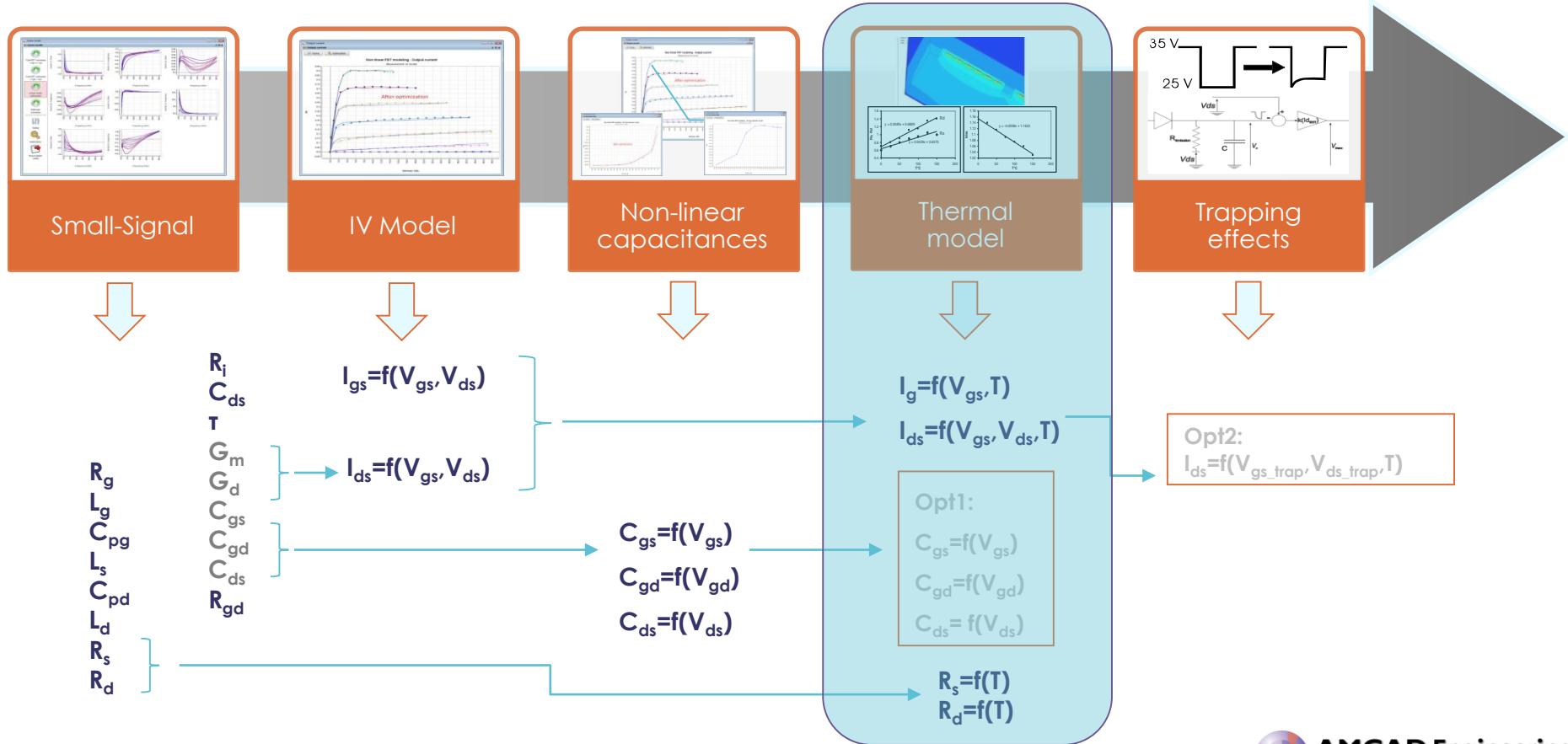
Name	Definition	Units	Default
cdso	Cds capacitance parameter	F	0E-18
vbi	Built in potential	V	0.9
cj0	Zero bias depletion capacitance	F	0E-15
mz	Grading factor of depletion capacitance	None	0.5
aj	Limiting factor of depletion capacitance in forward bias region	None	100E-3
dj	Fitting parameter	None	1

/*QDI_drain_charge_Calculation*/

```

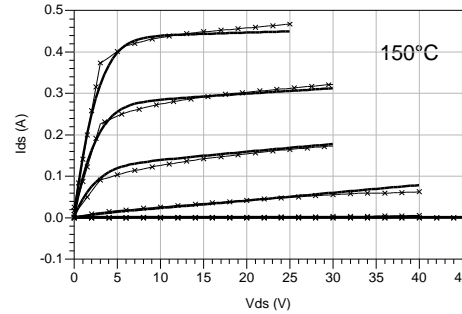
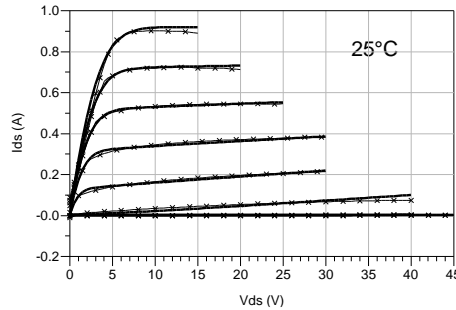
t0d = Vg0 .+ Vtv .- psim;
t1d = (psis .+ 2.0.*psid)/3.0;
t2d = (1/12).*(psid.*psid)/t0d;
t3d = (1/120).*(psid.*psid.*psid)/(t0d.*t0d);
t0qdep=(vbi .- (Tdev./Tnom .- 1.0).*ktvbi).*(1.0.-exp(-log(aj)./mz));
Vth= Kb0Q.*Tdev;
tlqdep=(t0qdep.+Vds1)/Vth;
t2qdep=sqrt(dj.*tlqdep.*tlqdep.+ 1.92);
t3qdep=(tlqdep.+t2qdep)*0.5;
t4qdep=t0qdep.-Vth.*t3qdep;
t6qdep=log(1.0.-t4qdep./vbi);
t8qdep=cj0.*(vbi .- (Tdev./Tnom .- 1.0).*ktvbi).*(1.0.-exp(t6qdep.*(1.0.-mz)))/(1.0.-mz);
Qdep=t8qdep+aj.*cj0*(-Vds1-t4qdep);
q dint = -(Cg_gme.*w.*1.*Nf.*0.5).*(Vg0 .- t1d .+ t2d .+ t3d);
    
```

Model Extraction Flow

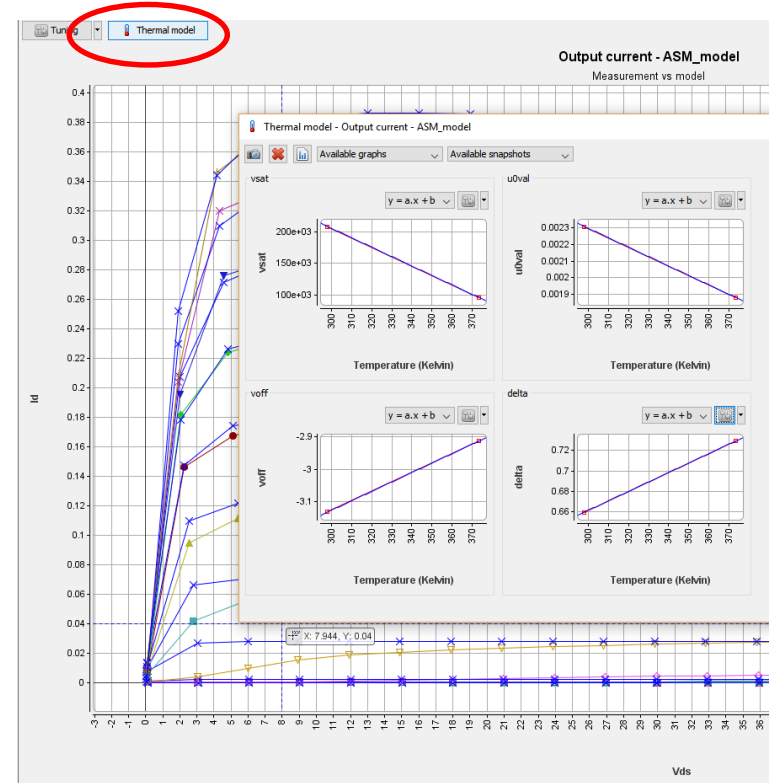


Thermal effects with IVCAD

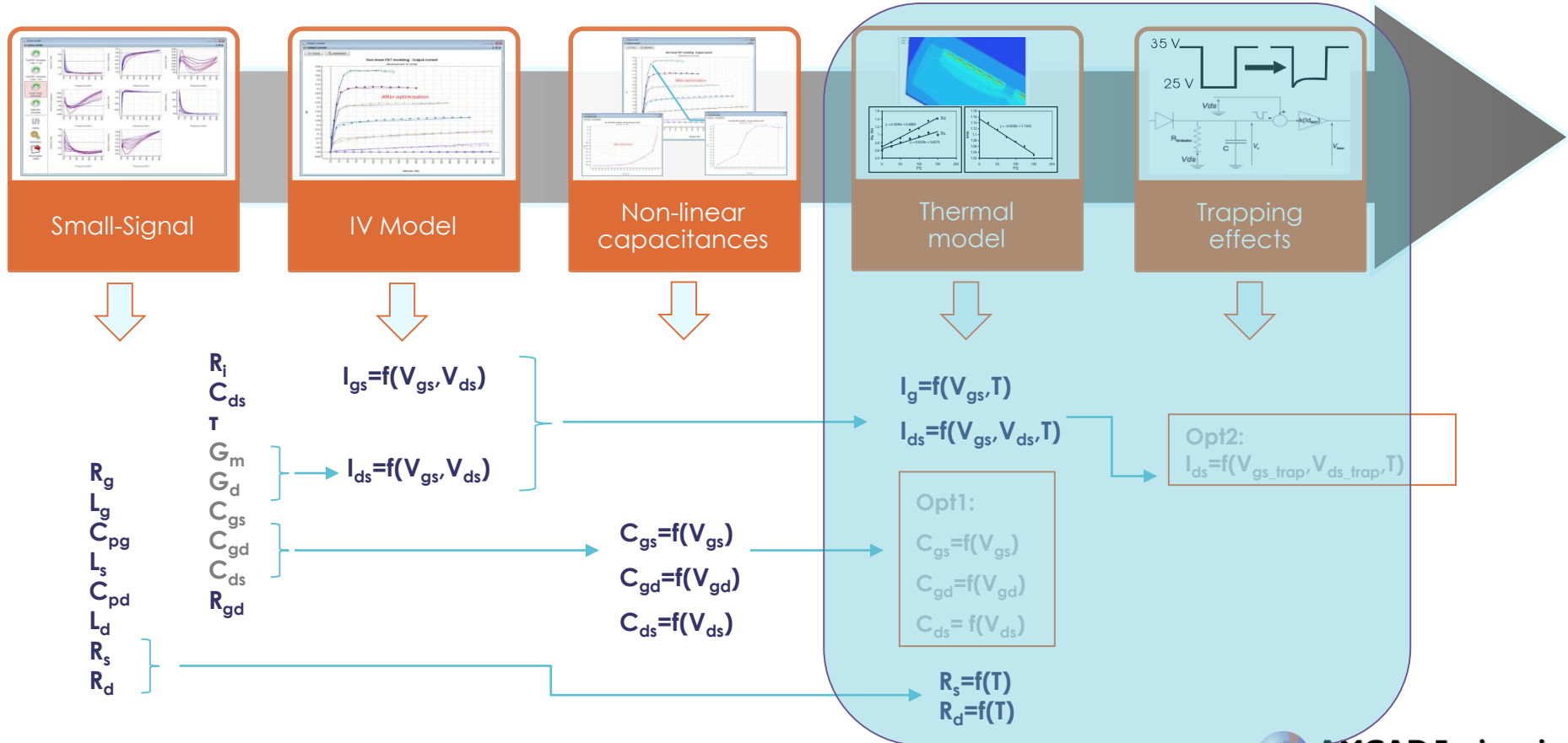
- Temperature dependence with ambient or chuck temperature



IVCAD can be used to model thermal effects on different parameters of current source and capacitances.



Model Extraction Flow



Thermal and Trapping effects

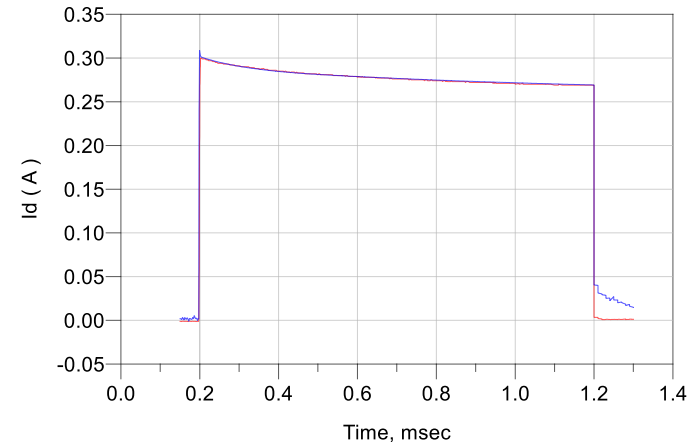
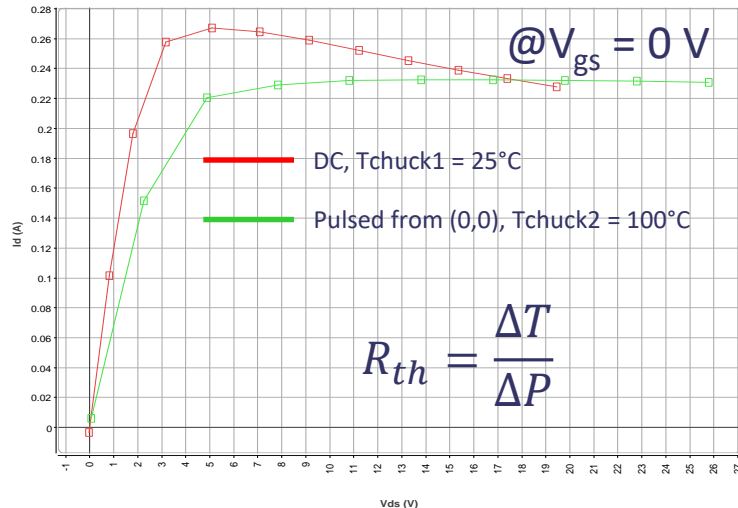
- Thermal and Trapping effects require a time-based simulator. IVCAD software does not have an on-board simulator. That's why, the thermal and trapping effect included in AMCAD models are implemented using commercial software like Advanced Design System.

Trapping Effects :

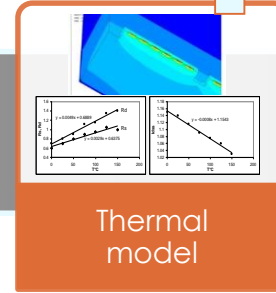
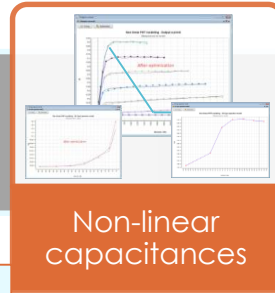
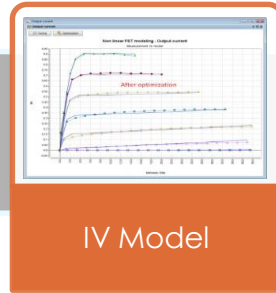
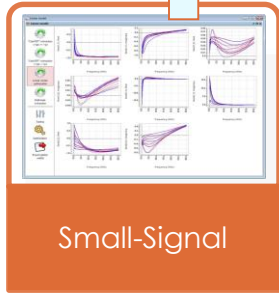
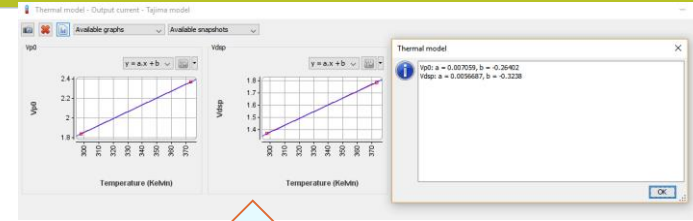
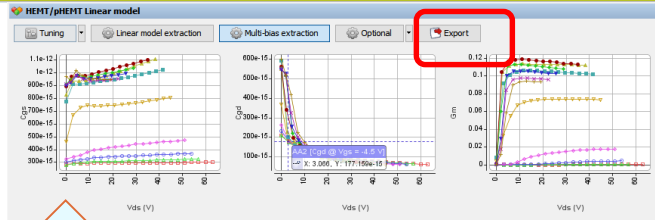
→ Gate-lag & Drain-Lag measurements.

Thermal resistance extraction → Coincidence method / Del Alamo method

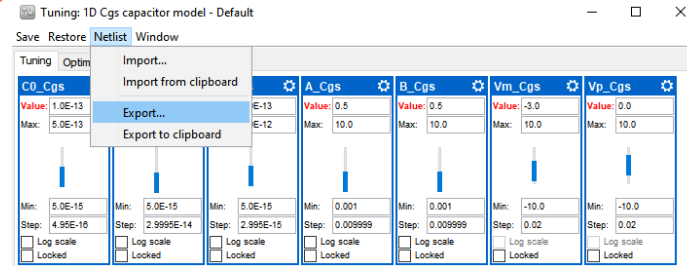
Thermal impedance extraction → Drain long pulse characterization



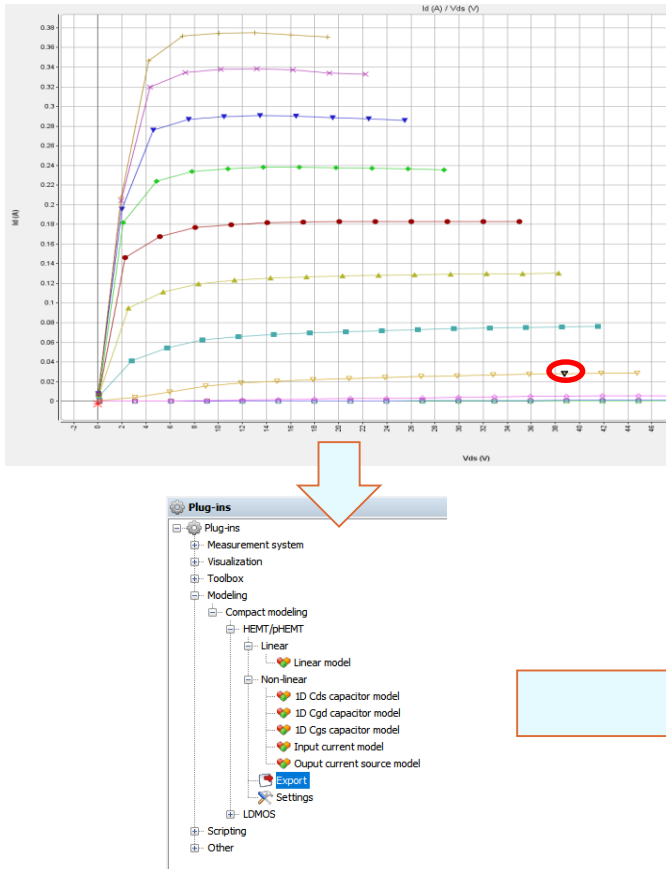
Export



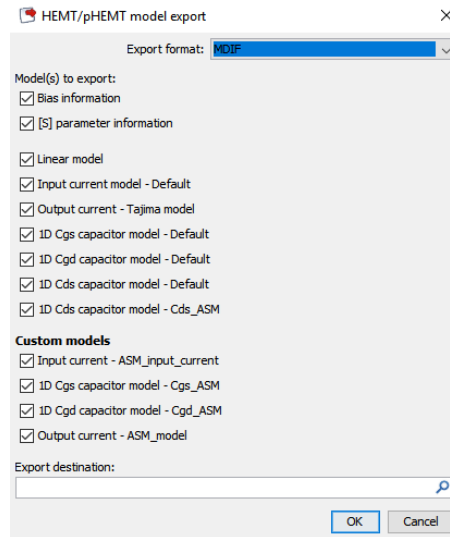
Commercial Simulators



Export



- To export the nonlinear model, select only one point of the I(V) network.



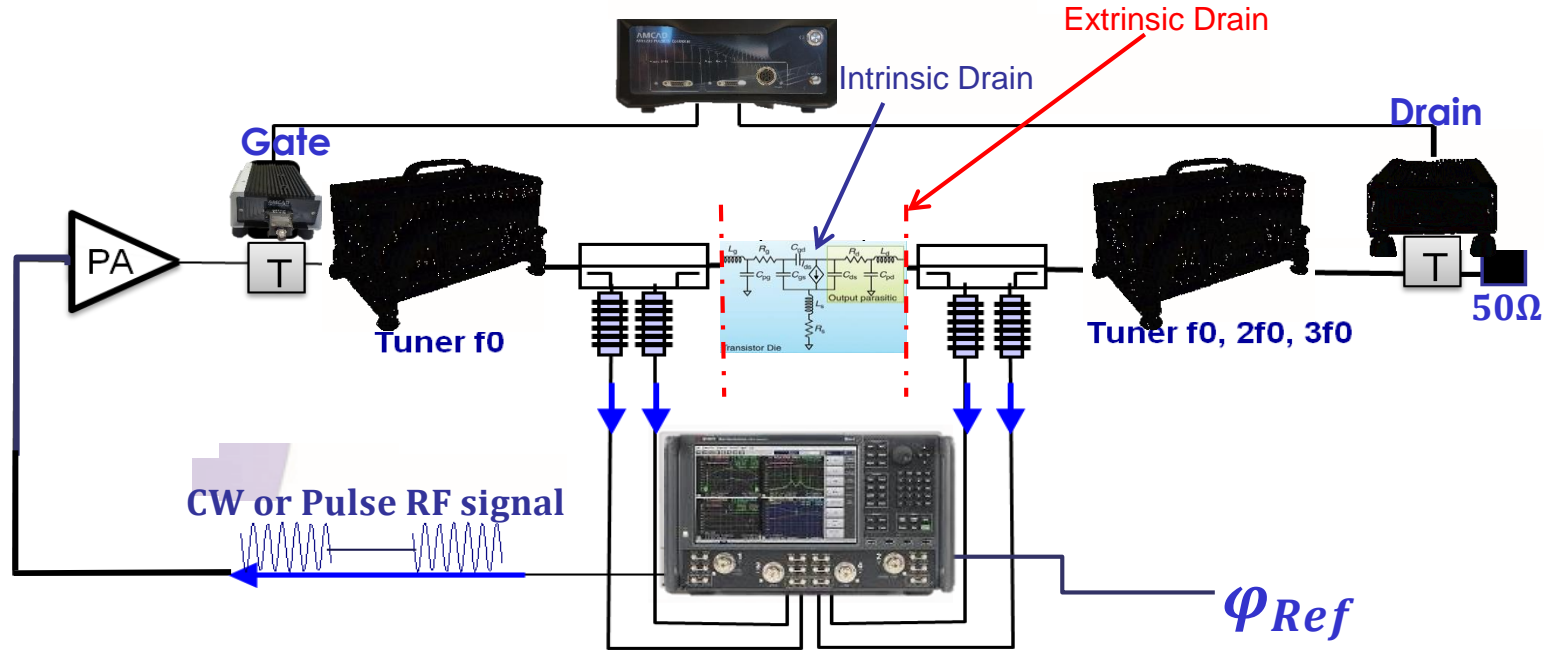
Example netlist file

Generated by IVCAD at 2019/01/09 14:56:08

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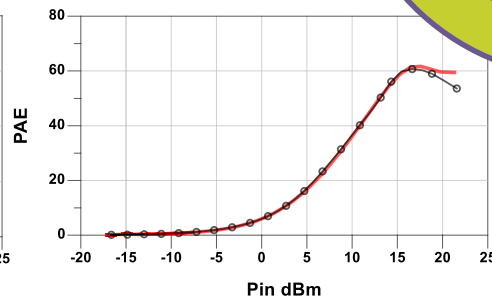
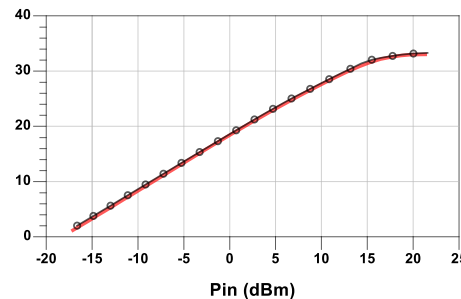
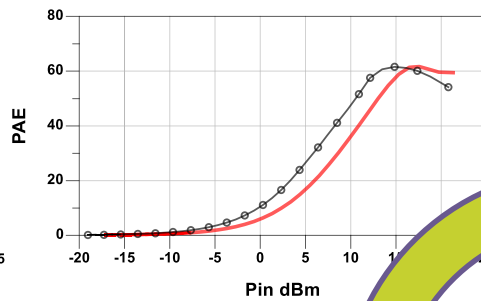
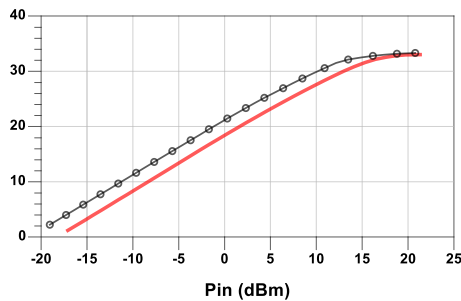
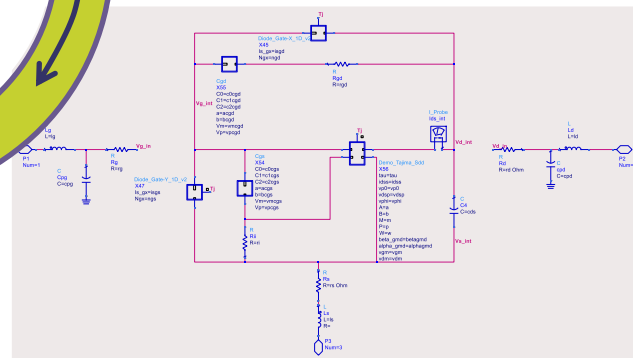
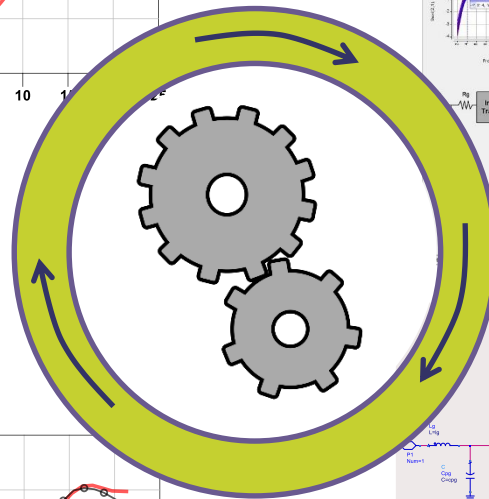
Large Signal model validation

Empiric Load Pull measurements at the extrinsic planes



Application specific Load Pull Validation: ASM model

Modeling and validation flow



Q&A

Thank you

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