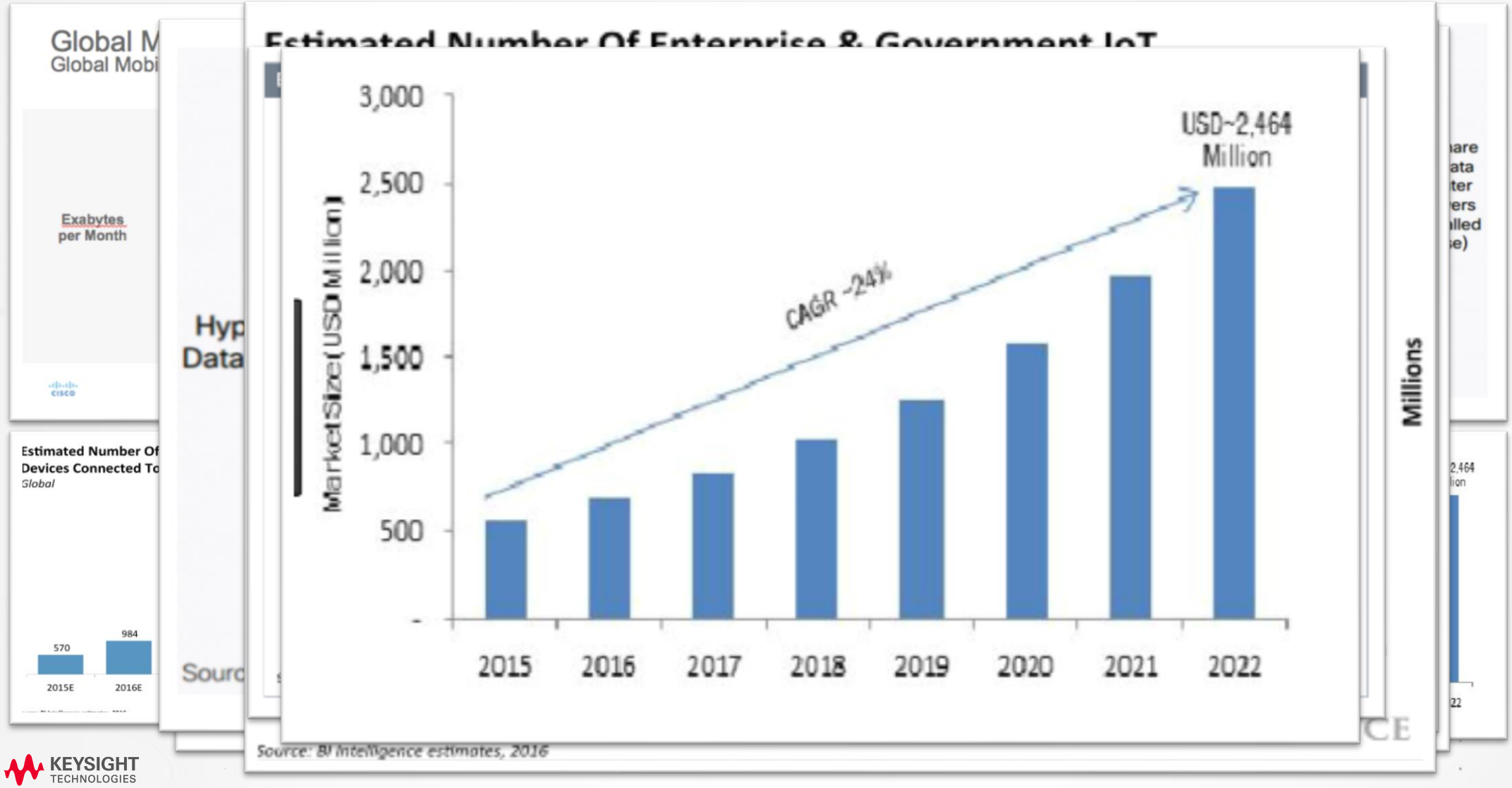
Understanding the Test Impacts to Today's High-Speed Digital Trends

Brig Asay	***2019-04***
Keysight Technologies	

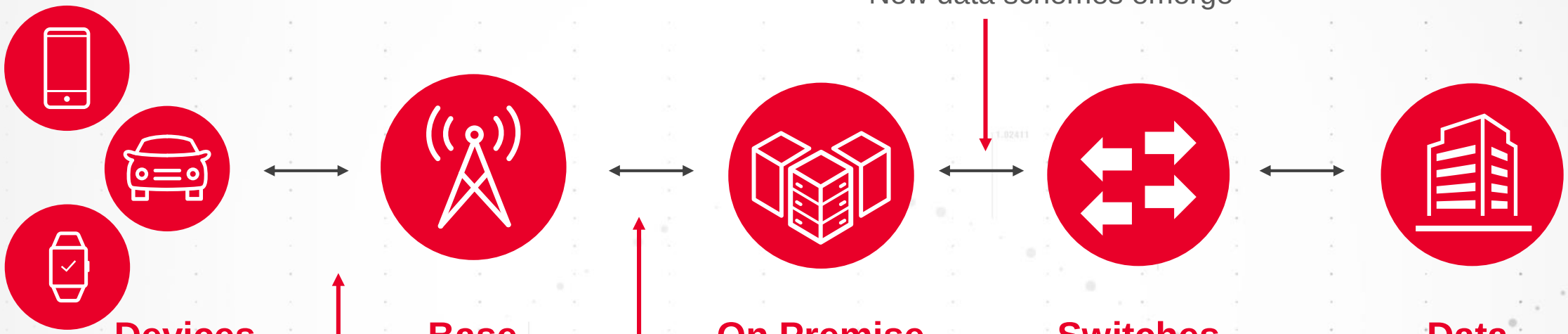
The New Age… Digital is Being Pushed

CONSUMERS AND THEIR INSATIABLE DEMAND FOR MORE DATA



Technology Trends

- Network capacity crunch drives the need to push more data through the same channel
- New data schemes emerge



Devices

- 5G acceleration: China/6GHz leading, mmWave following
- Small cell and Wi-Fi integration drive the complexity of network test

Base Station

- Mobile Edge Computing grows rapidly - data center traffic moves to the base-band unit (BBU)
- Drives the need for fronthaul analysis, eCPRI takes over

On Premise Server

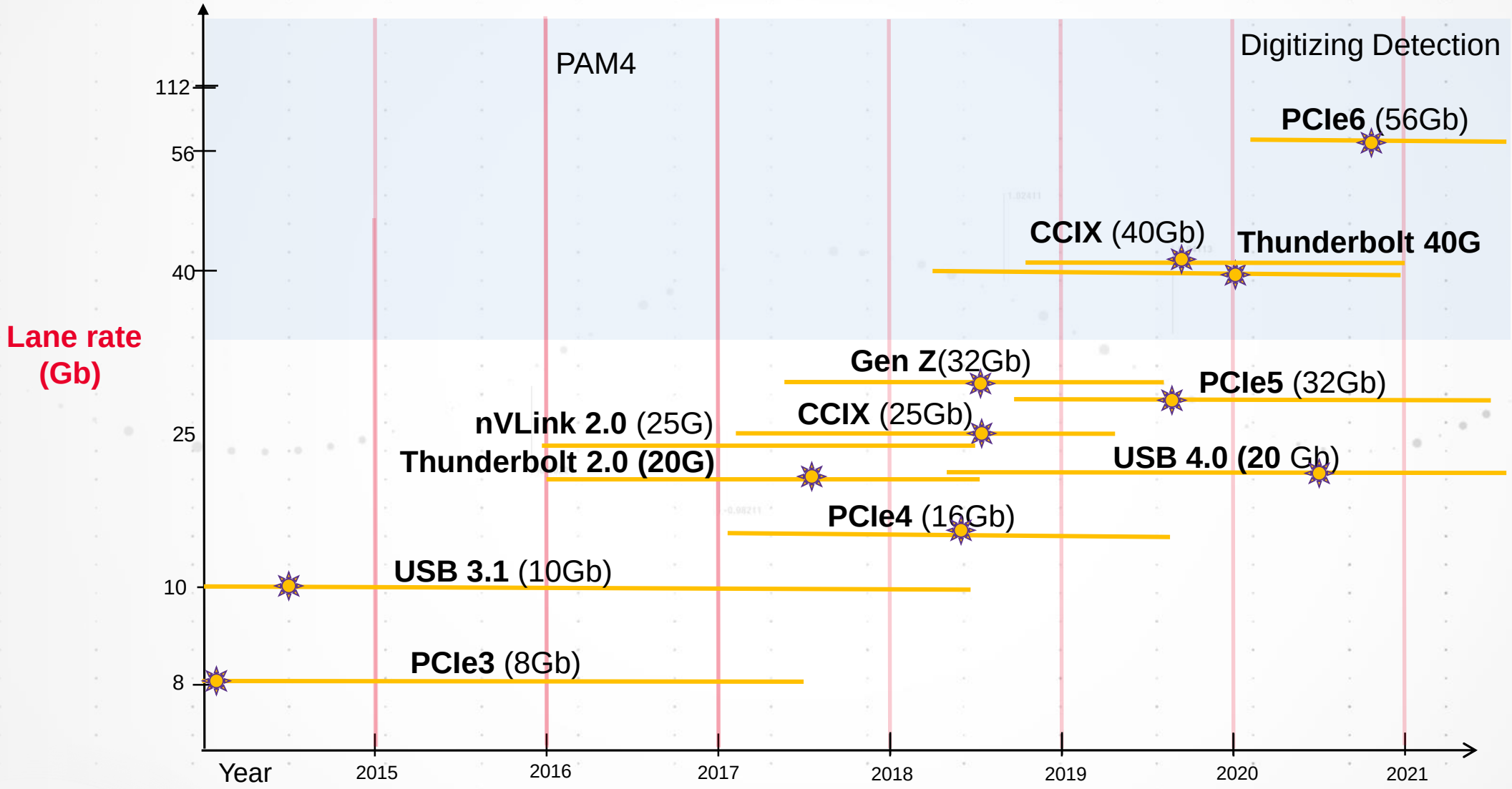
Switches

- Increased data loads drive the need for faster switching speeds - 400G gives way to 800G

Data Center

- Hyperscaling increases speeds throughout the data center
- New switch architectures are defined
- New standards emerge (CCIX, GenZ, OpenCAPI, gen5)

High-Speed Computing Roadmap



Top Three Bus Technologies Evolve

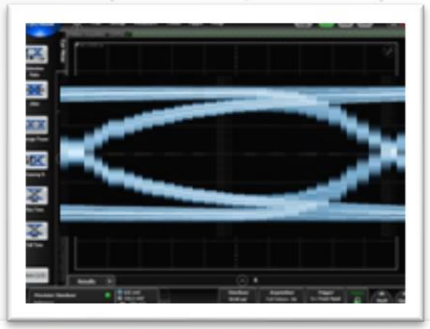
- DDR is moving to DDR5
- PCI Express (PCIe) is moving to PCIe Gen5
- USB is moving to USB 3.2 and then to 4.0

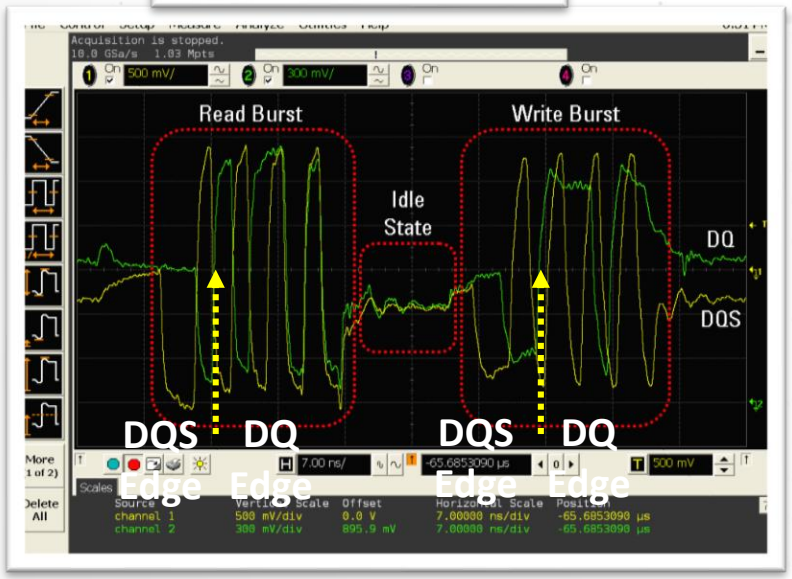
DDR5

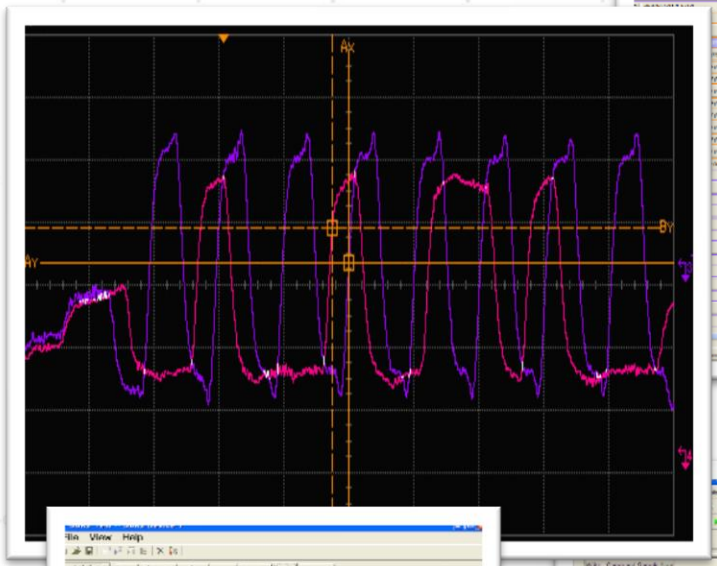
THE IMMINENT CHANGE

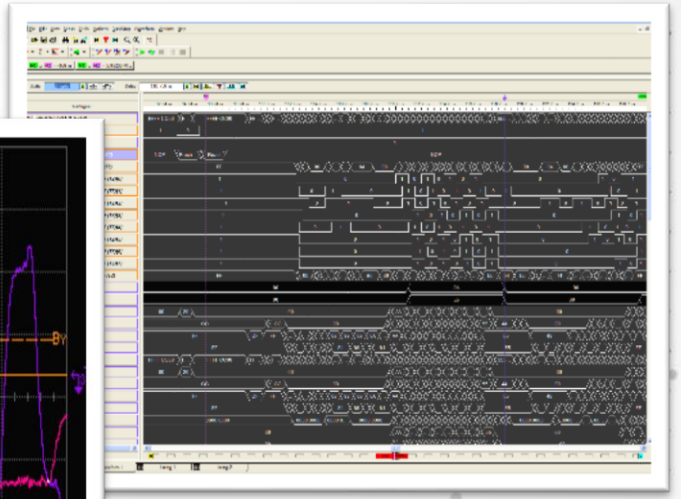
The Good Old Days

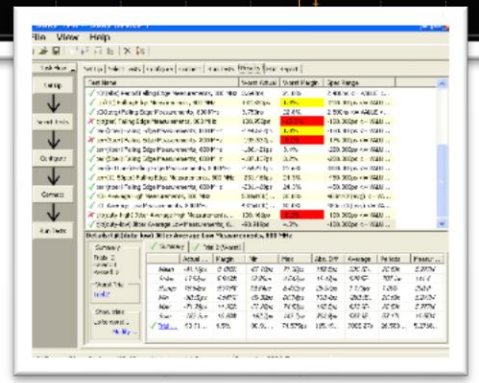
HIGH-SPEED DIGITAL – WAVEFORMS, TIMING, STATE

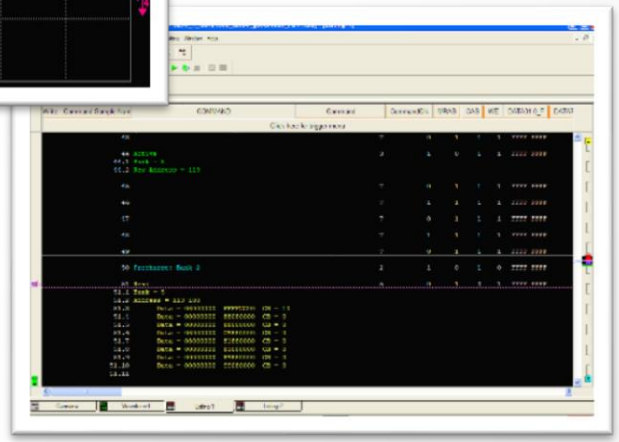












The New Age - DDR Signaling Evolution

DDR6?

"Light Speed"
- Complex modulation?

IQ Threshold

DDR5

"Hyper Speed" - No visible eye
- Pre/De-Emphasis, Impulse response

Impulse Response Threshold

DDR4

"Serial Speed" - Clock often embedded
- Eye Diagrams/Masks
- Error rates, Jitter/Noise

Jitter & Noise Threshold

DDR3

DDR2

DDR

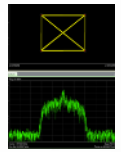
"High Speed" - Transmission lines
- Timing
- Impedance / load curves

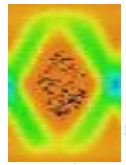
Signal Integrity Threshold

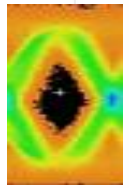
Static RAM

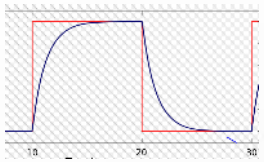
"Low Speed" - Auto place and route
- Fanout
- Capacitance

Signal

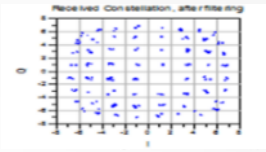


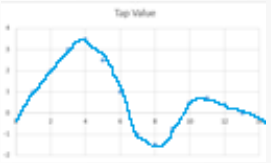


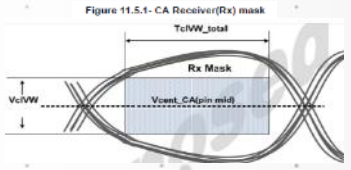


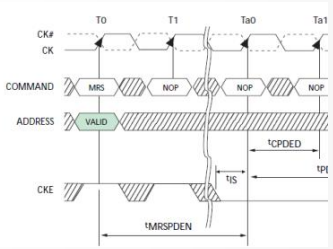


Specification





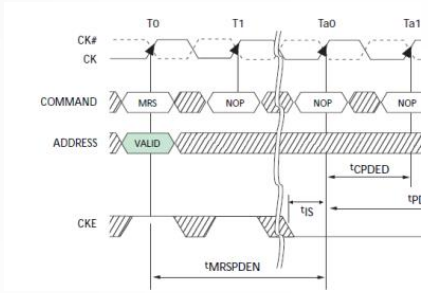


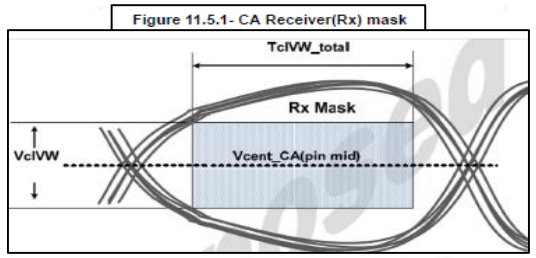


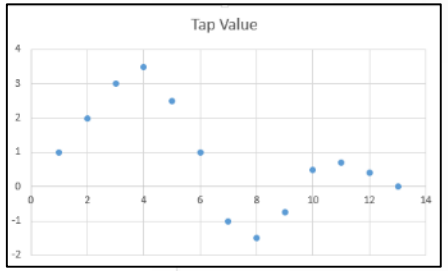
Symbol	Parameter
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)
$V_{OH}(AC)$	AC output high measurement level (for output SR)
$V_{OL}(AC)$	AC output low measurement level (for output SR)

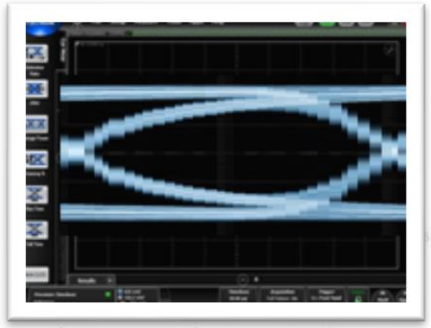
Just When You Thought it Was Safe…

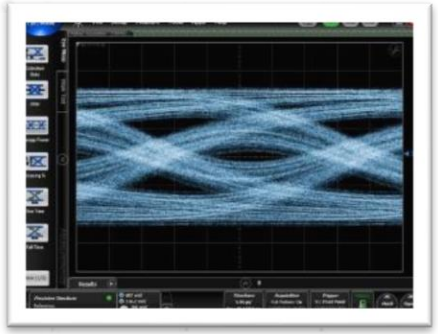
RULES ARE CHANGING WITH EVERY GENERATION- DDR5 IS COMING

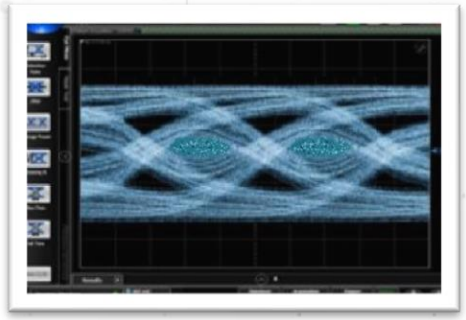












DDR1/2/3

High-Speed Digital

DDR4

Serial Speed

DDR5?

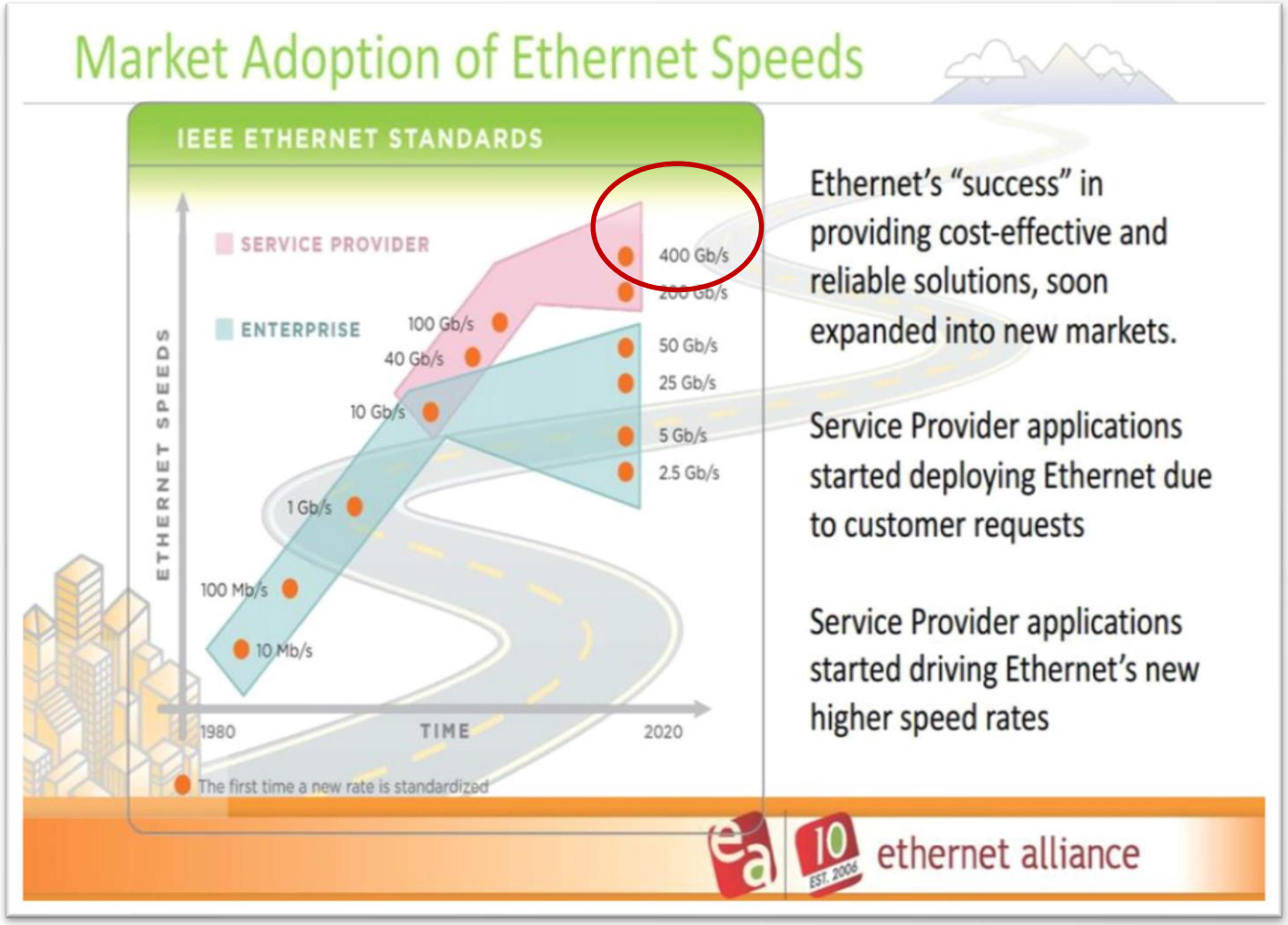
Hyper Speed

PCI Express Gen5

MOVING TO 32 GBPS

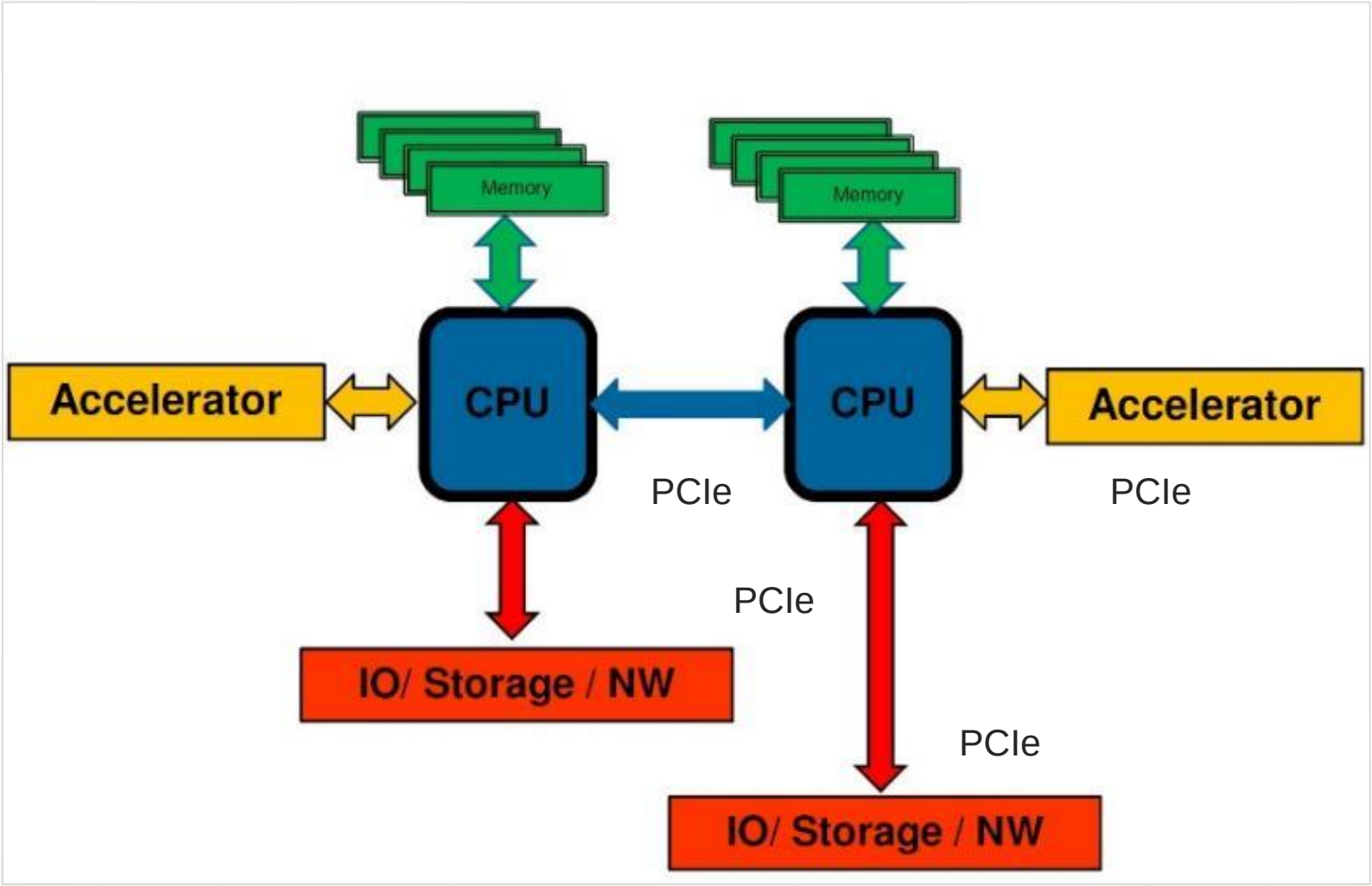
Example of How Data Drives High-Speed Digital PCIe Performance

- High-end networking
  - 400 gigabit Ethernet (GE)
  - Dual 200Gb/s InfiniBand
- Storage Networking
  - NVM Express
  - Big Data
- Increased IC I/O Speeds
  - FPGA
  - ASIC
  - IP



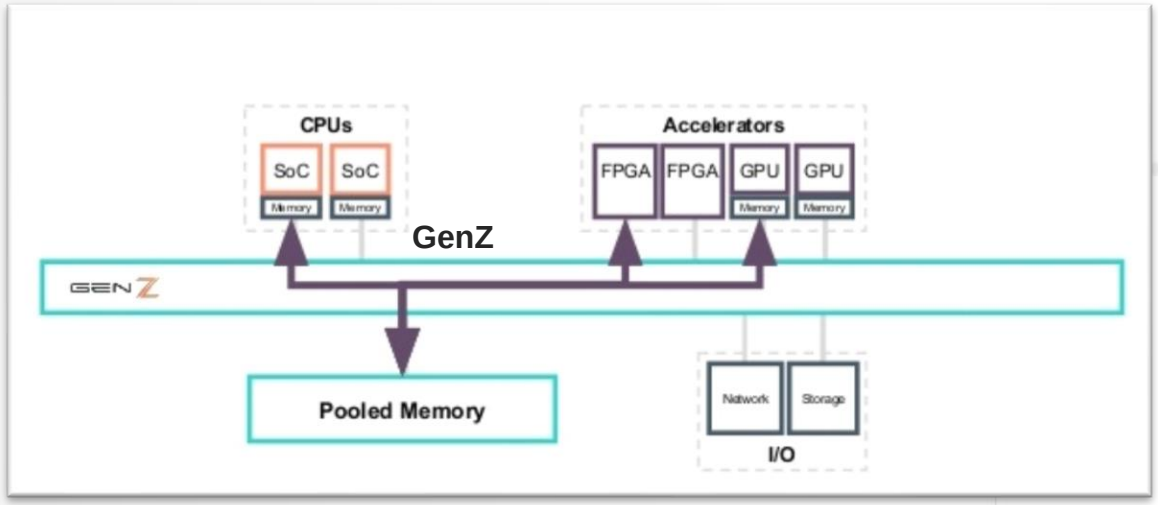
Next-Generation Computer Architecture Examples

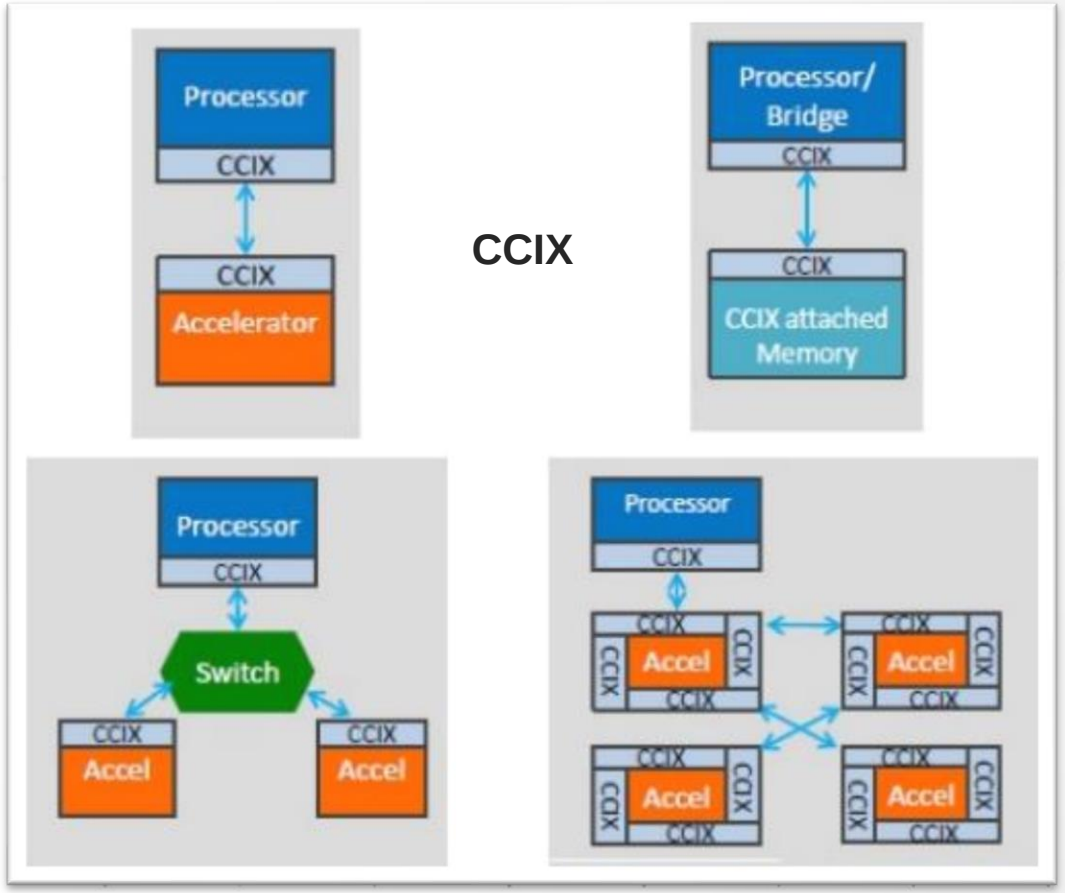
Typical Two CPU Architecture 2017



Next-Generation Computer Architecture Examples

Computer Architecture 2018-2021





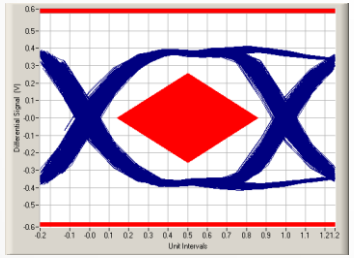
Industry Drives Higher PCIe Bandwidth Requirements

- PCIe 5.0 = 32 Gb/s
- Required for 400GE
  - This equates to 50 GB bidirectionally
  - 16 lanes provides up to 64 GB/s
  - Total full duplex bandwidth = 128 GB/s
- CEM connector for PCIe 5 is planned to be backward compatible with earlier PCIe technologies
- Tentative schedule for spec release in 2019

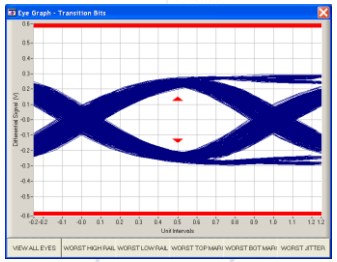
	Raw Bit Rate/Lane	Link BW	BW/Lane	Total x16 Bandwidth
PCIe 1.x	2.5 GT/s	2 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8 Gb/s	~1 GB/s	~32 GB/s
PCIe 4.x	16.0 GT/s	16 Gb/s	~2 GB/s	~64 GB/s
PCIe 5.x	32.0 GT/s	32 Gb/s	~4 GB/s	~128 GB/s

PCI Express Technology Roadmap

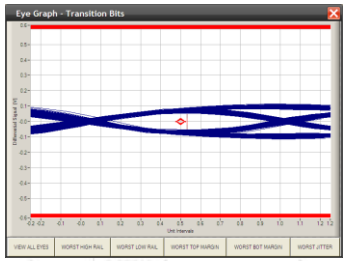
2003
PCIe 1.0 (2.5 GT/s)



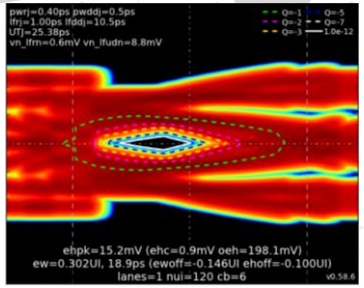
2006
PCIe 2.0 (5 GT/s)



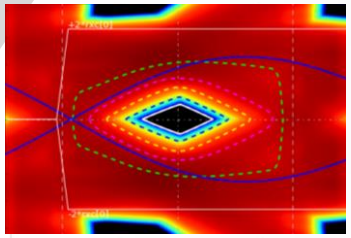
2010
PCIe 3.0 (8 GT/s)



2017
PCIe 4.0 (16 GT/s)



2019
PCIe 5.0 (32 GT/s)



USB 3.2 / 4.0

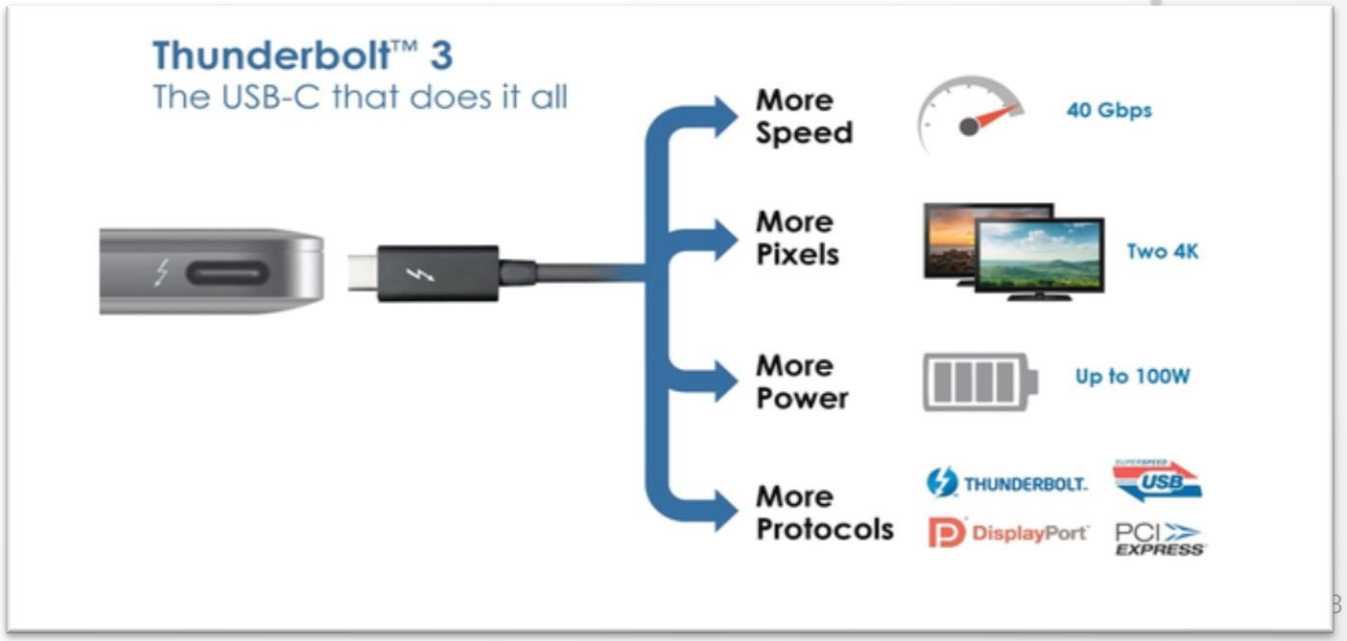
TECHNOLOGIES CONVERGE

Industry Drivers for USB Type-C

- New form-factor
  - Smaller size
  - Reversible plug orientation
  - Reversible cable direction
- Establishes power delivery
  - Scalable charging to 100W
  - Power direction, data direction, Vconn swap
- Enables adoption by other standards
  - ALT (Thunderbolt, DisplayPort, MHL, HDMI) and Accessory Mode (Audio)
  - Future scalability
- Legacy Compatibility
  - USB 2.0, USB 3.1 Gen 1, BC 1.2
  - 5V Vbus start

USB 4.0 Merges into Thunderbolt 3.0

- Announced in 2018
- Uses the Type-C connector
- Channel aggregation: two independent 20 Gb/s links into one logical 40 Gb/s link
- Supports other standards through ALT mode
- Cost competitive vs multi-chip, discrete, mux solutions
- Keysight can help test TX, RX, and Return Loss
- Open standard and integrated in CPU



New Interconnect Standards Emerge

SPECIALIZE IN AREAS WHERE PCIE IS NOT CUSTOMIZED

- OpenCAPI accelerates computing
  - Enables tighter integration of different types of technologies within servers
    - Ex. Advanced memory, accelerators, networking, and storage
  - Moves computing power closer to the data
- Gen-Z targets memory-to-CPU connections
  - Optimized for storage technology
- CCIX increases data throughput
  - Uses the PCIe physical (PHY) layer
  - Changes bus function for increased efficiency and faster speeds

110GHz
bandwidth

Highest ENOB
>4.5 @110GHz

*Enabling Next Gen High Speed Digital Technology for the **5G Era***

First Time Ever

Lowest Noise
<1.0mV rms

256GSa/s
On all 4 channels

Breakthrough Technology

ENABLES 1-TERABIT/S MEASUREMENTS

Introducing UXR-Series Ultra-High Performance Infiniium Oscilloscopes

110 GHz maximum bandwidth with
extremely high signal integrity

- 80, 100, and 110 GHz models (on all channels)
- 256 GSa/s on all channels
- 2G max memory per channel
- 10-bit ADC and superior ENOB with extremely low noise
- Vertical sensitivity from 10 mV to 500 mV per division
- 2 or 4 channels
- Full self-calibration

The Industry's Best Signal Integrity

- **Lowest noise**
  < 1.0 mV rms*
- **Lowest intrinsic jitter**
  < 25 fs rms*
- **Lowest inter-channel jitter**
  < 35 fs rms*
- **Highest ENOB**
  > 4.5 bits @ 110 GHz*
  > 5 bits @ 100 GHz*
- **Flattest frequency response (magnitude and phase)**

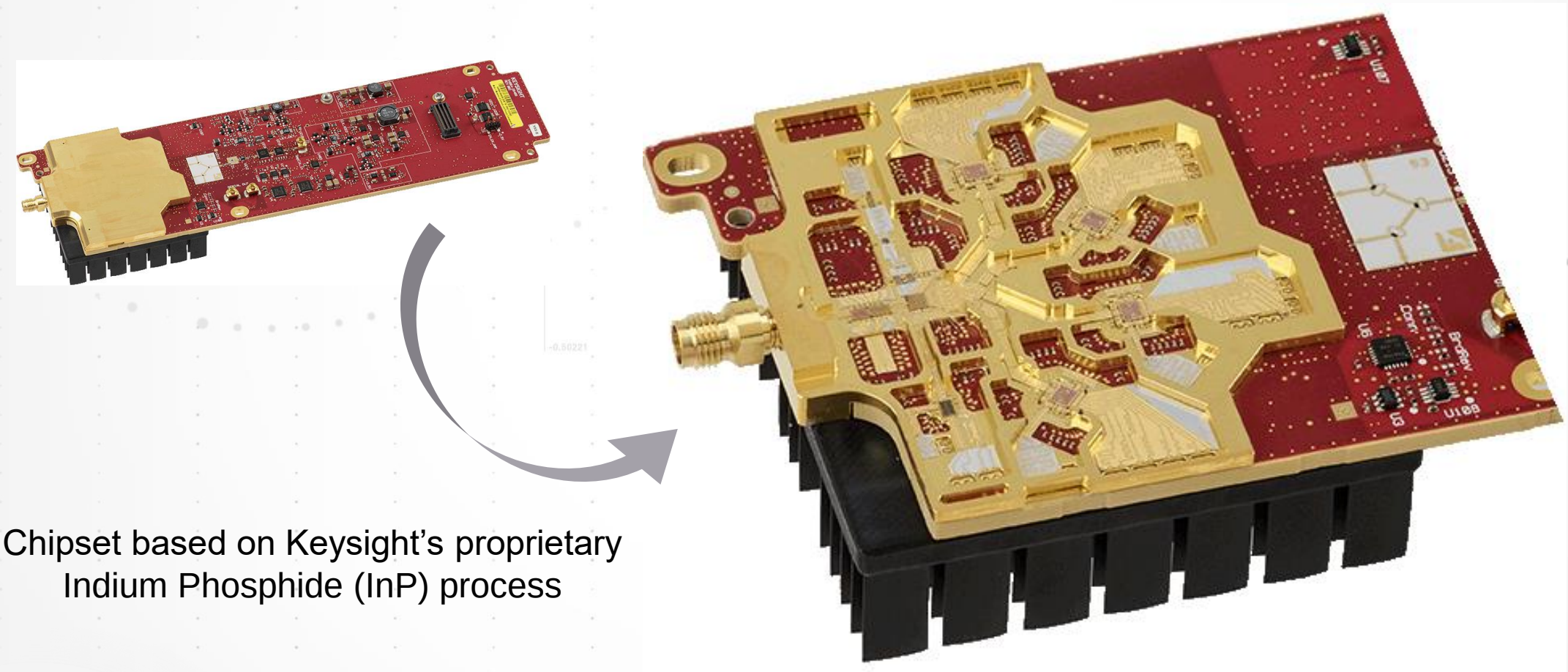
*Typical performance measured on prototype units

KEYSIGHT TECHNOLOGIES

UXR-Series Front-End Multi-Chip Module

THIRD GENERATION FARADAY CAGE TECHNOLOGY

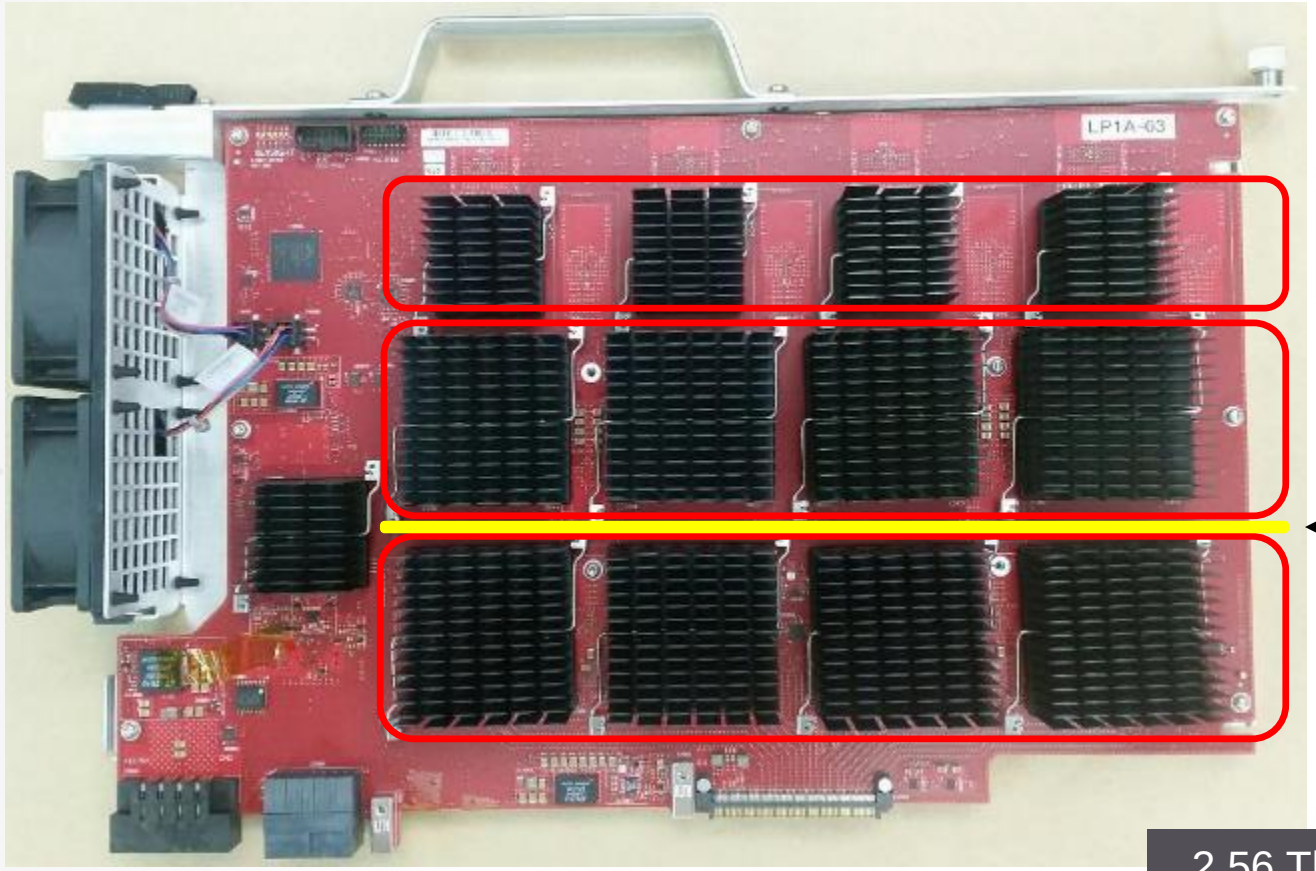
Advanced architecture delivers unprecedented signal fidelity



Chipset based on Keysight's proprietary Indium Phosphide (InP) process

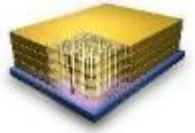
UXR-Series Acquisition System

EACH BOARD ENABLES ONE 110 GHz CHANNEL AT 256 GSa/s



Front-end module connects here

Hybrid Memory Cube



New Data Processor

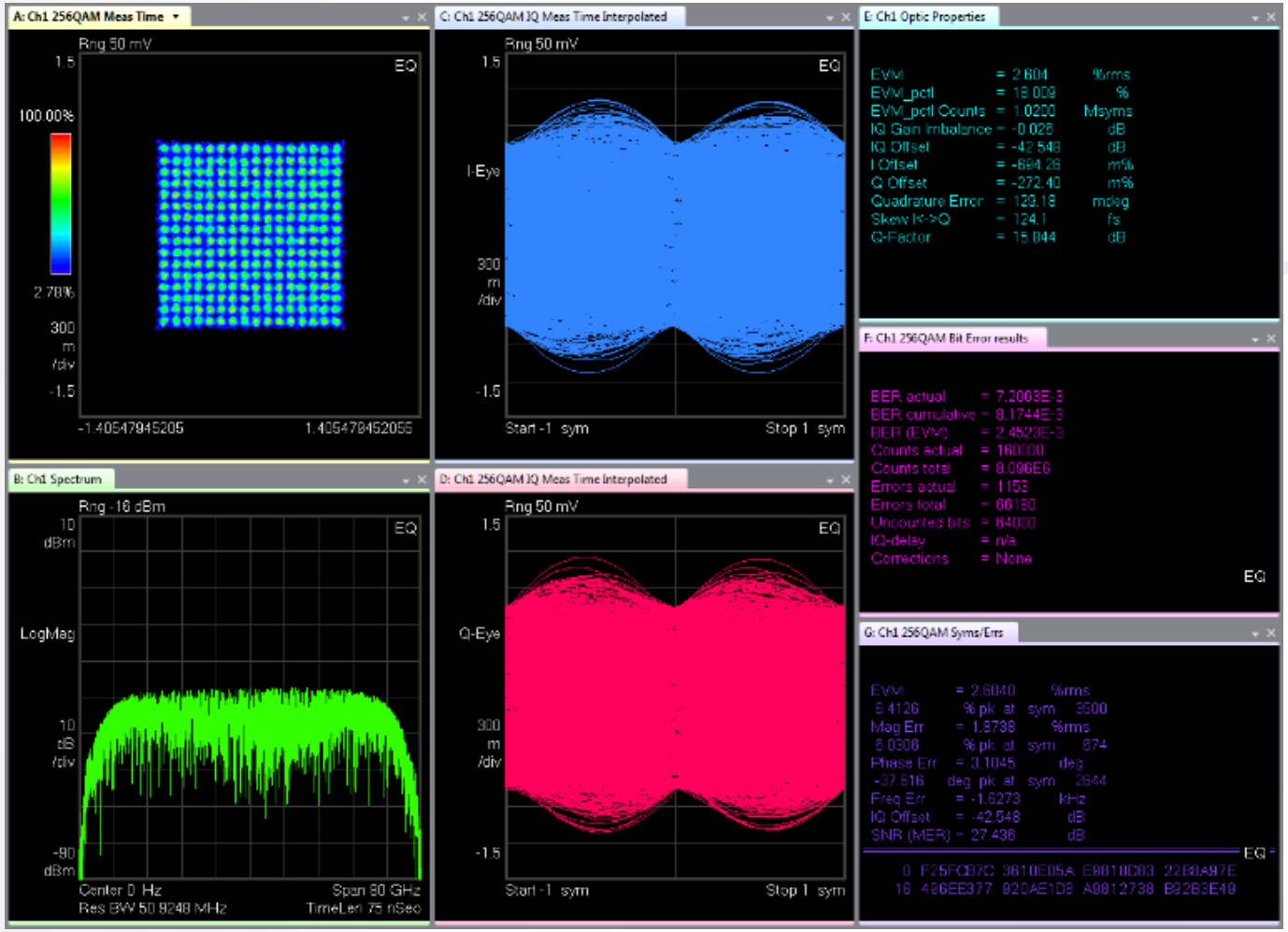
New Custom ADC

2.56 Tb/s at this interface
(320 lanes at 8 Gb/s each)

10 Tb/s
total data
rate across
4 channels

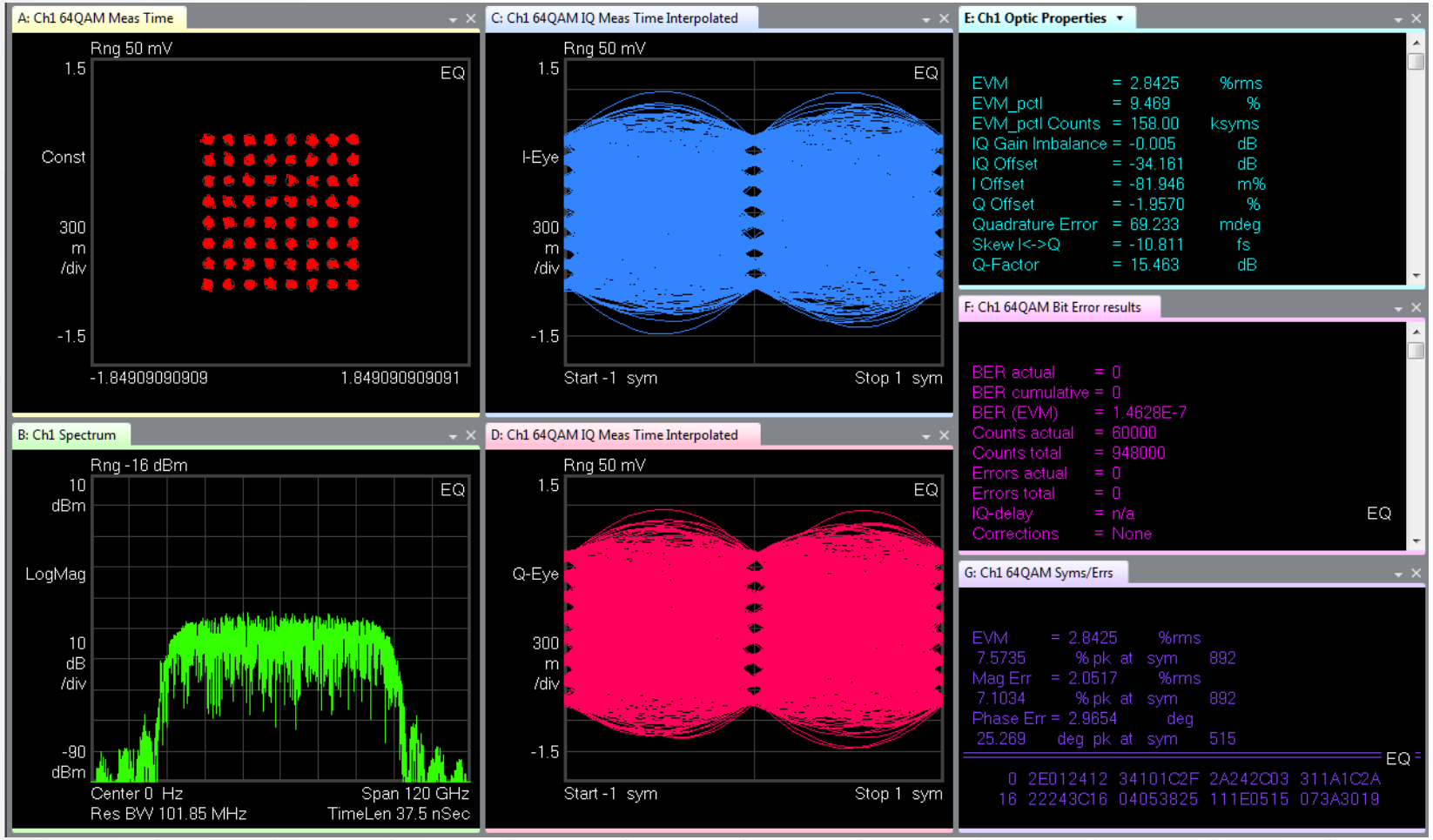
What It Means: You Can Be First and Best

FIRST TIME EVER TO HAVE 2.6% EVM MEASURED FOR 1-TBIT/S EQUIVALENT COHERENT MODULATION



64 Gbaud / 256 QAM, 1-Tbit/s Equivalent Coherent Modulation Measurement	
Infiniium UXR	**2.6% EVM**
Previous Best	Not possible

What It Means: You Can Be First and Best



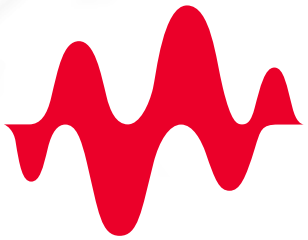
Coherent Modulation 64 Gbaud / 64 QAM (600G+)	
Infiniium UXR	**2.8% EVM**
Previous best	5.4% EVM

What It Means: You Can Be First and Best

40 Gbaud PAM4 Eye		
	Height	Width
Infiniium UXR	**~80 mV**	**~15 ps**
Previous best	~40 mV	~8 ps

Additional Resources

- Learn more about Keysight's High-Speed Digital System Design solutions
- Download the following white papers:
  - Evolution of High-Speed Computing Interfaces: Paving the Way for 400GE in the Data Center
  - The Fast Track to PCIe 5.0: Doubling the Throughput of PCIe 4.0 to 32 GT/s
  - DDR5 - Full Speed Ahead to 400GE: Faster Networking Speeds Require Faster Memory
- Register for Data Center webinars from Keysight



KEYSIGHT
TECHNOLOGIES