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Low power SERDES transceiver for supply-induced jitter sensitivity methodology analysis

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Agenda

- Design Challenge:
  - Jitter-aware target impedance of power delivery network approach
  - Design challenge for Low power Transmitter
    - CLK path : DCC & CLK tree buffer and its side effect
    - Data path : Pre-driver & CML IO
  - Design challenge for Receiver
    - Recover very loss signal. Needs re-driver.
  - Design challenge for PLL
    - Ring VCO
- Solution to Design Challenge
  - Solution to CLK path : Active & passive method
  - Solution to Data path: Current modulation skill
  - Solution to recover very loss signal for receiver : Multi-stage CTLE&VGA cascade design
- Summary

Design Challenge:

Jitter-aware target impedance of power delivery network approach

$$Z(f) = \frac{Vdd * (\pm 1\% \sim \pm 10\%)(V)}{I(f)} \rightarrow \text{[Conventional target impedance formula]}$$

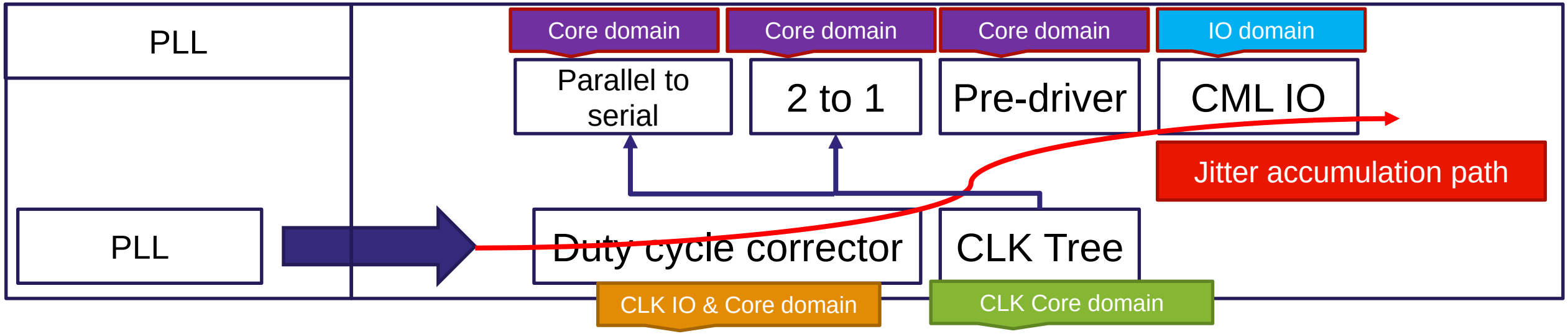
$$Z(f) = \frac{\text{Budget Jitter induced by supply}}{\text{Sensitivity}(f) * 1 * I(f)} \rightarrow \text{[jitter aware target impedance formula]}$$

Introduction :

To complete the PDN analysis, it is necessary to determine the target impedance of the overall power network. However conventional target impedance only shows on-chip supply noise value information. Conventional target impedance does not show any jitter-related information. With jitter sensitivity extraction of IO circuit, it is to enable accurate jitter-aware target impedance calculation

Design Challenge:

Jitter-accumulation of Low Power Transmitter Data & CLK path approach



General SERDES transmitter architecture is serial-to-parallel converter and is sensitivity to the supply noise. The serdes transmitter has many power domains which have different influences in the jitter-sensitivity contribution. The jitter sensitivity is dependent of each block silicon characterization and combined with Data/CLK path.

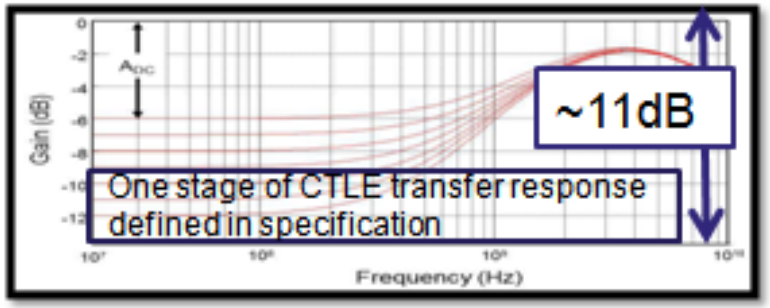
Design Challenge:

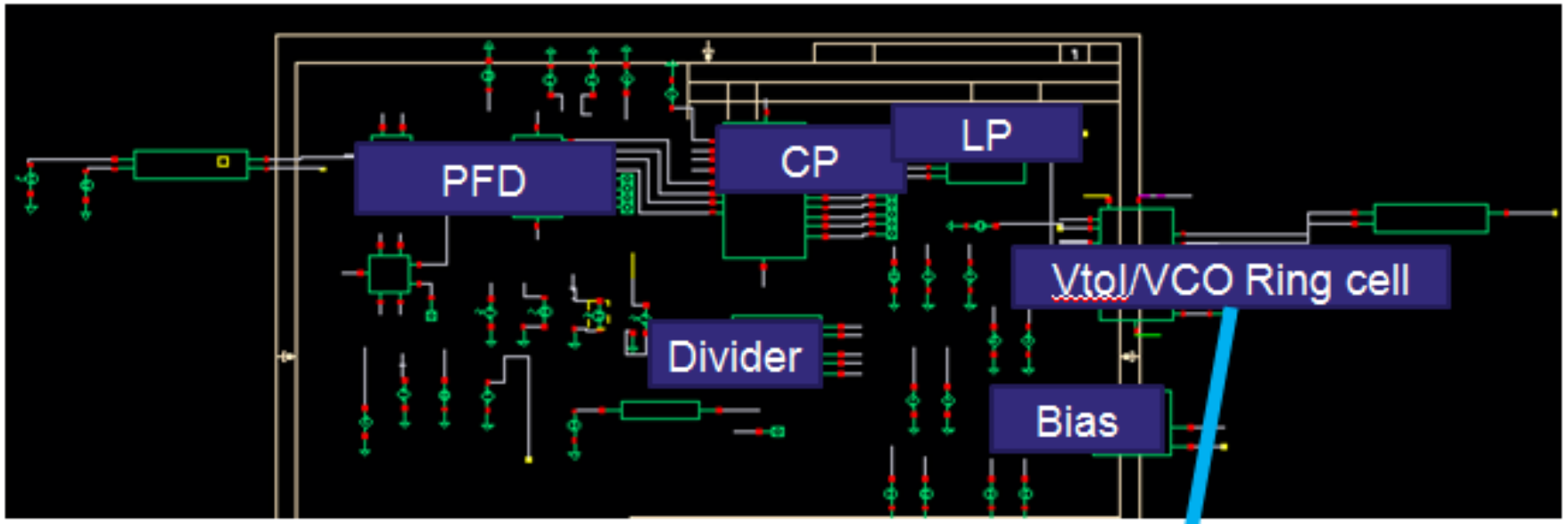
Challenge to PLL design approach

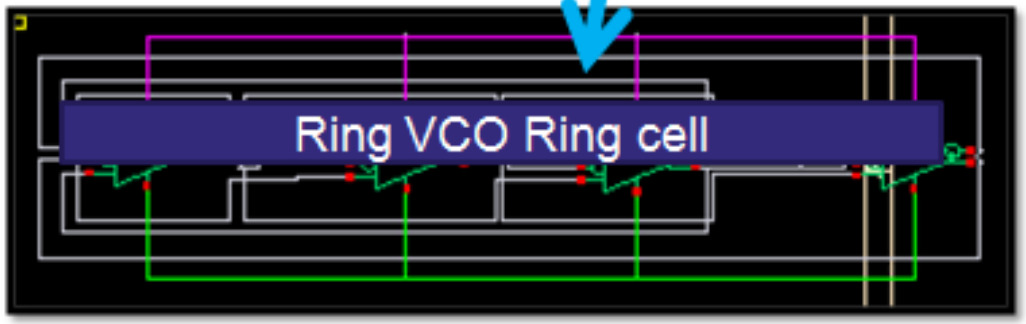
Receiver analog frond-end

Termination | One stage of CTLE

IO & Core domain



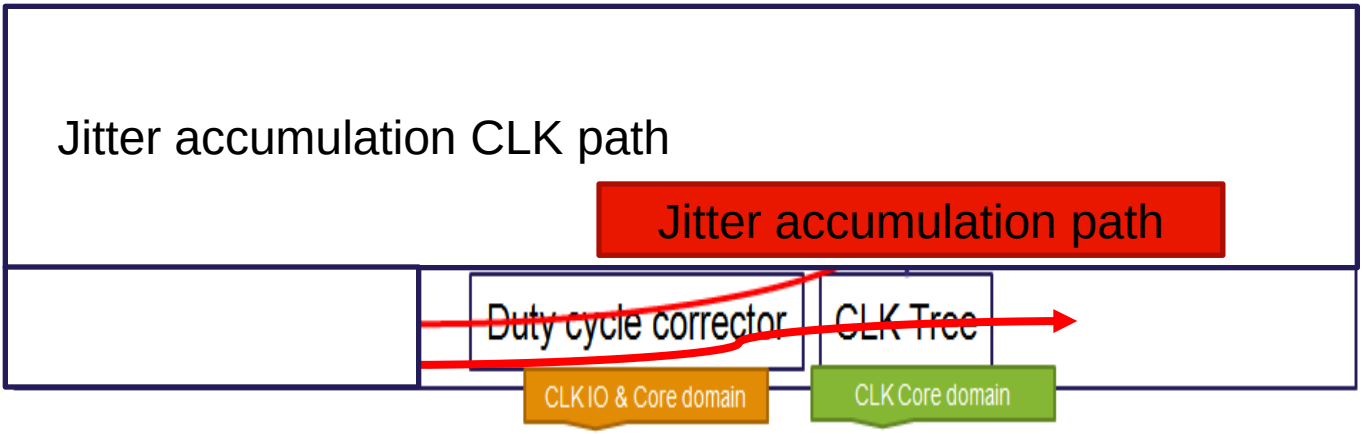


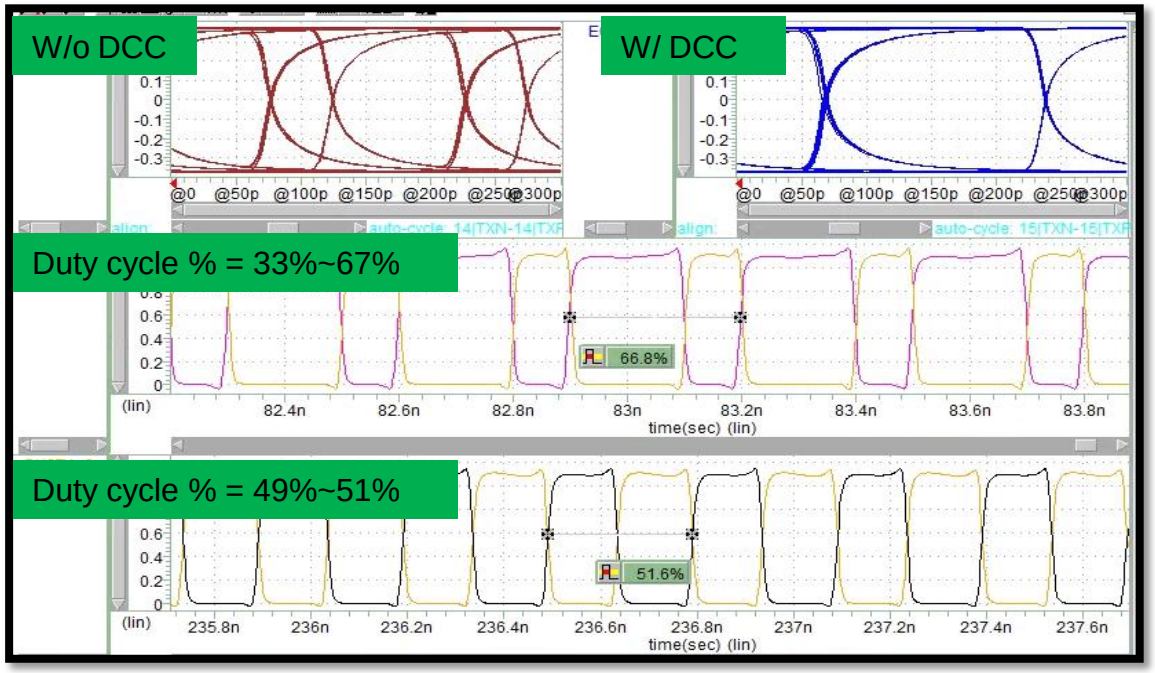


For design cost, small area, large tuning range, multi-phase clock generation and lower power effectiveness, a Ring VCO based PLL is first considered to use in application design. To optimize a supply-induced phase noise performance of PLL architecture, PSIJ of PLL architecture is analyzed to provide the robust solution to performance.

Design Challenge:

Challenge to Jitter-accumulation of Low Power Transmitter CLK path approach





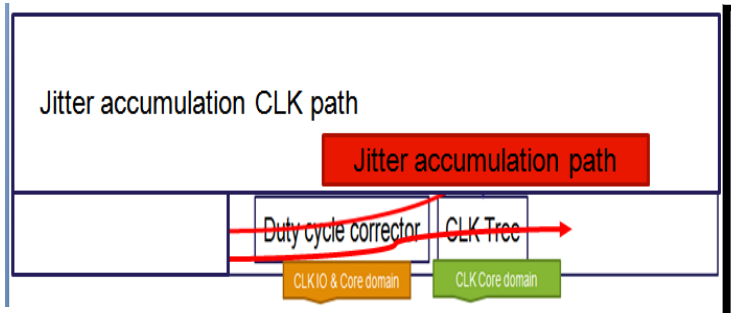
Duty cycle corrector function and its side effect:

Duty cycle corrector is commonly used to adjust the duty cycle of clock signals from PLL, to improve the signal quality of the clock signal and to ensure a ~50% duty cycle that maintain the high speed signal performance.

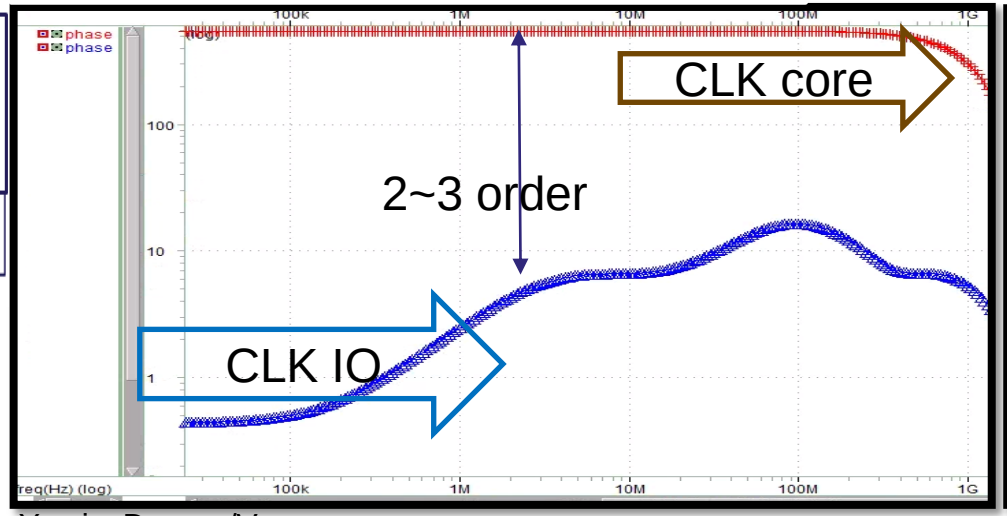
However its supply-induced jitter sensitivity is increased, and the performance is affected.

Design Challenge:

Challenge to Jitter-accumulation of Low Power Transmitter CLK path approach

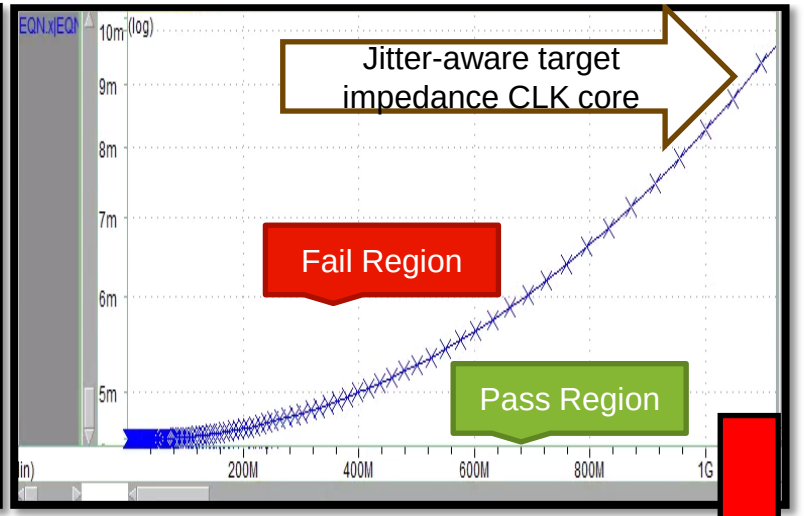


Supply-induced jitter sensitivity Plot



Y axis: Degree/V
X axis: Frequency

Jitter-aware target impedance Plot



Y axis: Impedance(ohm)
X axis: Frequency

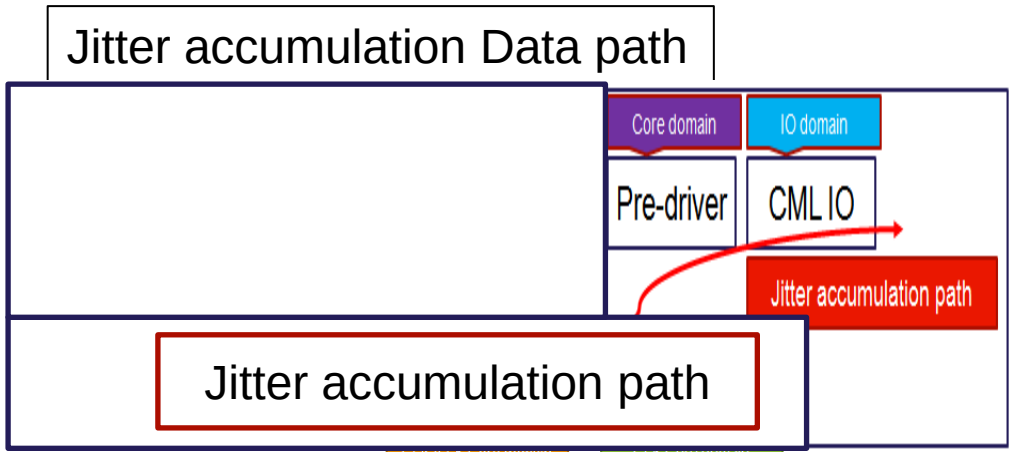
Need a lot of resource of on-chip decap, Package and PCB BOM cost to meet the PDN target impedance requirement. Reach to the goal with difficulty

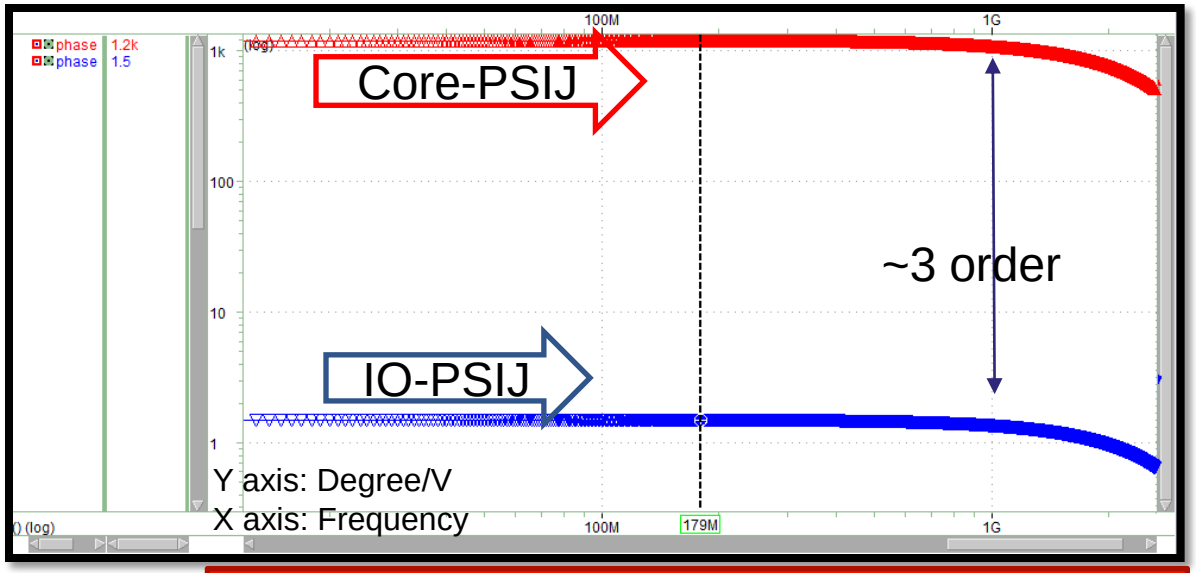
CLK path supply induced jitter analysis :

Merge Core power and CLK core power in Die-package bump region that causes the very strict requirement of target impedance because core power supply many blocks which is power hungry such as clock data recovery/receiver AFE/Transmitter logics and pre-drivers.

Design Challenge:

Challenge to Jitter-accumulation of Low Power Transmitter Data approach





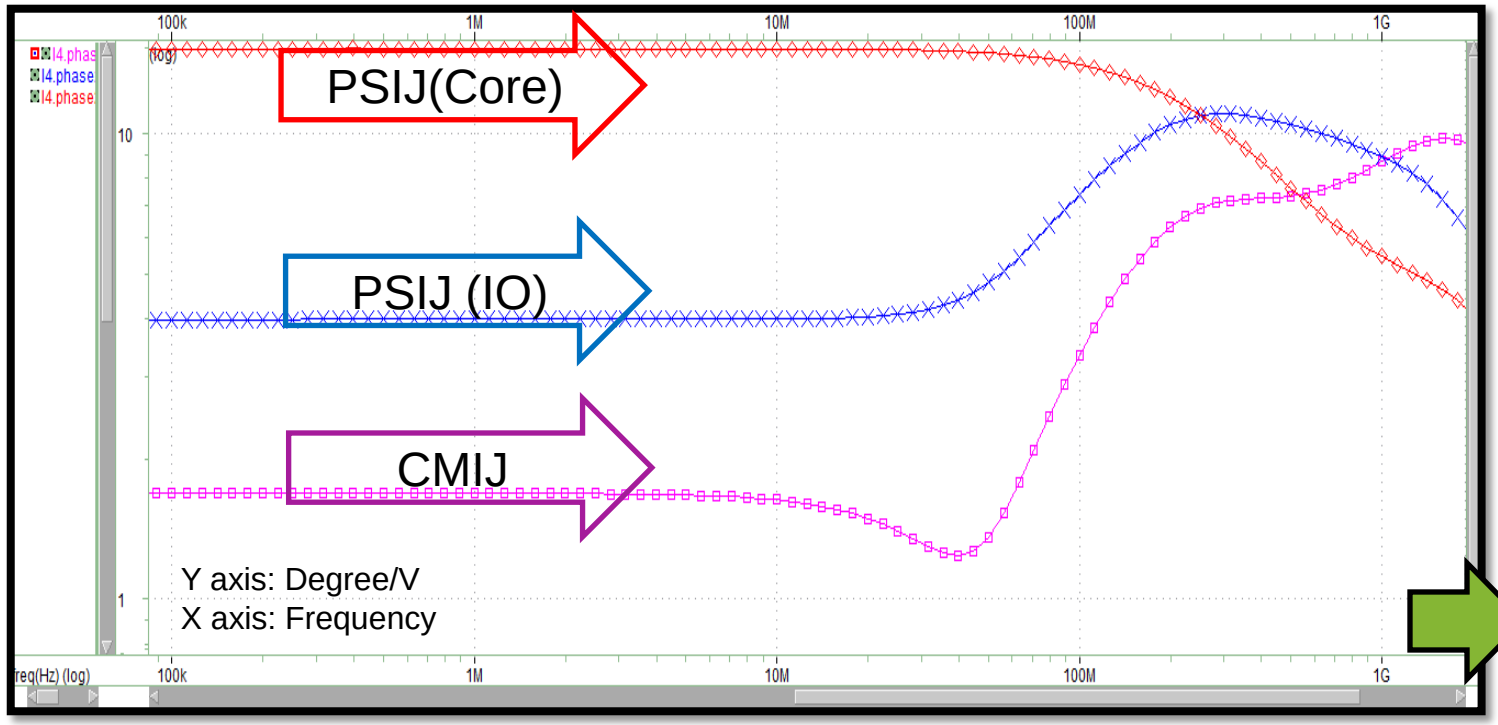
Need a lot of resource of on-chip decap, Package and PCB BOM cost to meet the Core power target impedance requirement. Reach to the goal with difficulty

Introduction :

For optimizing this jitter performance induced by supply noise, characterizing the jitter distribution between different power domains is the key to resource allocation of PDN design. The simulation shows that if an internal data path is consist of voltage mode pre-driver, it is sensitive to core power supply noise.

Design Challenge:

Power supply & common mode noise induced jitter of Receiver AFE approach



Signal Common mode noise induced jitter →CMIJ

Power supply noise induced jitter →PSIJ

Reach to the PDN Z goal with No difficulty

Due to the complexity of CM/Power supply noise generated from non-linear power supply noise/non-symmetry Packaging/PCB trace, the effect of common mode noise is analyzed independently to investigate the CM noise induced jitter inside receiver.

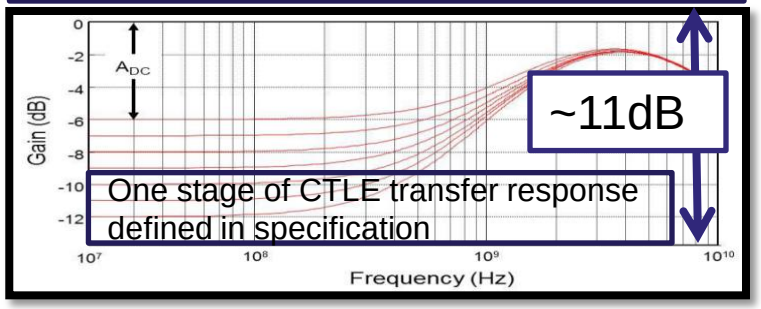
Design Challenge:

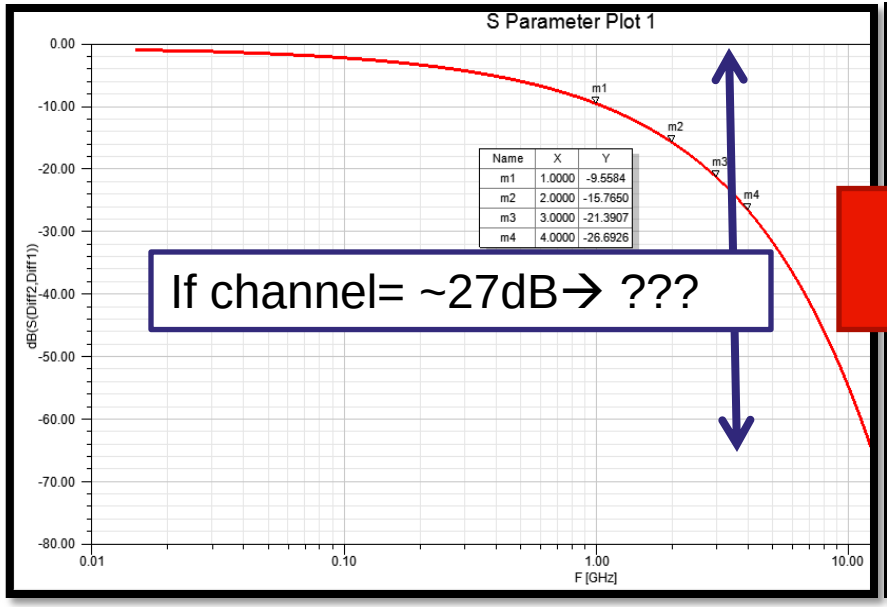
Challenge to Receiver AFE recover ability approach

Receiver analog frond-end

Termination | One stage of CTLE

IO & Core domain

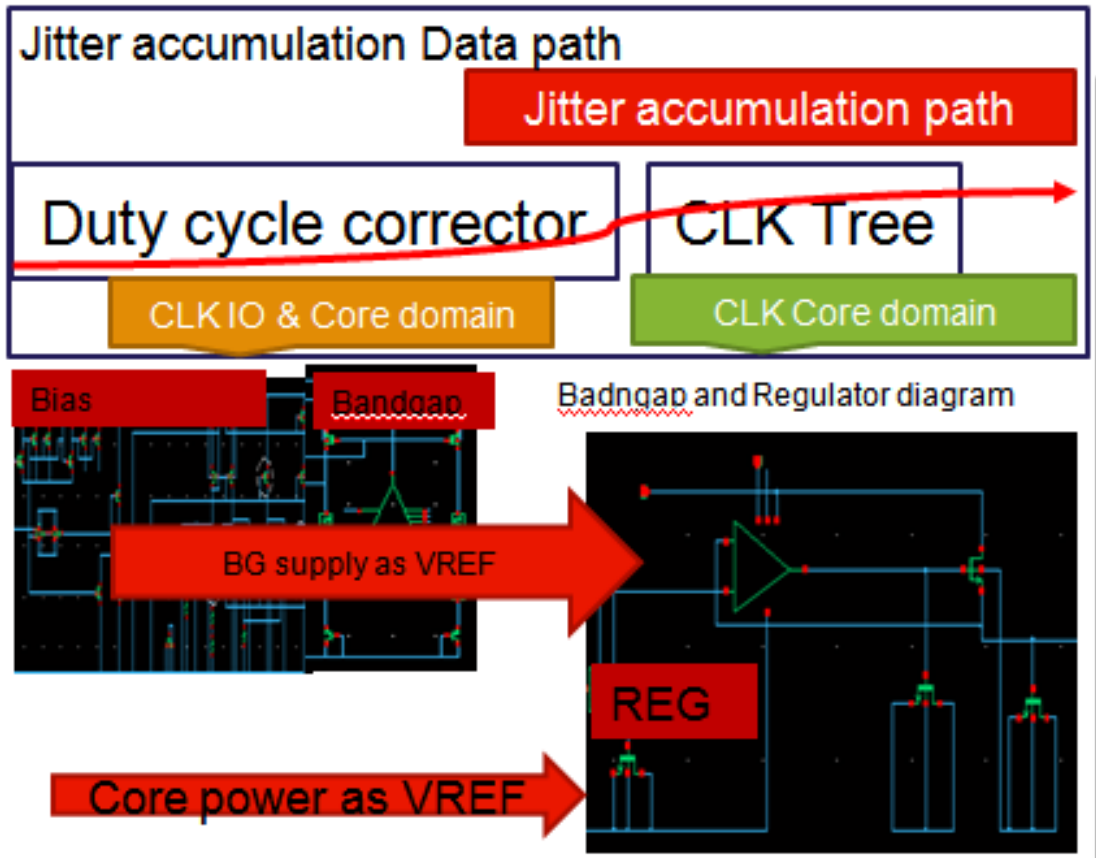


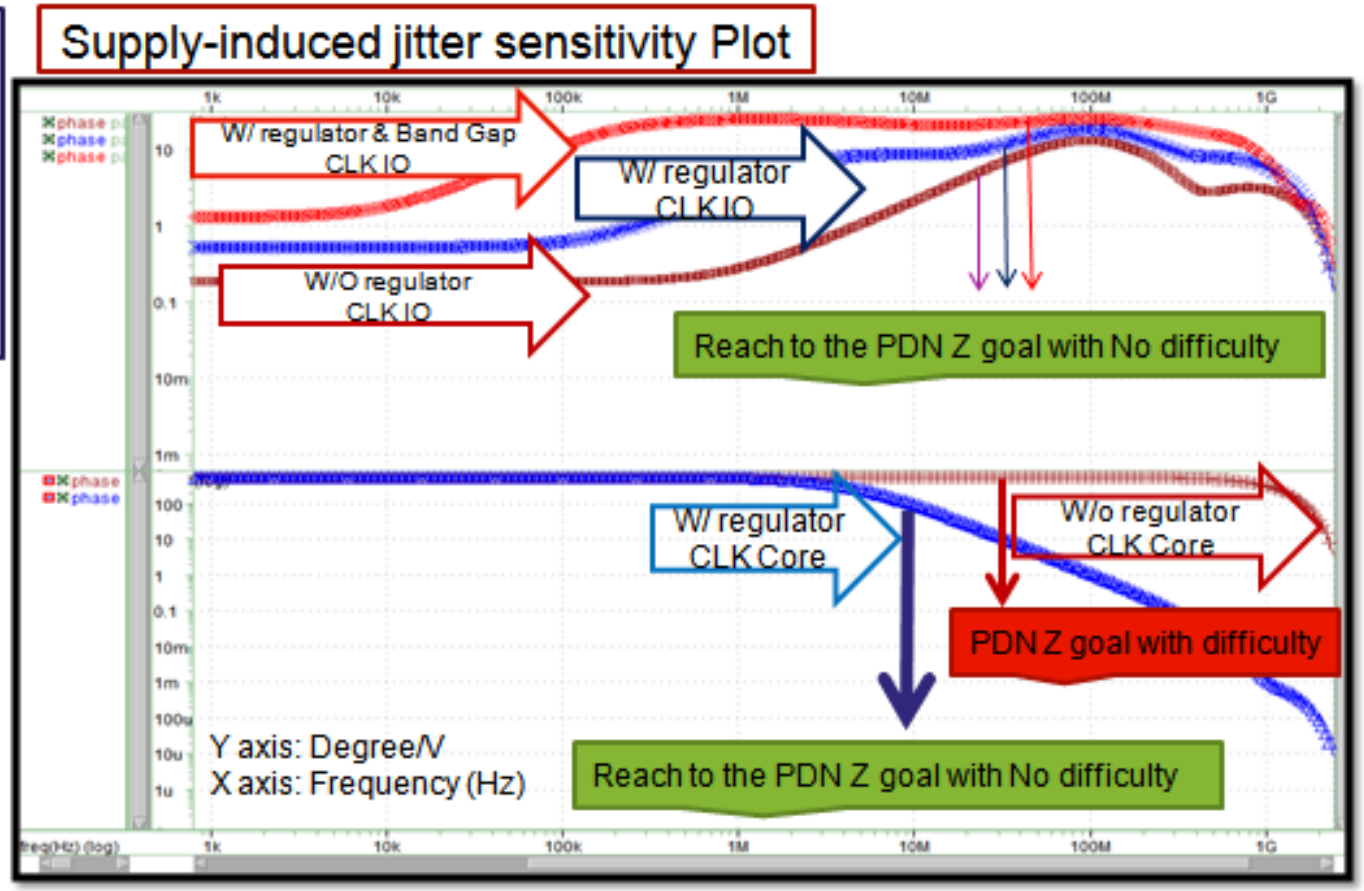


The received signal, however, suffers from seriously inter-symbol interference (ISI) due to channel imperfections making the signal integrity face big challenges. Re-driver/Re-timer requirement is always strong demand but brings more power consumption, cost and form factor.

Design Challenge:

Solution-1 to Jitter-accumulation of Transmitter CLK path approach: Regulator skill





Solution:

Regulator filters the high frequency noise from VREF power and forces REG output to follow VREF. The jitter sensitivity of CLK core power is reduced ~2 order above ~5MHz and the jitter sensitivity of CLK IO is increased 1 order under ~1MHz. So the target impedance is relaxed by ~2 order above ~5MHz.

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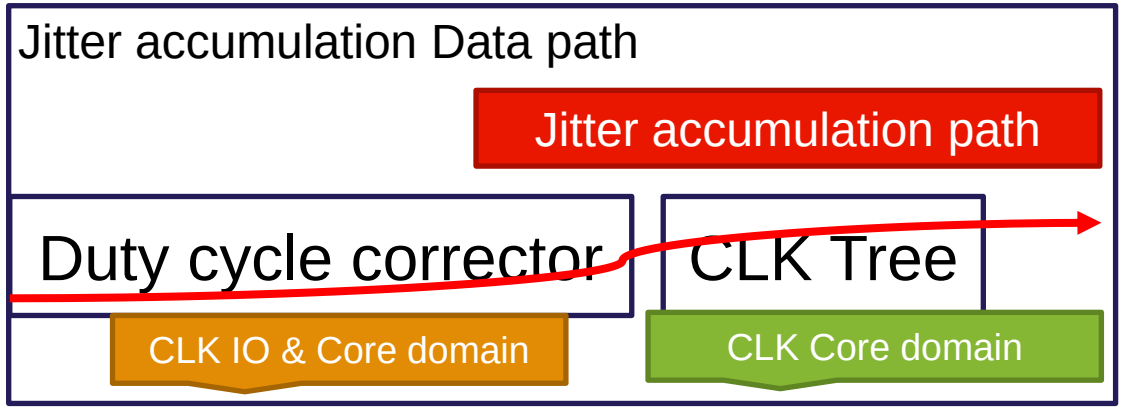
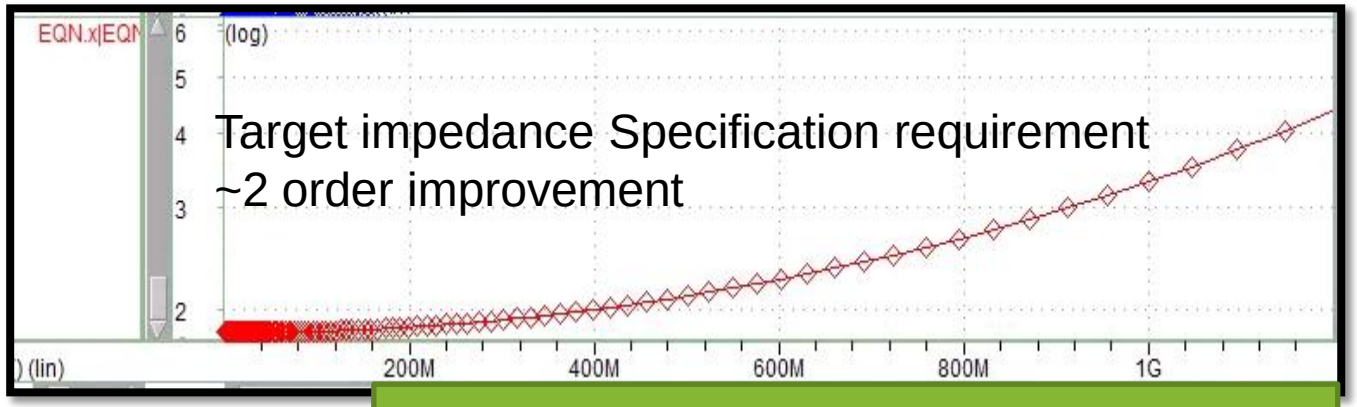
Design Challenge:

Solution-2 to Jitter-accumulation of Transmitter CLK path approach: Separated coupling layout skill similar to on-chip regulator behavior

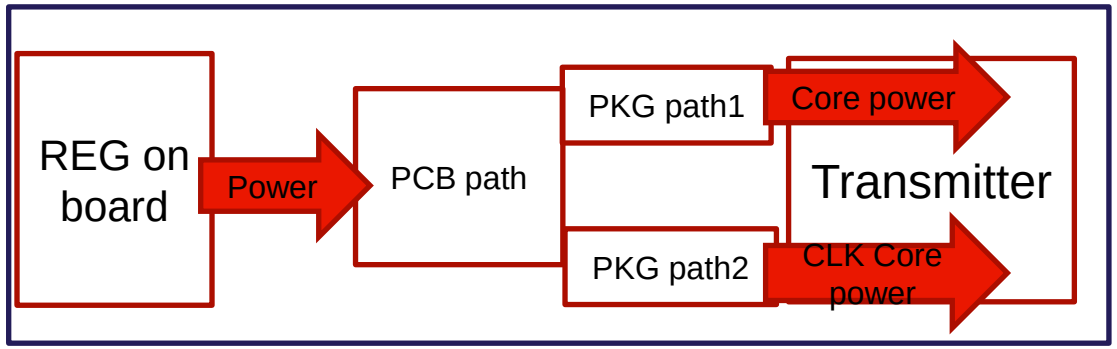


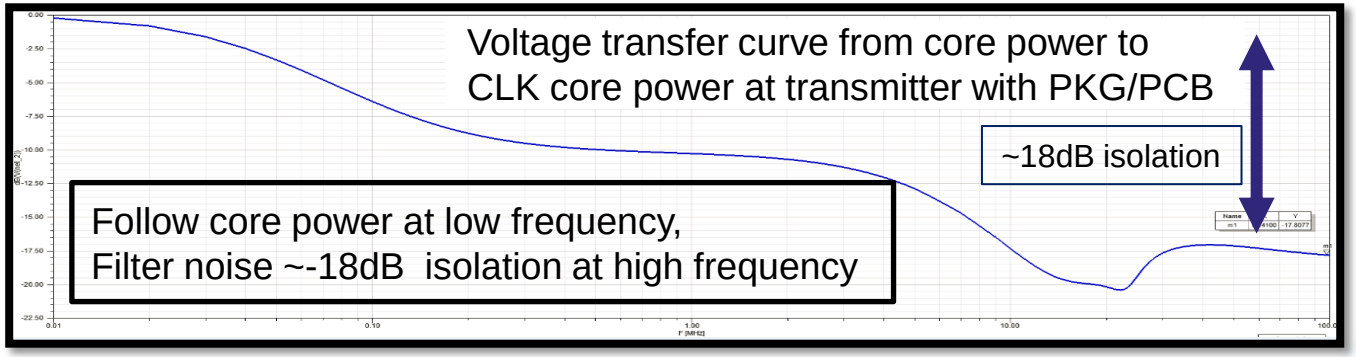
Jitter-aware target impedance Plot



Y axis: Impedance(ohm)
X axis: Frequency

Reach to the PDN Z goal with No difficulty





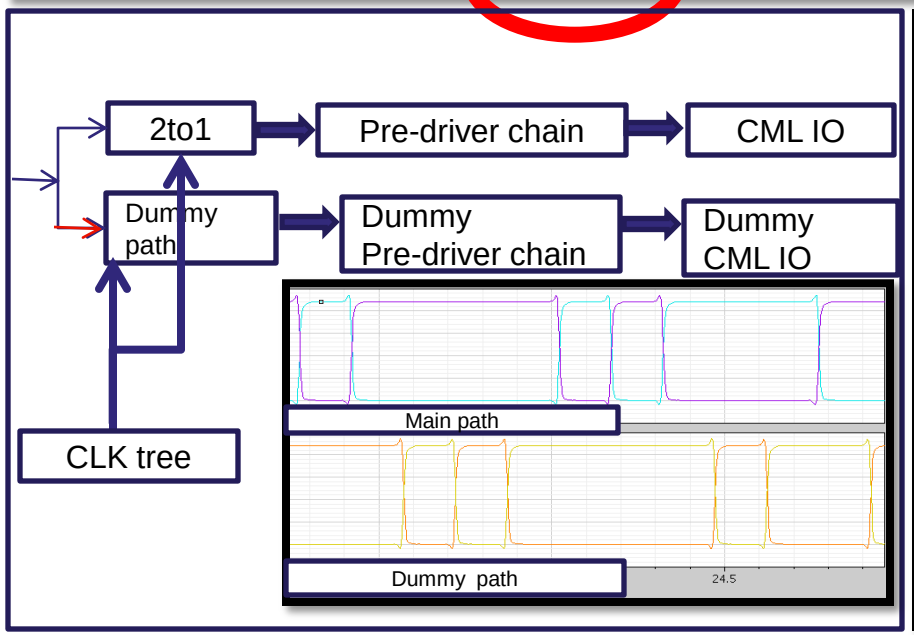
Solution :

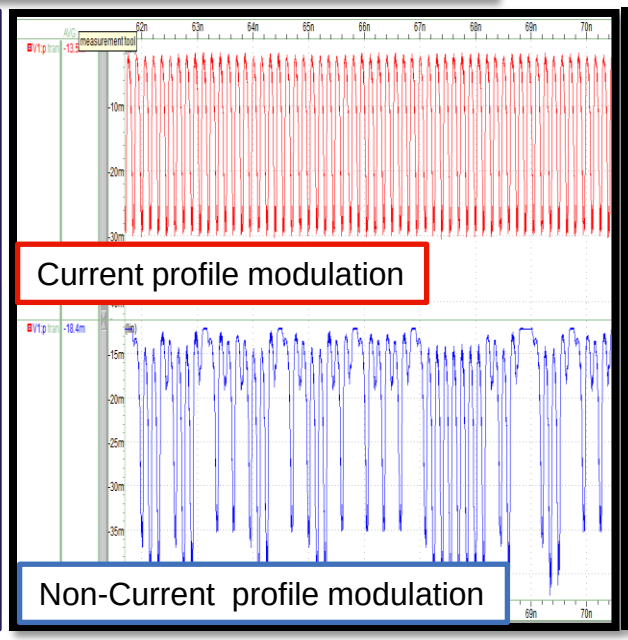
Separate Core power and CLK core power in Die-package and merged together under board-level BGA region. Specification requirement is relaxed by ~2 order and likely to meet. Separated layout skill is similar to on-chip regulator behavior and without any additional power consumption.

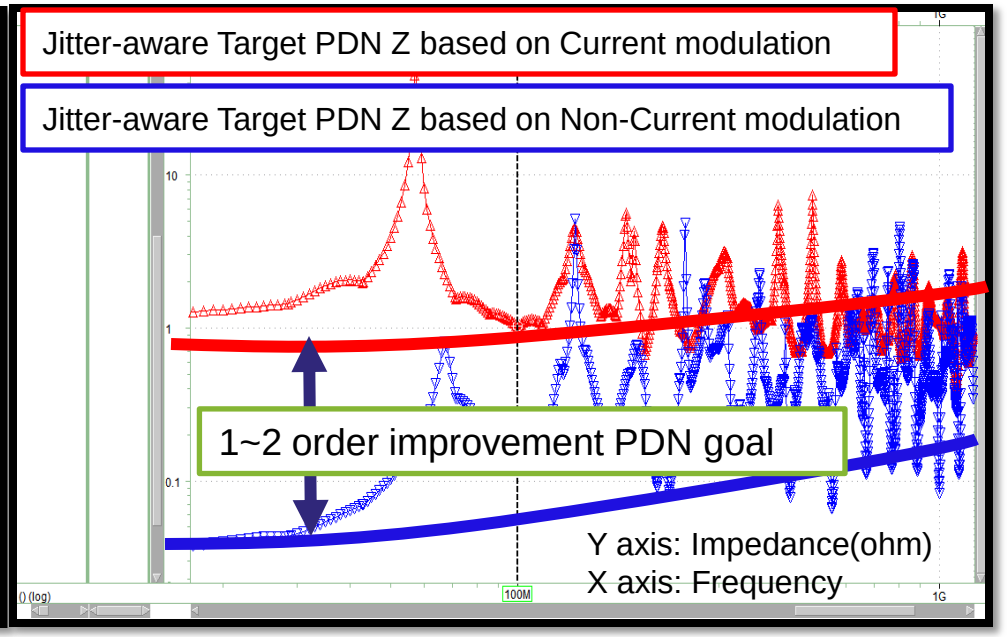
Design Challenge:

Solution to Jitter-accumulation of Transmitter Data approach

$$Z(f) = \frac{\text{Budget Jitter induced by supply}}{\text{Sensitivity}(f) * \Delta I * I(f)} \rightarrow \text{[jitter aware target impedance formula]}$$







Current profile modulation skill is applied in analog skill to analyze the improvement of target impedance of Core power domain PDN. Specification requirement is relaxed by 1~2 order.

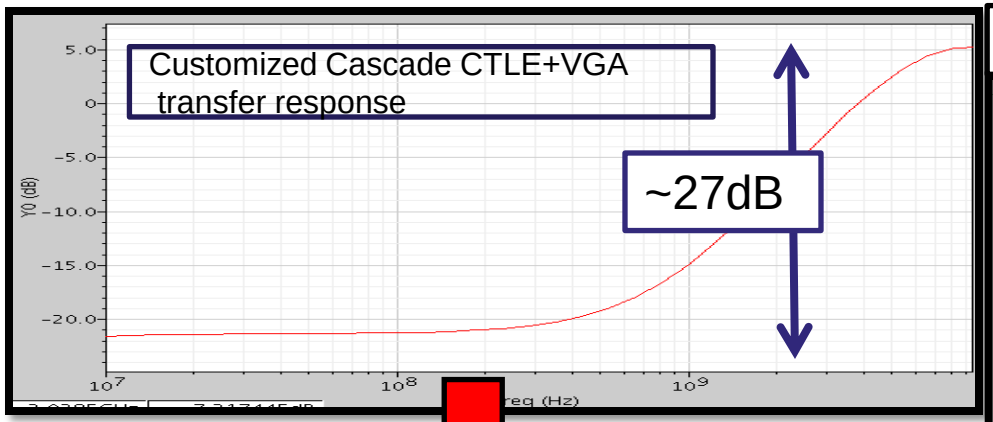
Design Challenge:

Solution to recover very loss signal for receiver approach: Multi-stage CTLE&VGA cascade design

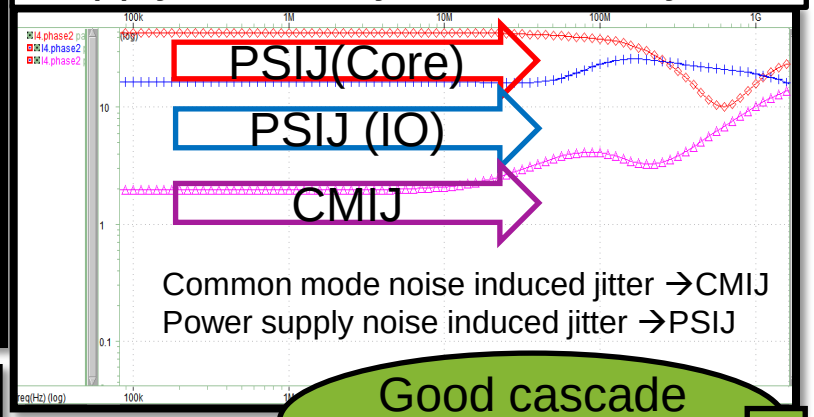
Receiver Analog frond-end

Signal path

Customized Cascade CTLE+VGA

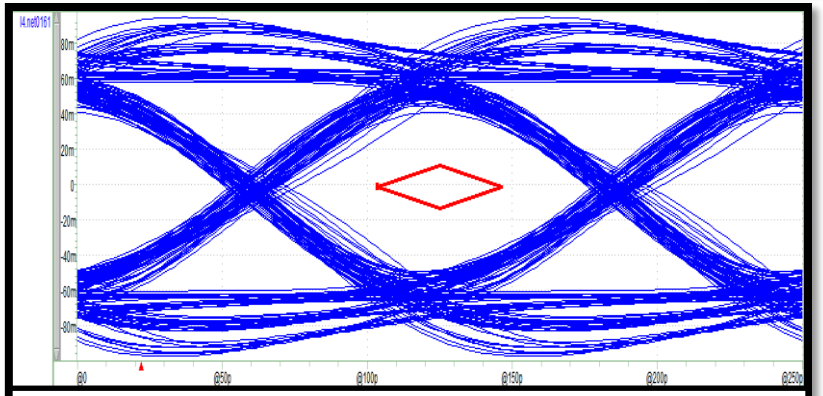


Supply-induced jitter sensitivity Plot

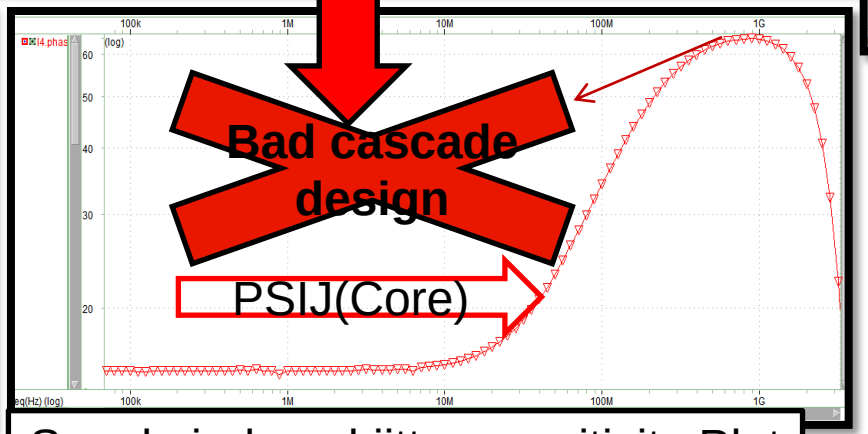


Common mode noise induced jitter →CMIJ
Power supply noise induced jitter →PSIJ

Good cascade design



PASS 27dB channel with RX AFE enable only



Supply-induced jitter sensitivity Plot

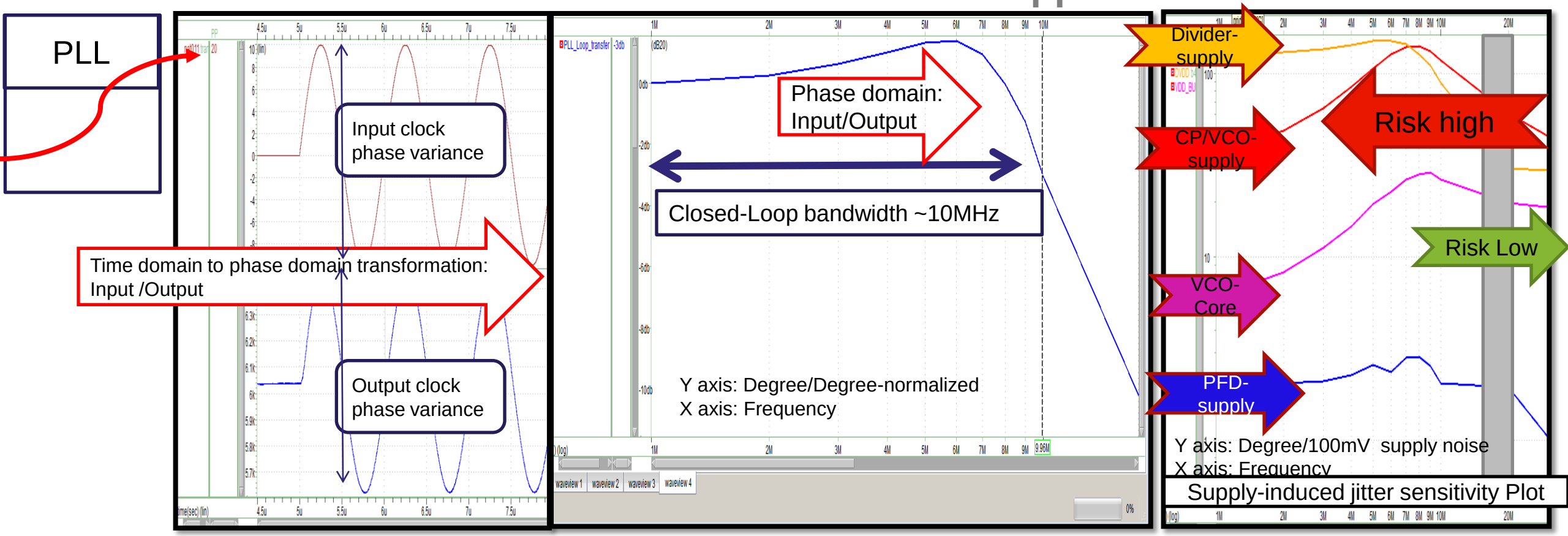
Jitter Sensitivity slightly increases.
Reach to the PDN goal with No difficulty

Solution :

Customized AFE Receiver overcomes the serious loss channel and bring a lot of advantages in hardware field application. Combined with transmitter feed forward equalizer (Customized ~9dB), 36dB channel loss is expected to pass the requirement.

Design Challenge:

Solution to Jitter-accumulation of Low Power PLL approach



To optimize a supply-induced phase noise performance of PLL architecture, PSIJ of PLL architecture is analyzed to provide the robust solution to performance.

1. Divider supply-induced jitter dominates the performance before ~7MHz.
2. VCO cell supply-induced jitter dominates the performance after ~7MHz.
3. PLL supply-induced jitter performance is low pass filter behavior. → Robust de-coupling/isolation design and regulator type selection at board stage at frequency before PLL closed-loop frequency X 2.

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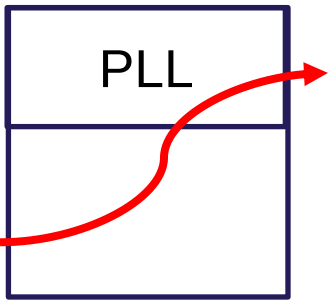
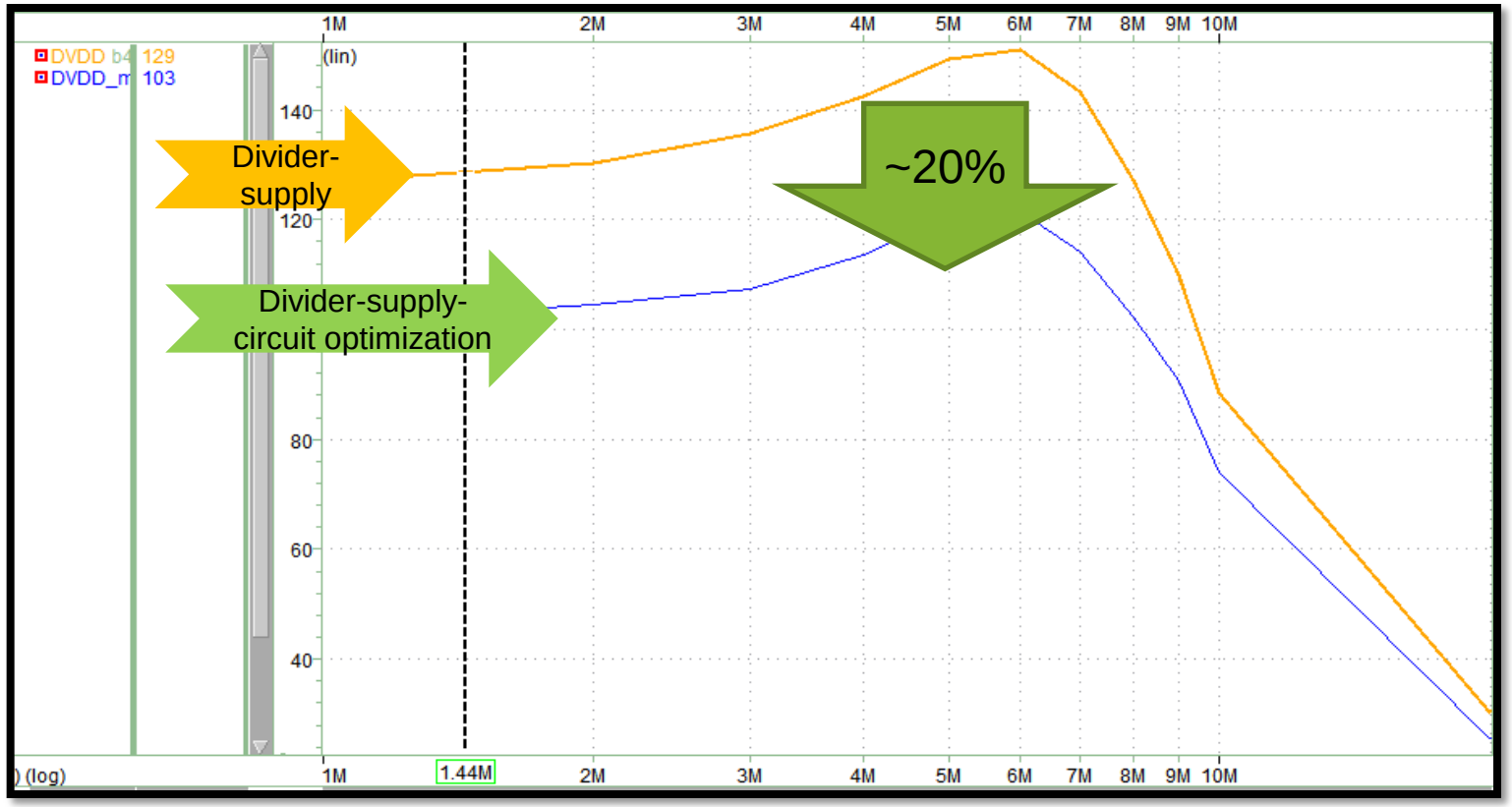
Design Challenge:

Solution to Jitter-accumulation of Low Power PLL approach





To optimize a supply-induced phase noise performance of PLL architecture, PSIJ of PLL architecture is analyzed to provide the robust solution to performance.

1. Optimize the divider of analog circuit design to achieve the optimal performance by ~20%.

Summary

- Advanced Jitter-sensitivity analysis in analog field is applied for low power transceiver and provide three kinds of skills to solve the jitter performance improvement based on PDN analysis.
- It gives the in-depth SI/PI insight into analog design field and optimization/achieving on silicon success.