How different FPGA firmware options enable digitizer platforms to address and facilitate multiple applications

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- Digitizer definition and application
- Firmware FWDAQ for standard acquisition and triggering
- Firmware FWATD for advanced noise filtering
- Firmware FWPD for pulse data capture and analysis
- Development Kit for open FPGA access
- Conclusion

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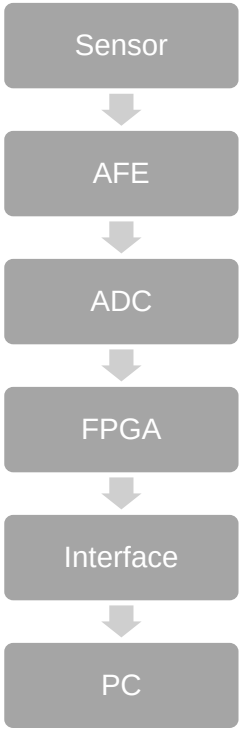
What is a digitizer ?



- A digitizer translates sensor signals to digital data
- The core is an analog-to-digital converter (ADC)
- Signal conditioning is done in the analog front-end (AFE)
- The field-programmable gate array (FPGA) is used for control and real-time signal processing
- Supports multiple interface types / form factors for easy integration in different type of systems
- High data transfer rate to the host PC (CPU or GPU)
- A digitizer can be used both as stand-alone or as an embedded sub-module
- Synchronization capabilities enable multi-channel systems

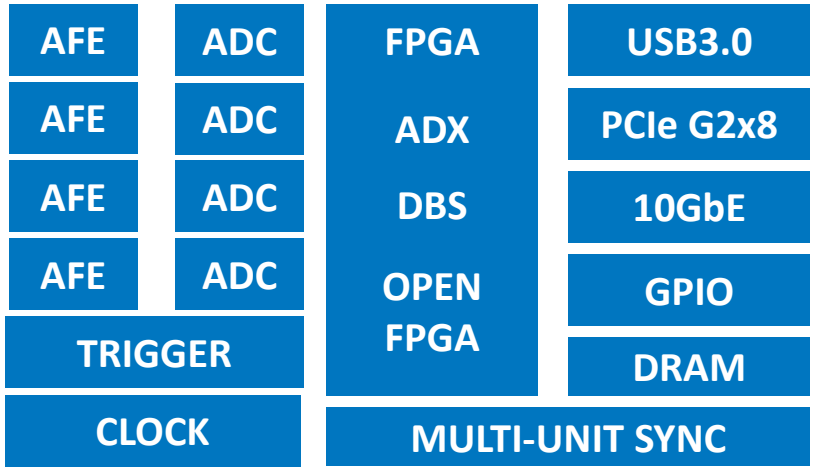
ADQ14 Series Digitizer

Hardware

- 1, 2 or 4 analog channels with 14 bits vertical resolution
- Sampling speed of 500, 1000 or 2000MSps
- DC and AC coupling capable with 1.2GHz of analog bandwidth
- Variable gain option for DC coupling board
- 2 Gbyte on-board data memory
- High-precision trigger (resolution:125ps; jitter:25ps)
- General-purpose I/O (GPIO) and custom GPIO expansion option
- Multi-channel & unit synchronization support
- Multiple form factor: USB3.0, PCIe, PXIe, 10GbE, MTCA.4
- 3-year warranty

Firmware and Software

- SDK supporting multiple environments
- Windows and Linux support
- Firmware options for pulse detection, averaging and software defined radio
- DBS IP for baseline stabilization
- Open Xilinx Kintex 7 K325T FPGA
- FPGA firmware development kit optional
- GPU peer-to-peer streaming with PCIe Gen3x8



Application areas

Time-of-flight

- Mass Spectrometry
- Swept-Source OCT
- Distributed fiber-optical sensing
- Airborne LIDAR
- Analytical Instrumentation
- Quantum Physics

High Frequency

- EPR/NMR Spectroscopy
- RADAR
- Software Defined Radio
- RF Recording
- L-band direct sampling

General purpose instrument

- Semiconductor Functional Test
- Wafer Inspection
- Automated Test Equipment
- Test and Measurement

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FWDAQ – Introduction

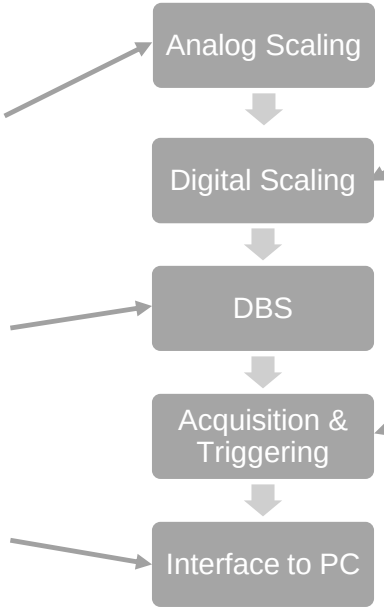
- FWDAQ is the standard Teledyne SP Devices firmware provided with any digitizer.
- It is a general purpose firmware allowing standard acquisition and triggering.
- FWDAQ support digital signal conditioning and specific noise optimization IP.
- Multiple triggering options are possible including external trigger and level trigger.
- When no specific processing is necessary, FWDAQ is a very flexible solution

FDAQ – Firmware Overview

Analog scaling allow optimization of the input signal to closely match the full scale of the digitizer

DBS – Digital Baseline Stabilization optimizes baseline level up to 22b precision

Multiple interface option are supported including USB3.0, PCIe, PXIe, 10GbEth and MTCA.4



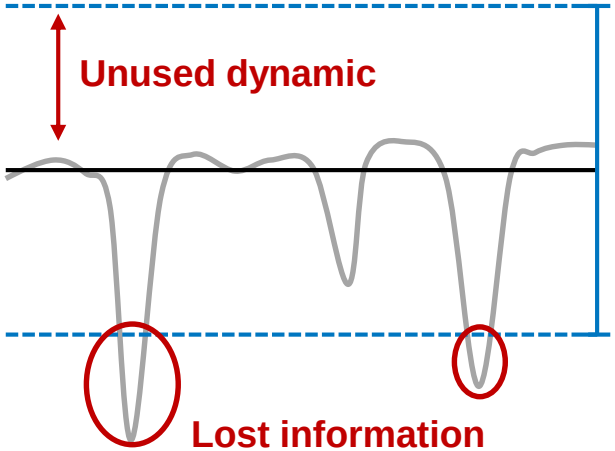
Digital offset and gain control allows optimize the digitial data (e.g for later processing)

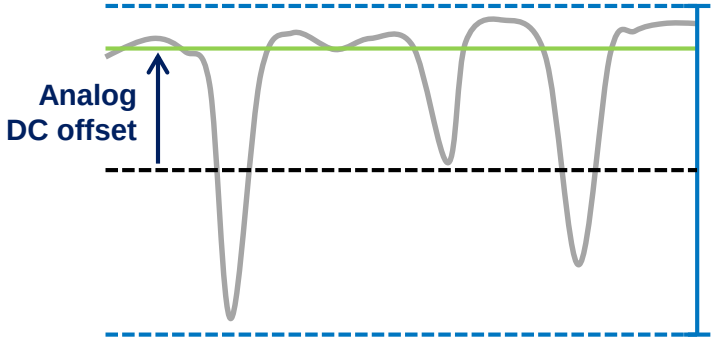
Acquisition are performed on an trigger event that can be software controlled, external or generated by threshold on the input data

FWDAQ – Analog Scaling

Analog scaling to optimize the dynamic range of the input signal, effectively doubling the dynamic range for uni-polar pulses

- Analog Scaling
- Digital Scaling
- DBS
- Acquisition & Triggering
- Interface to PC



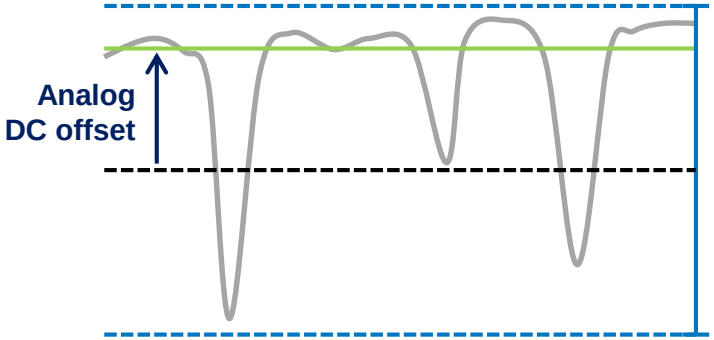


Fully used dynamic
No loss of information

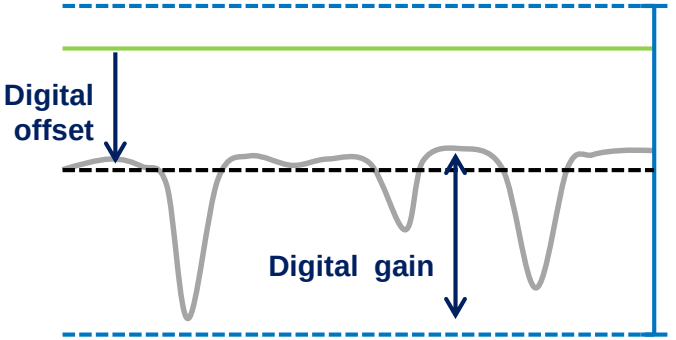
FWDAQ – Digital Scaling

Digital scaling with gain and offset control to simplify application processing

- Analog Scaling
- Digital Scaling
- DBS
- Acquisition & Triggering
- Interface to PC



Fully used dynamic
No loss of information



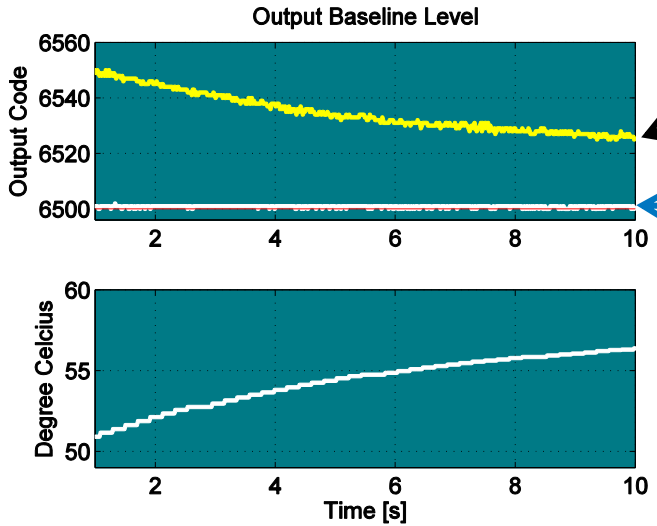
Fully used dynamic
No loss of information
Digital data ready for processing

FWDAQ – Digital Baseline Stabilization

- Analog Scaling
- Digital Scaling
- **DBS**
- Acquisition & Triggering
- Interface to PC

Digital Baseline Stabilizer tracks slow and periodic baseline variation

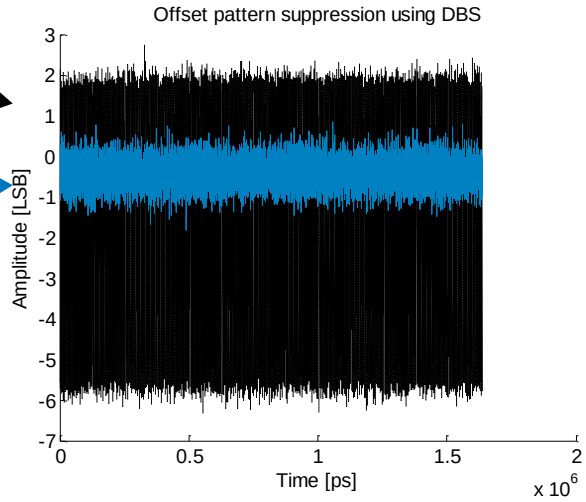
- Temperature variation
- Component aging
- Pattern noise from ADC due to interleaving



DBS benefit versus temperature variation

DBS disabled

DBS enabled



DBS benefit versus pattern noise

FWDAQ – Acquisition and Triggering

Analog Scaling

Digital Scaling

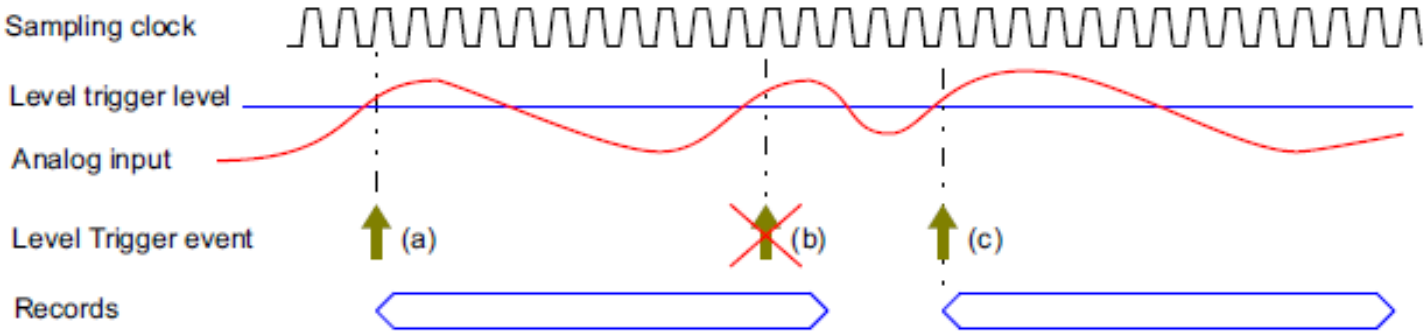
DBS

Acquisition & Triggering

Interface to PC

Acquisition with multiple triggering options

- Software trigger – trigger generated from the PC
- Internal trigger – trigger generated in the FPGA (configured by the PC)
- External trigger – trigger provided as an exernal input
- Level trigger – trigger extracted from the input signal



Example of level trigger

FWDAQ – Interface to PC

- Analog Scaling
- Digital Scaling
- DBS
- Acquisition & Triggering
- Interface to PC

Multiple interface offering different compromise

- USB: Easy to use but limited in terms of data rate
- PCIe / PXIe: Fastest data rate, and optimized for large scale and chassis integration
- 10GbE: Enables long distance between digitizer and PC, provide electrical isolation
- MTCA.4: Optimized for very large scale integration

USB 3.0

PCI EXPRESS

PXI™ -5

µTCA®

10x GIGABIT ETHERNET

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- **Firmware FWATD for advanced noise filtering**
- Firmware FWPD for pulse data capture and analysis
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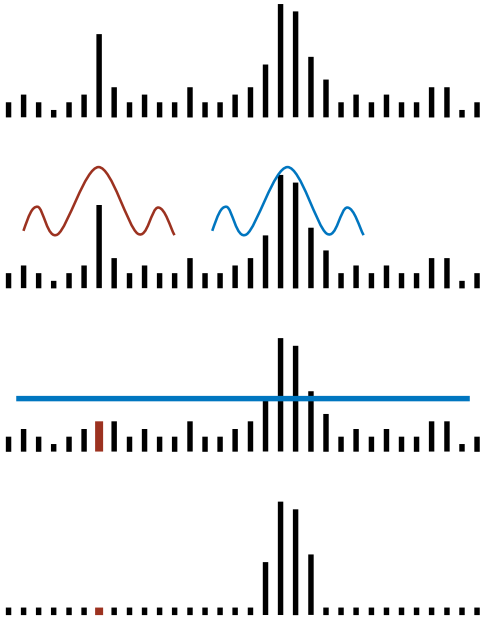
FWATD – Introduction

- FWATD is an application specific firmware for time-domain measurement with extreme dynamic range.
- The purpose of the firmware option –FWATD is to detect periodic pulses drowned into the noise through multiple noise suppresion steps.
- It contains multiple noise suppression functions to enhance signal to noise ratio in pulse measurement application.
- Capability to detect periodic pulse with a significant improvement of dynamic range

FWATD – Introduction

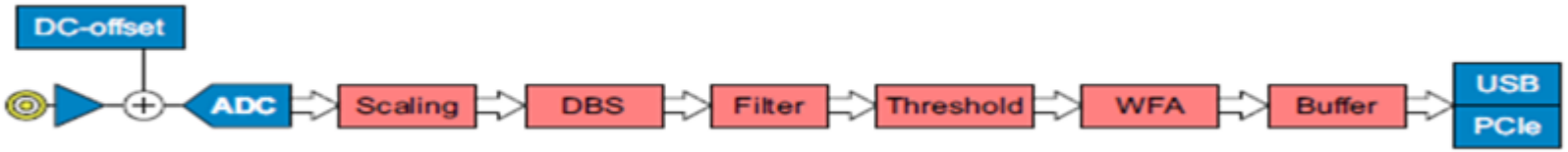
Applications

- High dynamic range pulse detection
- High sensitivity for weak pulse detection
- Detection of rare events

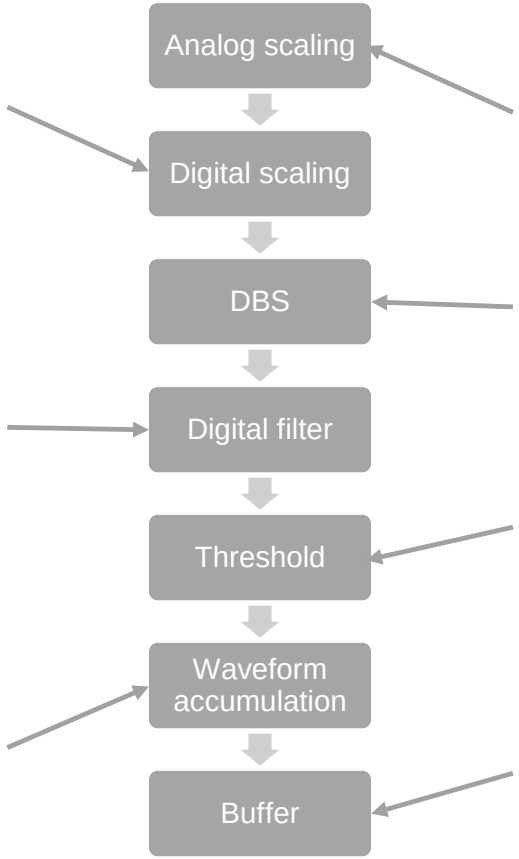


Key specifications

- Linear FIR filter for frequency domain noise suppression
- Baseline stabilization with DBS IP
- Non-linear threshold for time-domain noise suppression
- Waveform averaging
  - Waveform length up to 2 Msamples
  - Unlimited/Continuous accumulation number
- Dead time 20 ns for ADQ14 and 32ns for ADQ7DC (static)



FWATD – Firmware Overview



Digital gain and offset to simplify the application processing

Analog configurable DC-offset to optimize the dynamic range to the input signal

Digital Baseline Stabilization

Linear FIR filter provides additional noise filtering in the digital domain

Non-linear noise suppression discriminating samples below a defined level including a linear phase FIR filter

Waveform accumulation for noise suppression through repeated measurements

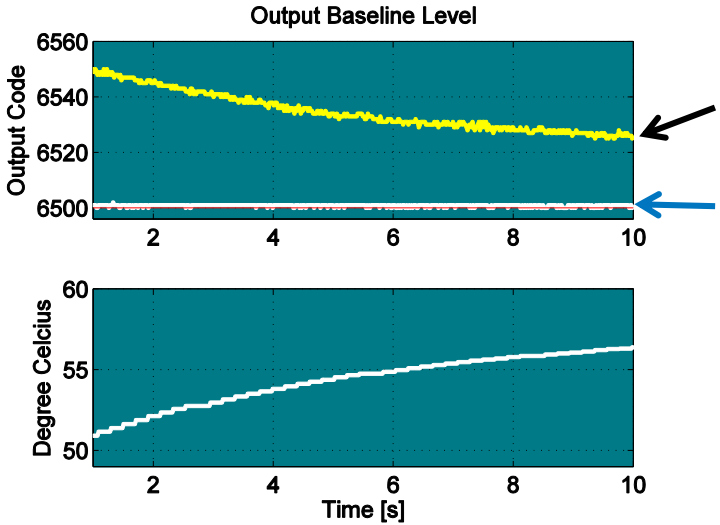
Ensures a dead-time free transfer acquisition

FWATD – Digital Baseline Stabilization

- Analog scaling
- Digital scaling
- **DBS**
- Digital filter
- Threshold
- Waveform accumulation
- Buffer

Digital Baseline Stabilizer tracks slow and periodic baseline variation

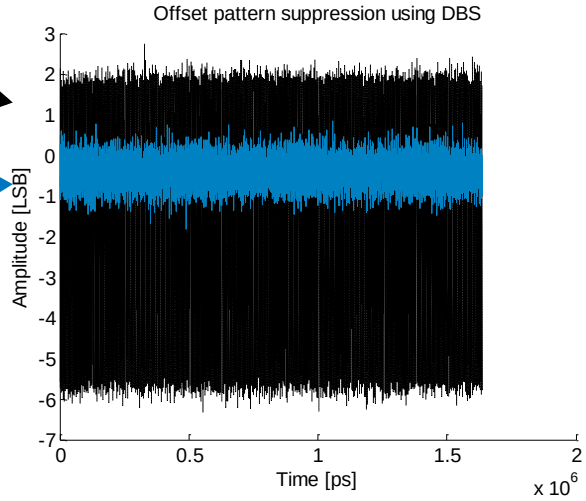
- Temperature variation
- Component aging
- Pattern noise from ADC due to interleaving



DBS benefit versus temperature variation

DBS disabled

DBS enabled

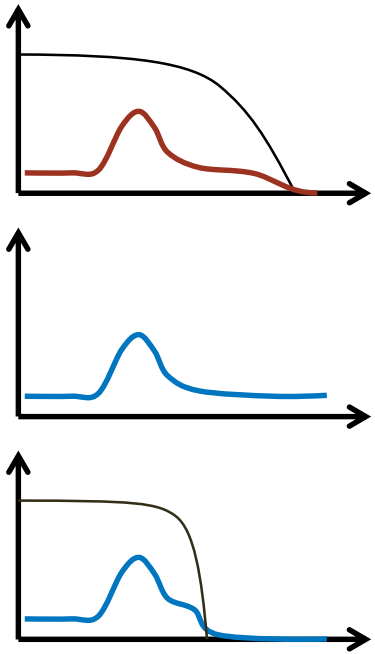


DBS benefit versus pattern noise

FWATD – Digital Filter

- Analog scaling
- Digital scaling
- DBS
- **Digital filter**
- Threshold
- Waveform accumulation
- Buffer

The digital FIR filter can be used as an additional linear noise suppression tool through filtering the high frequency noise

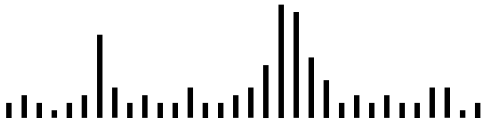


- Analog bandwidth filter high-frequency noise
- The sampled signal frequency domain has a flat noise floor
- Digital filter reduces noise power outside of the frequency band of interest

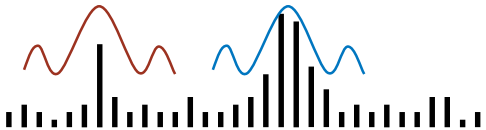
FWATD – Threshold

- Analog scaling
- Digital scaling
- DBS
- Digital filter
- **Threshold**
- Waveform accumulation
- Buffer

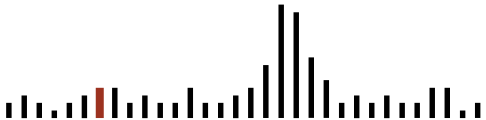
The threshold function provides a linear phasse FIR filter useful to shape the noise before aplying the threshold correction.



- Sampled signal



- The digital filter is designed to correlate with the pulse of interest (blue signal)

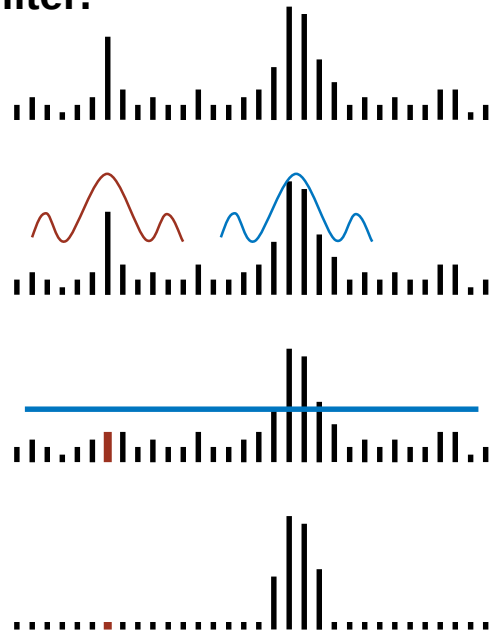


- Digital filter reduces the level of the uncorrelated noise pulse (red signal)

FWATD – Threshold

- Analog scaling
- Digital scaling
- DBS
- Digital filter
- **Threshold**
- Waveform accumulation
- Buffer

The threshold operation is a non-linear noise suppression function that sets noise below a threshold to a defined level. Its effectiveness can be enhanced through the previous use of the linear phase FIR filter.

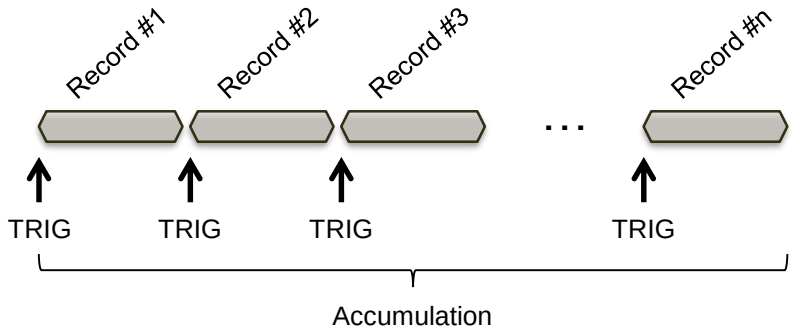


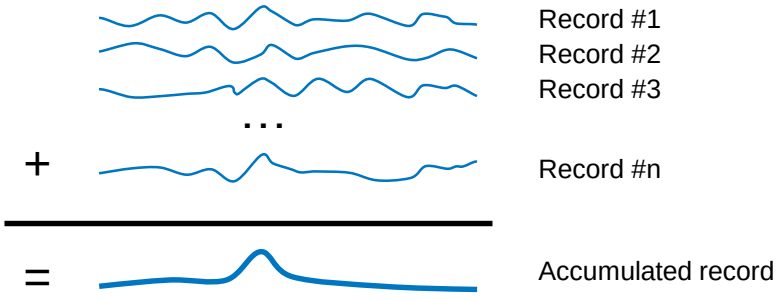
- Sampled signal
- The digital filter suppress linear noise
- The threshold level is defined as the blue line
- Every samples below the threshold level is set to a defined level

FWATD – Waveform accumulation

- Analog scaling
- Digital scaling
- DBS
- Digital filter
- Threshold
- **Waveform accumulation**
- Buffer

The waveform accumulation function accumulates a large number of waveforms for noise suppression by repeated measurements.





ADQ7DC	
Record length	+ Up to 2Mi samples (1CH) + Up to 1Mi samples (2CH) + 200µs
Accumulation number	+ 262144 in FWATD with safe scaling + Infinite if continued in User Application
Dead-time	+ 32ns

ADQ14	
Record length	+ Up to 2Mi samples (2GSps) + Up to 1Mi samples (1, 0.5GSps) + 1ms
Accumulation number	+ 65536 in FWATD with safe scaling + Infinite if continued in User Application
Dead-time	+ 20ns

FWATD – Buffer for Seamless Streaming

Analog scaling

Digital scaling

DBS

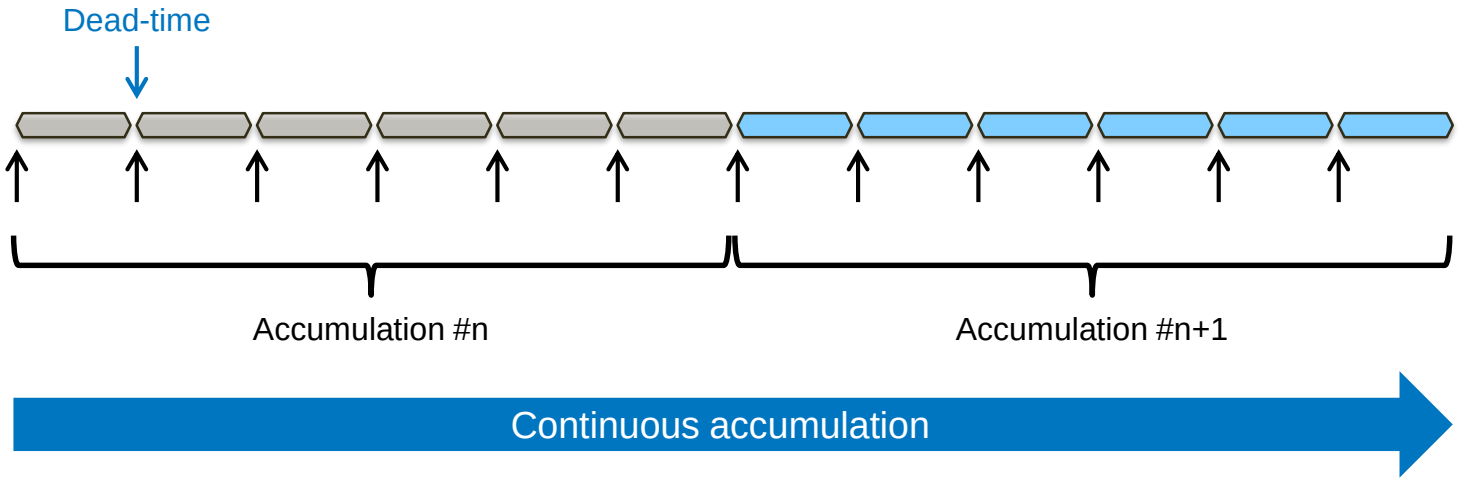
Digital filter

Threshold

Waveform accumulation

Buffer

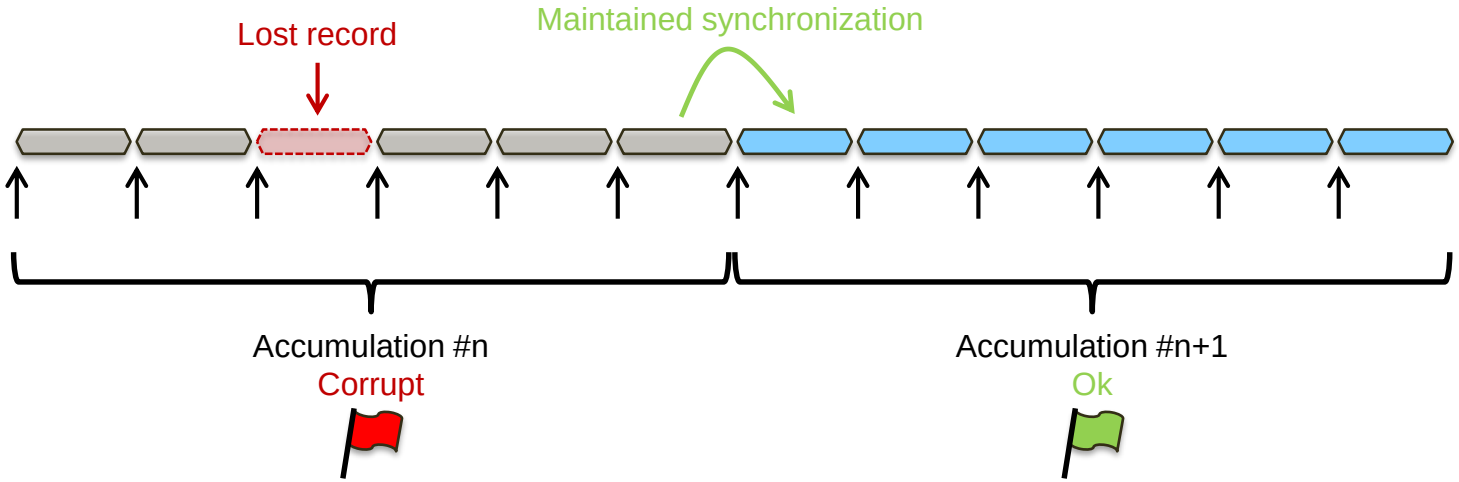
The buffer interfacing with the PC enables continuous seamless acquisition and accumulation. Fail-safe design for the interface between digitizer and PC is achievable for reliable, sustained operation.



FWATD – Buffer for Seamless Streaming

- Analog scaling
- Digital scaling
- DBS
- Digital filter
- Threshold
- Waveform accumulation
- **Buffer**

The buffer interfacing with the PC enables seamless acquisition and accumulation. Fail-safe design for the interface between digitizer and PC is achievable for reliable, uninterrupted operation.



- The digitizers are designed for real-time, sustained uninterrupted operation but they are only one part of the system. They can control and manage the system for reliable operation with automatic fault recovery.

FWATD – Introduction

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- It contains multiple noise suppression functions to enhance signal to noise ratio in pulse measurement application.
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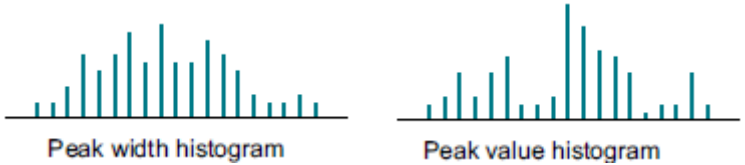
FWPD – Introduction

- FWPD is a flexible and powerful firmware option tailored for demanding pulse data applications with random events.
- The purpose of the firmware option –FWPD is to detect pulses and adapt the data collection to the properties of the pulses.
- Signal without information is discarded and disk space is saved.
- Pulse analysis is possible in real-time in the FPGA or in the host PC
- Timing rules for when to accept pulses

FWPD – Introduction

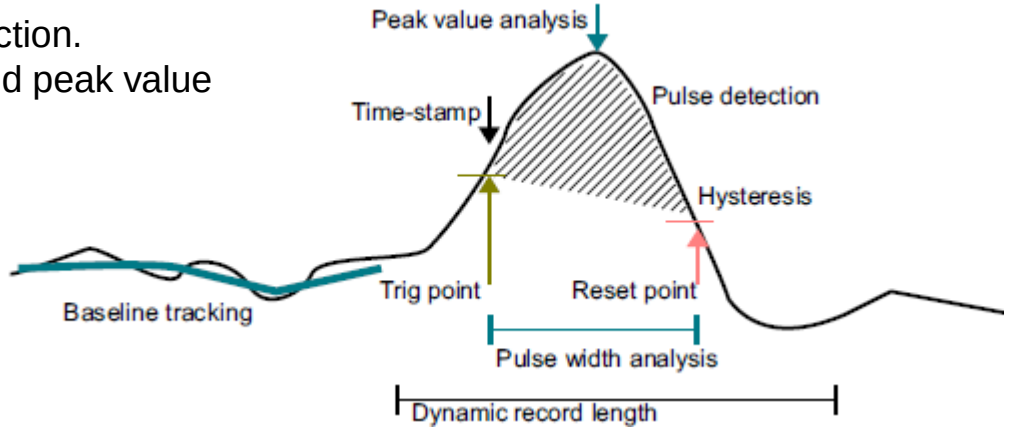
Applications

- Random pulse detection



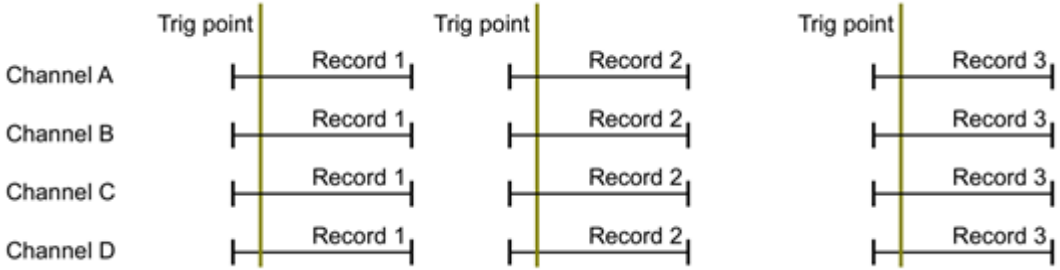
Key specifications:

- Baseline stabilization with moving averaging filter or DBS IP
- Adaptive record length for zero suppression
- Individual trigger and data recording
- Coincidence trigger for channels interaction.
- Histogram calculation of pulse width and peak value
- Time-stamp with 25ps precision



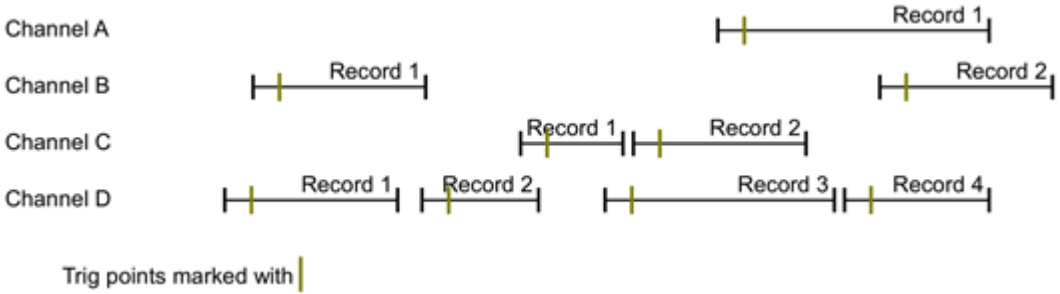
FWPD vs standard firmware FWDAQ

FWDAQ – Default Firmware



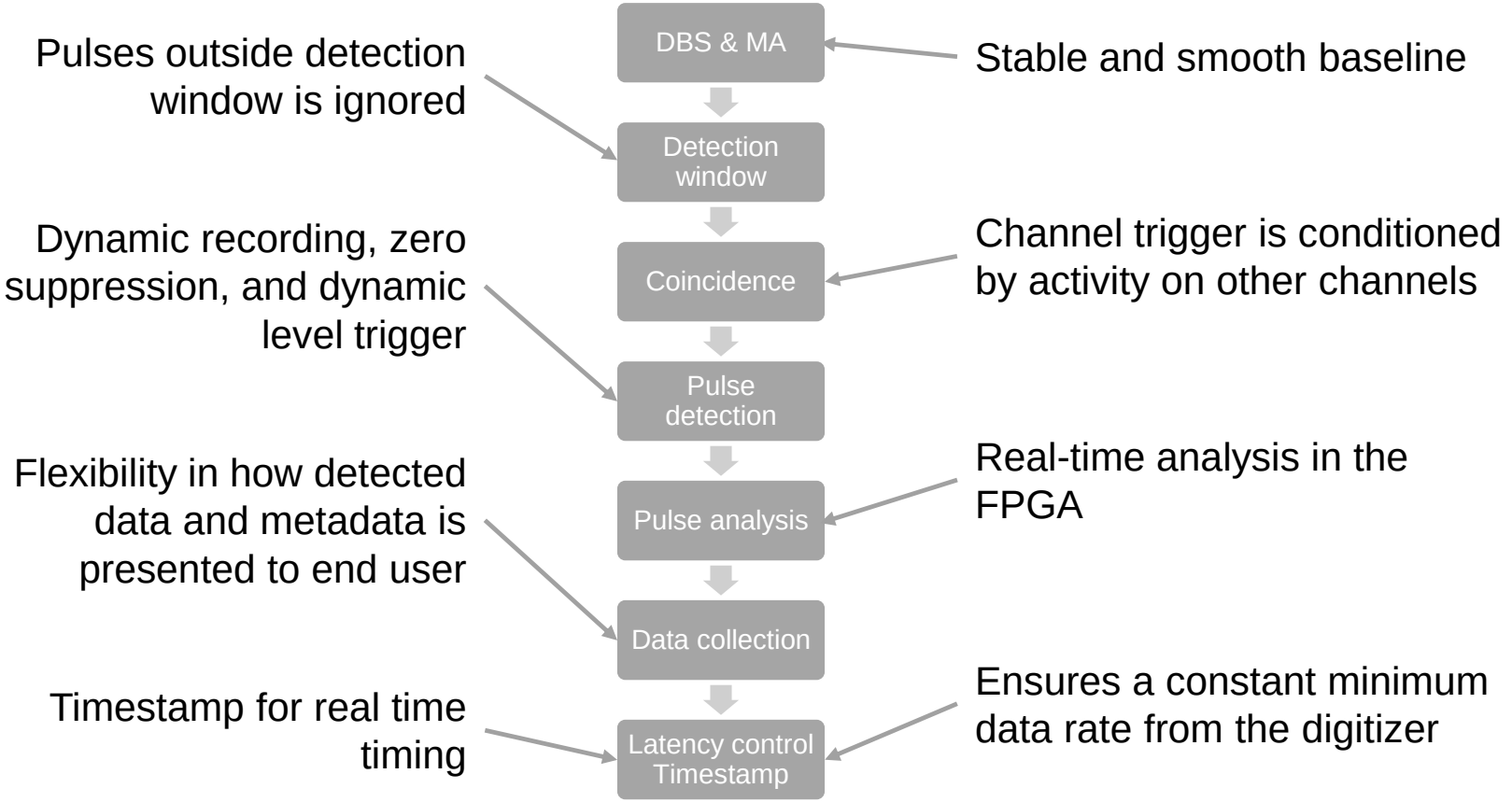
- Trigger applies on all channel simultaneously
- Record length is fixed

FWPD – Pulse Data Firmware



- Independent trigger capability per channel
- Dynamic record length to optimize the amount of data captured, processed and transferred to the PC

FWPD – Firmware Overview



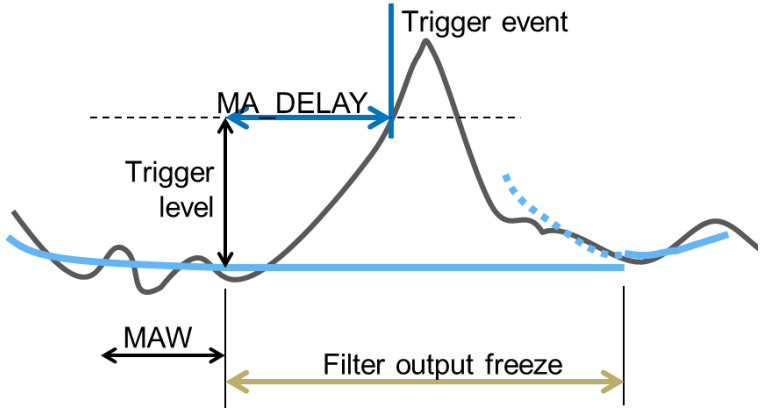
FWPD – Moving Average Filter & Digital Baseline Stabilization

DBS & MA

- Detection window
- Coincidence
- Pulse detection
- Pulse analysis
- Data collection
- Latency control Timestamp

Moving average filter tracks rapid baseline variation

- Pulse leakage, noise and interference
- Rapid signal variations
- Reduces sensitivity to rapid variations to avoid false trigger event



Digital Baseline Stabilizer tracks slow and periodic baseline variation

- Temperature variation
- Component aging
- Pattern noise from ADC due to interleaving

DBS

TELEDYNE SP DEVICES

FWPD – Detection window and Coincidence

DBS & MA

Detection window

Coincidence

Pulse detection

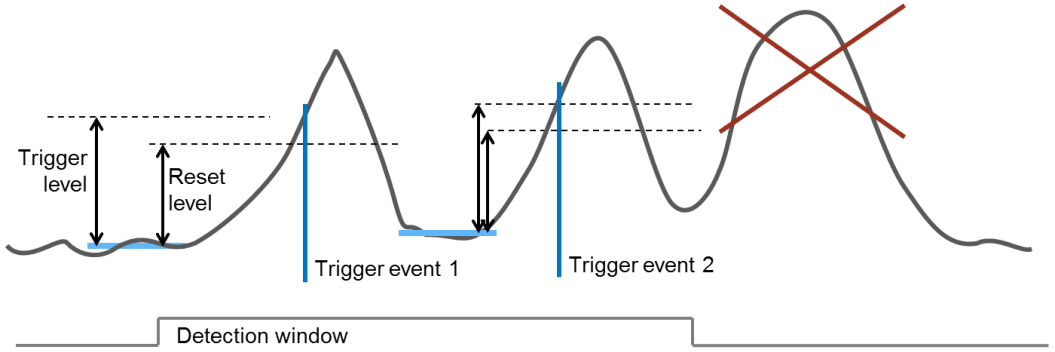
Pulse analysis

Data collection

Latency control Timestamp

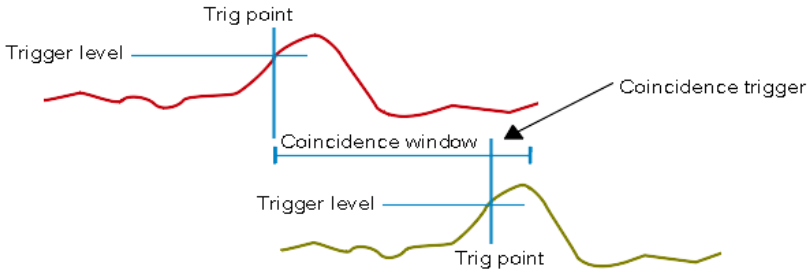
Detection window to control when triggers are accepted

- The last pulse does not trigger a recording, it is outside of the detection windows



Coincidence when channel dependancies is necessary

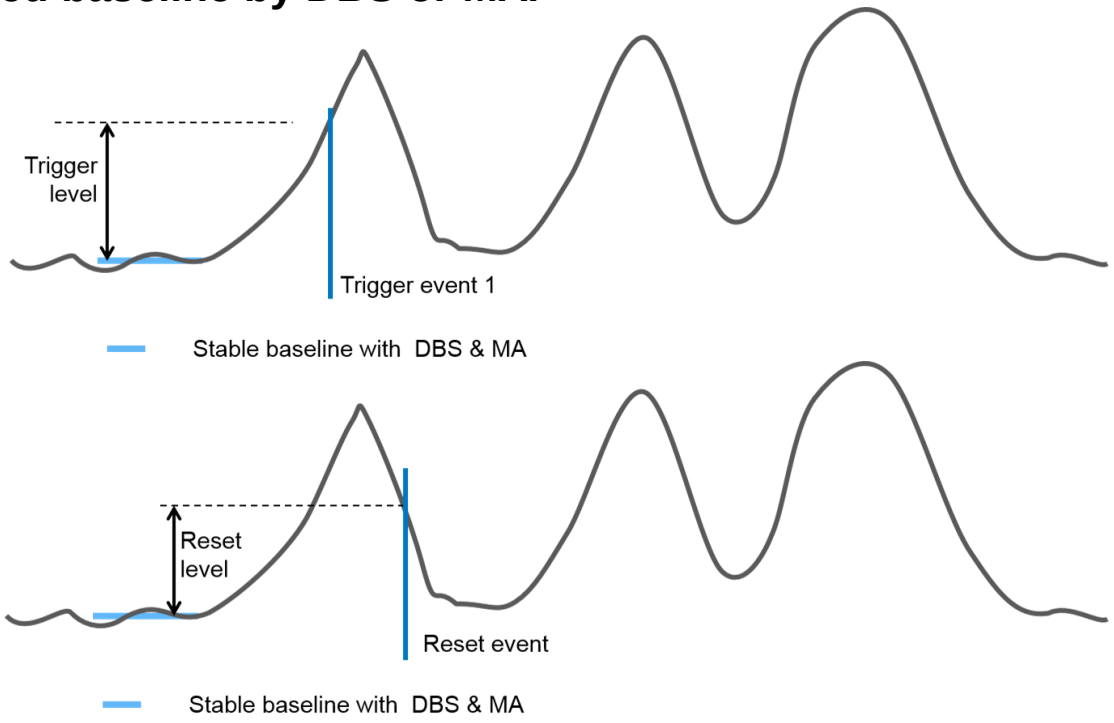
- Trigger on green channel will be considered only within a configured timeslot after the red channel is triggered



FWPD – Pulse Detection

- DBS & MA
- Detection window
- Coincidence
- **Pulse detection**
- Pulse analysis
- Data collection
- Latency control Timestamp

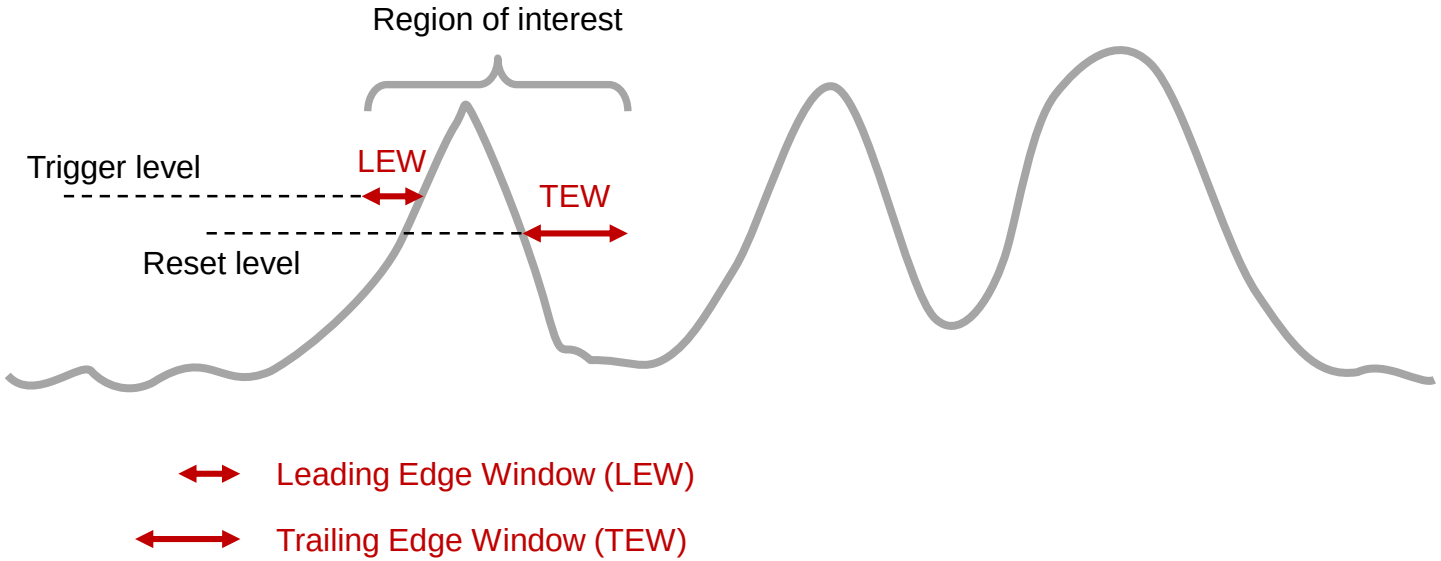
The pulse start is determined by the trigger level, while the pulse end is determined by the reset level. These levels are following the stabilized baseline by DBS or MA.



FWPD – Pulse Detection

- DBS & MA
- Detection window
- Coincidence
- **Pulse detection**
- Pulse analysis
- Data collection
- Latency control Timestamp

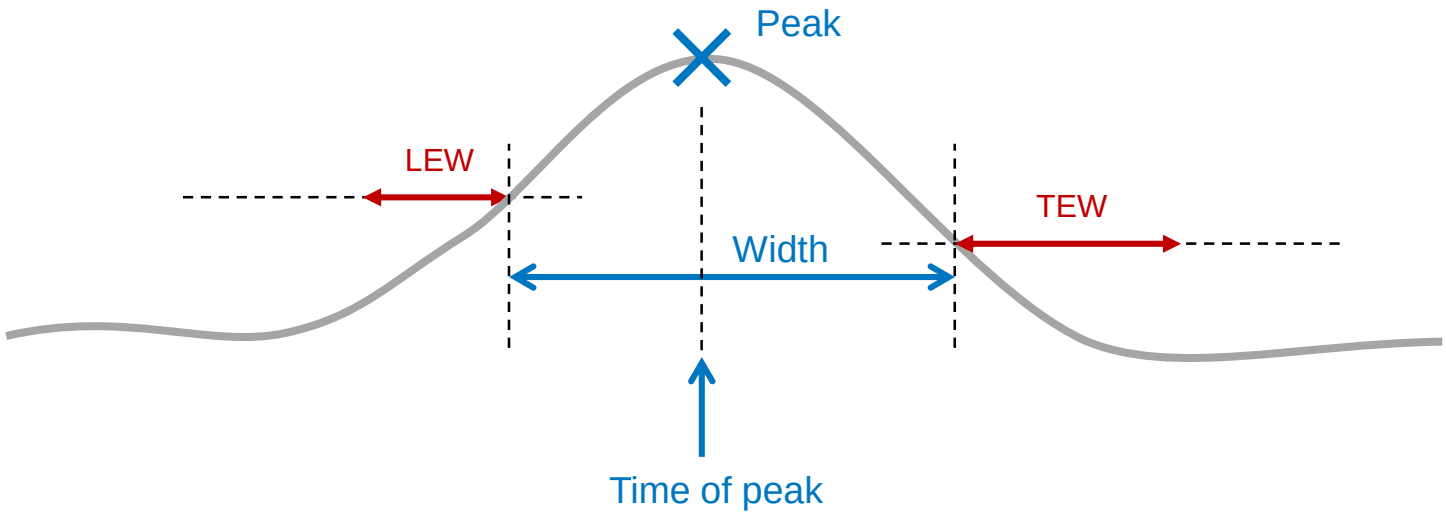
The pulse recorded can include the edges through the configuration of the leading and trailing edge window parameters



FWPD – Pulse Analysis

- DBS & MA
- Detection window
- Coincidence
- Pulse detection
- **Pulse analysis**
- Data collection
- Latency control Timestamp

Functions to measure the pulse maximum, width and time are available.



FWPD – Pulse Analysis

DBS & MA

Detection window

Coincidence

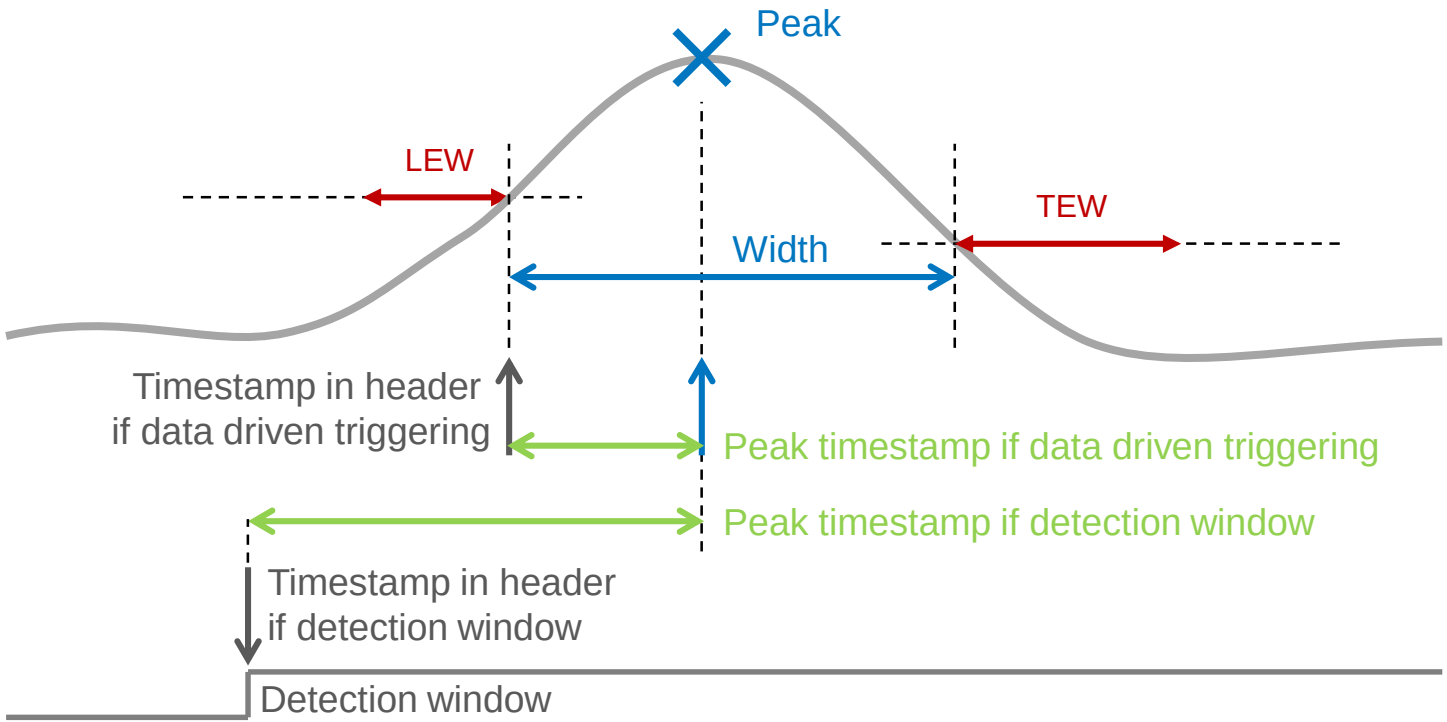
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

The peak time information recovered through the timestamp can be defined in two different ways



FWPD – Pulse Analysis

DBS & MA

Detection window

Coincidence

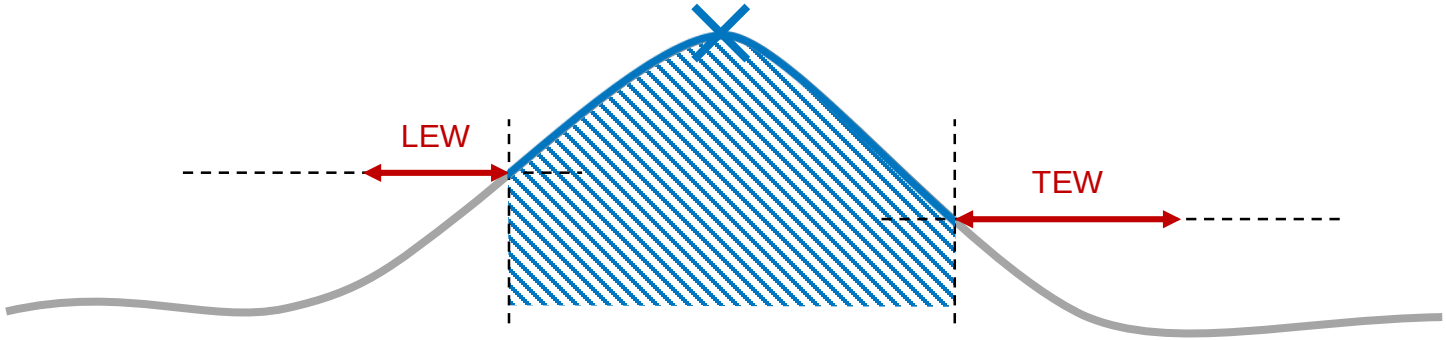
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

Each application requires a unique pulse analysis. The FPGA is thus open for custom designs by the customer. TSPD's design service is available to support the implementation work.



Example of analysis:

- Area
- Power
- Custom peak definition
- Gaussian curve fit
- Spline interpolation
- Qualify / disqualify pulse

FWPD – Data collection

DBS & MA

Detection window

Coincidence

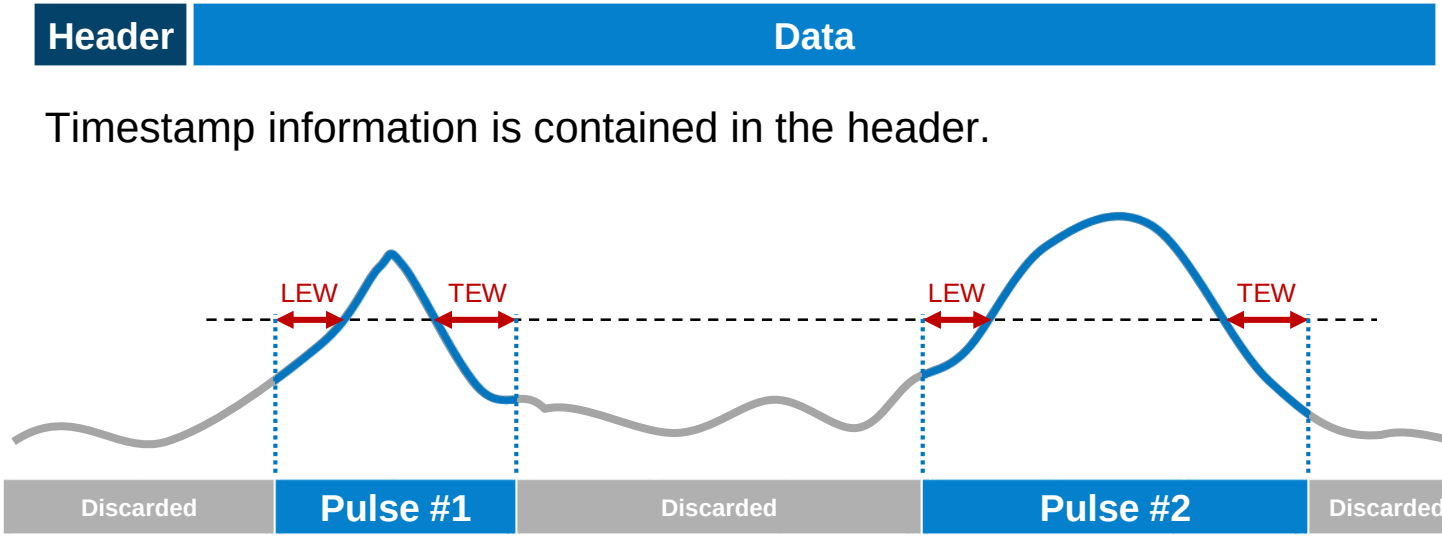
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

Data is collected in records with record headers and sent to user.



Raw data or metadata of pulse #1 and pulse #2 are collected in records. All other data is ignored optimizing the data processed and transferred to the PC.

FWPD – Data collection

DBS & MA

Detection window

Coincidence

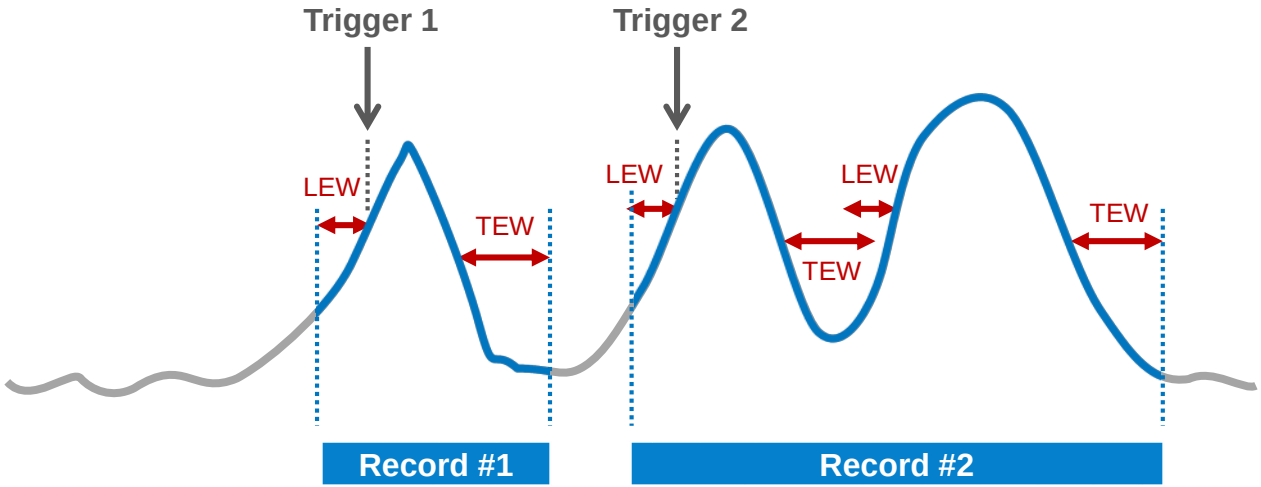
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

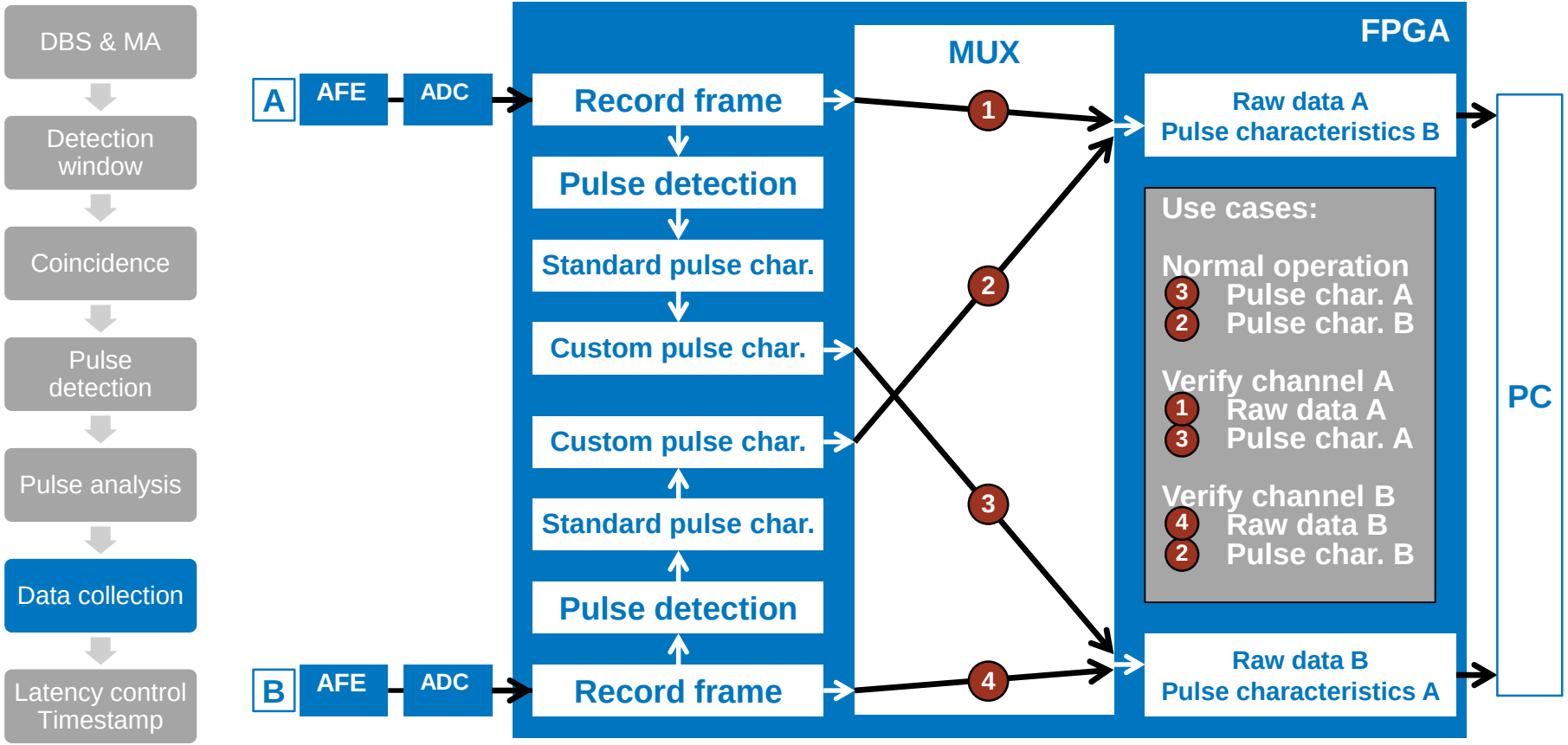
When multiple consecutive pulses overlap, the record length is adapted to capture all without loss of information.



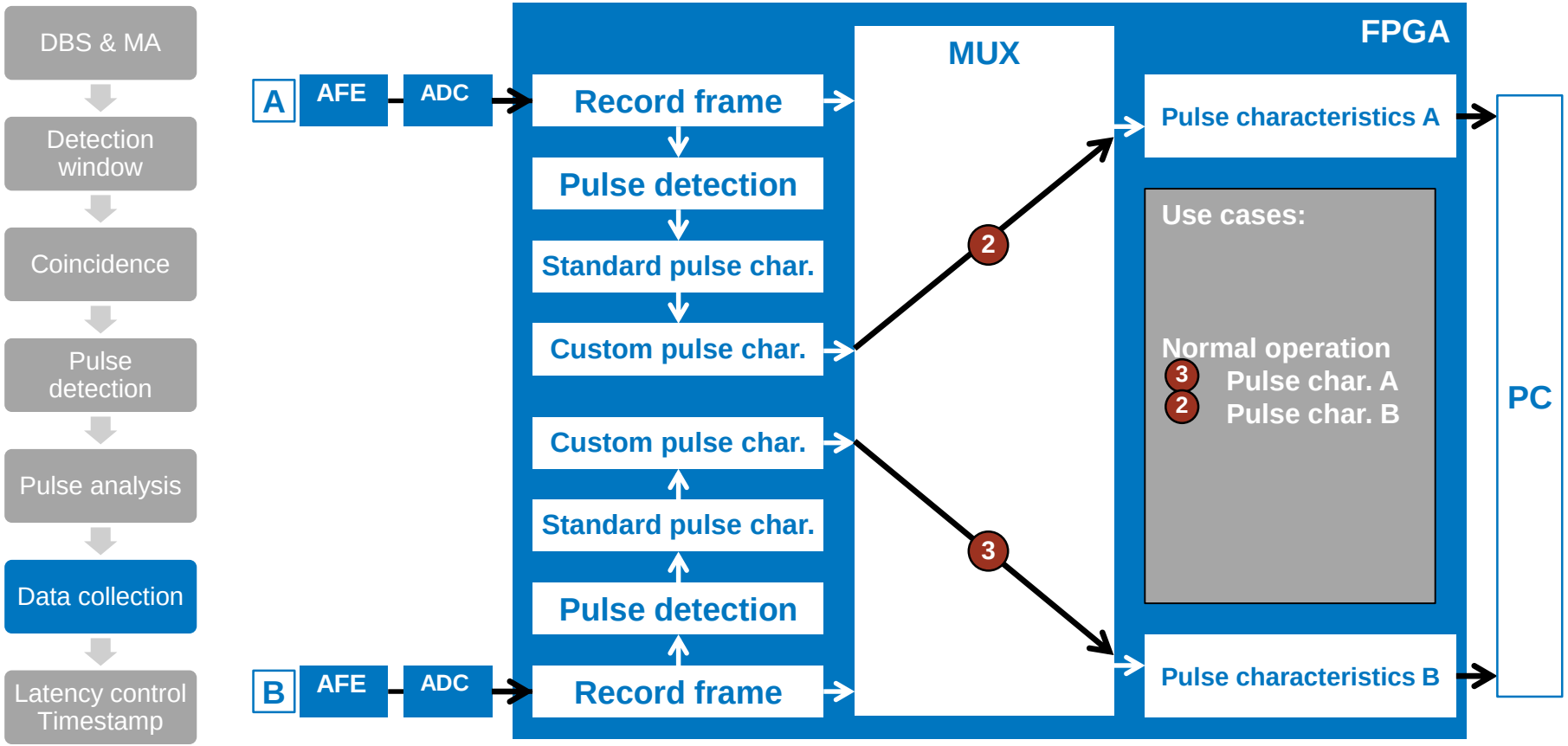
Leading Edge Window (LEW)

Trailing Edge Window (TEW)

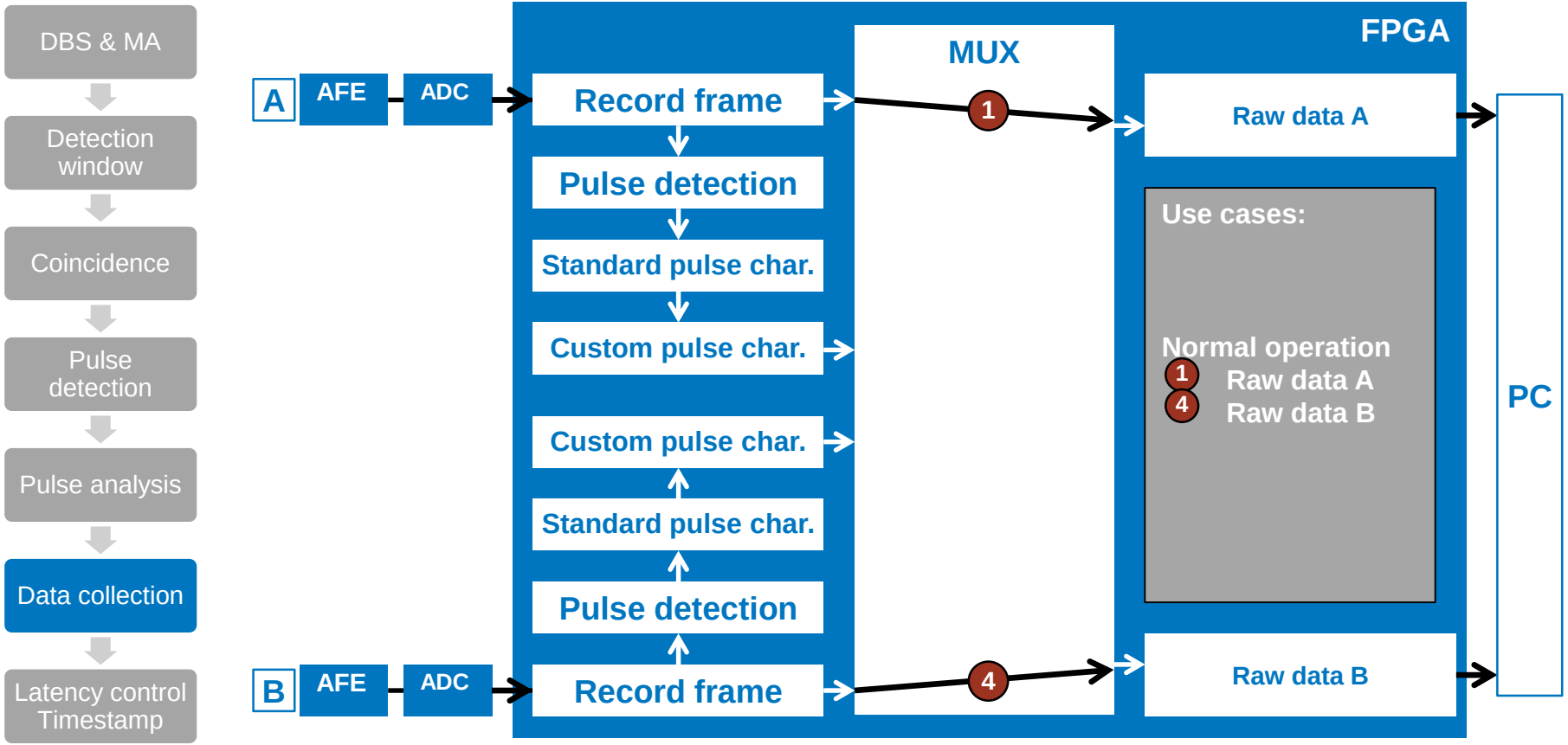
FWPD – Data collection



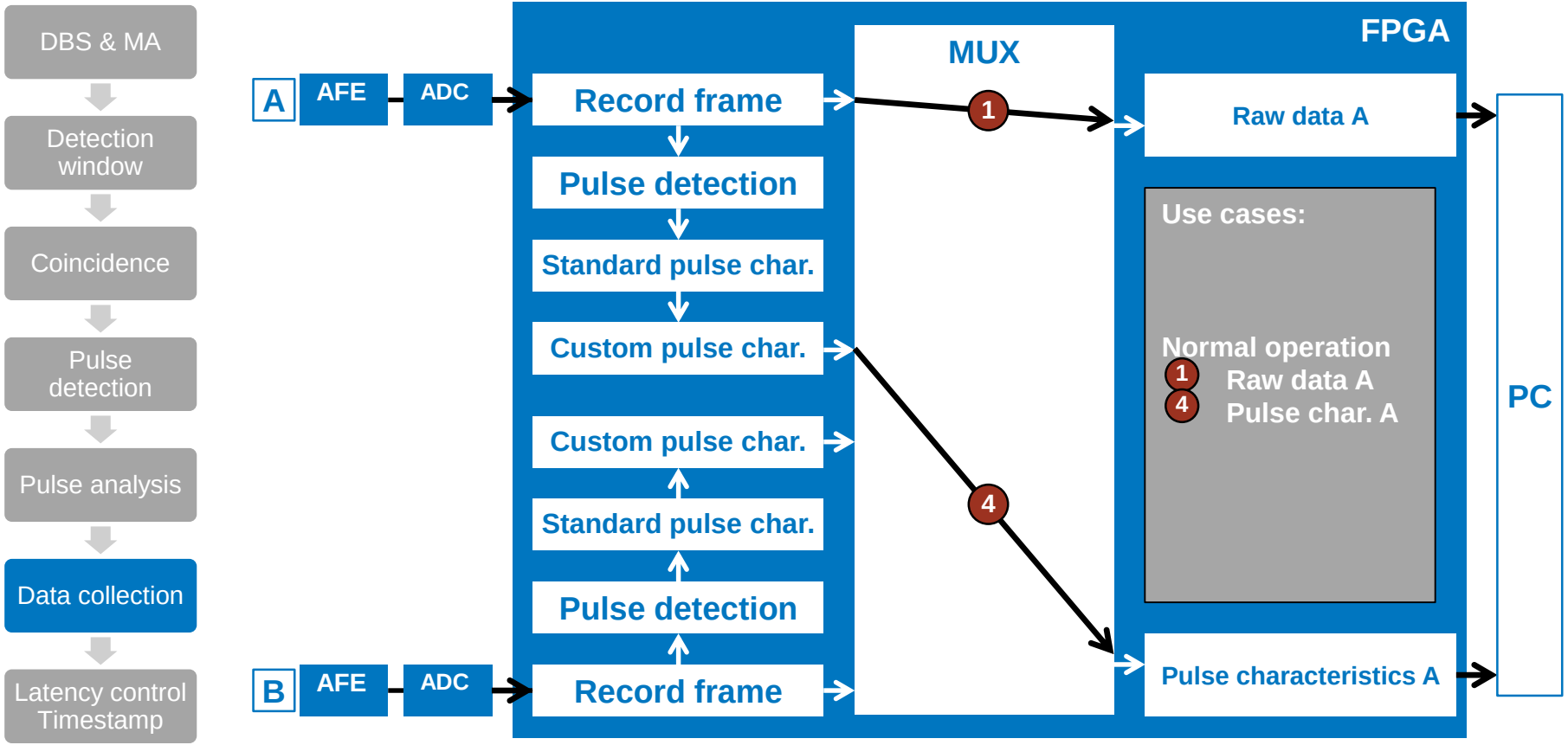
FWPD – Data collection



FWPD – Data collection



FWPD – Data collection



FWPD – Data collection

DBS & MA

Detection window

Coincidence

Pulse detection

Pulse analysis

Data collection

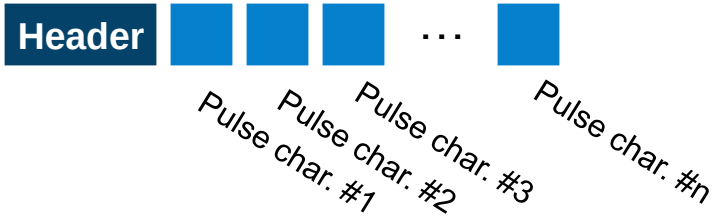
Latency control Timestamp

Meta data with pulse characteristics are stored in metadata packages.

Header	Pulse #1	Pulse #2	#3	#n
Time-stamp 64b	**Peak** 16b **Width** 16b **Time of peak** 32b	**Peak** 16b **Width** 16b **Time of peak** 32b		

Header	Pulse #1	Pulse #2	#3	#n
Time-stamp 64b	**Cust. value1** x bits **Cust. value2** y bits …	**Cust. value1** x bits **Cust. value2** y bits …		

Metadata record



FWPD - Timestamp

DBS & MA

Detection window

Coincidence

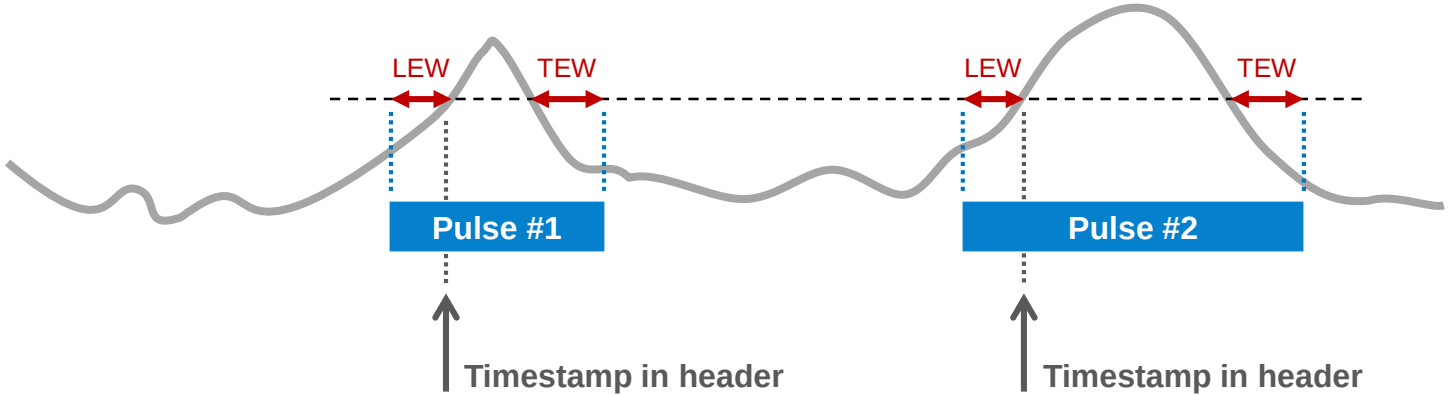
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

When no detection window is used, the timestamp increments without reset. It can be reset by external trigger or sync signals.



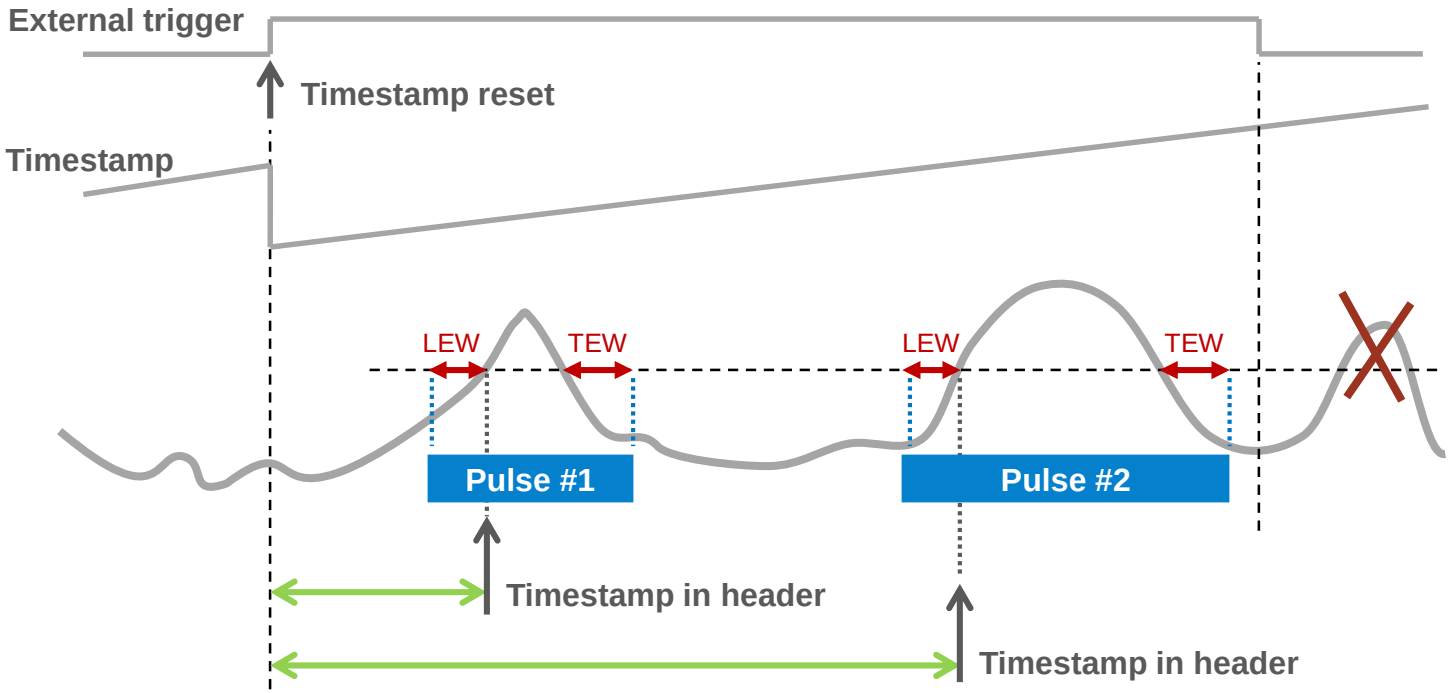
Raw data channel | Header | Raw data #1 | Header | Raw data #2

Pulse char. channel | Header | | Pulse char. #1 | Header | | Pulse char. #1

FWPD - Timestamp

- DBS & MA
- Detection window
- Coincidence
- Pulse detection
- Pulse analysis
- Data collection
- Latency control Timestamp

When detection window is used, the timestamp is reset every time the detection window starts. It can also be reset by external trigger or sync signals.



FWPD – Latency control

DBS & MA

Detection window

Coincidence

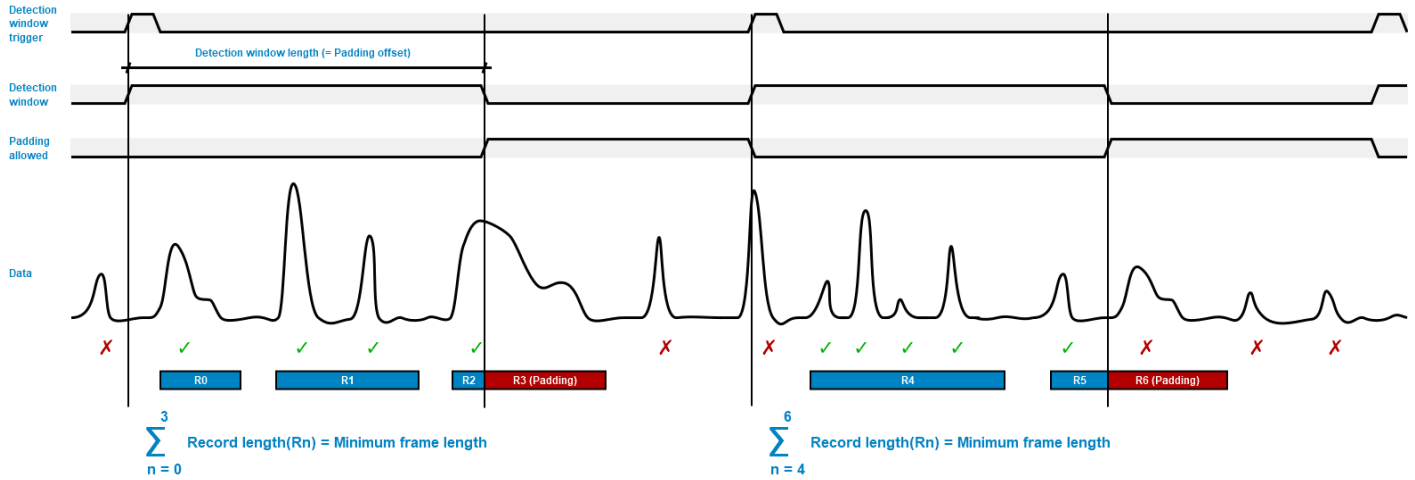
Pulse detection

Pulse analysis

Data collection

Latency control Timestamp

- Latency is controlled by adding the feature of padding.
- It will ensure a constant data rate from the digitizer.
- The padding block will append zeros to the data to ensure that the total amount of data measured over one is at least equal to the minimum frame length.
- Minimum frame length is set by the user



FWPD – Introduction

- FWPD is a flexible and powerful firmware option tailored for demanding pulse data applications with random events.
- The purpose of the firmware option –FWPD is to detect pulses and adapt the data collection to the properties of the pulses.
- Signal without information is discarded and disk space is saved.
- Pulse analysis is possible in real-time in the FPGA or in the host PC
- Timing rules for when to accept pulses

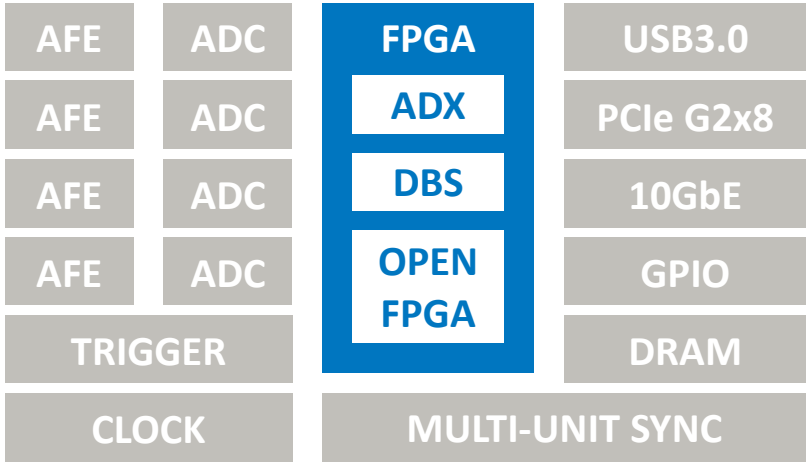
- Digitizer definition and application
- Firmware FWDAQ for standard acquisition and triggering
- Firmware FWATD for advanced noise filtering
- Firmware FWPD for pulse data capture and analysis
- **Development Kit for open FPGA access**
- Conclusion

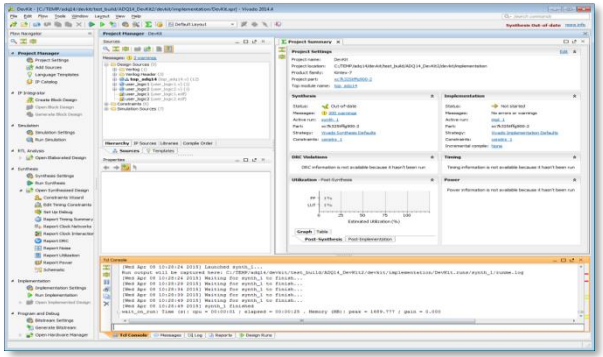
FPGA Dev Kit - Overview

- FPGA Development Kit is an optional firmware development kit consisting of project files and examples for Xilinx Vivado Design Suite

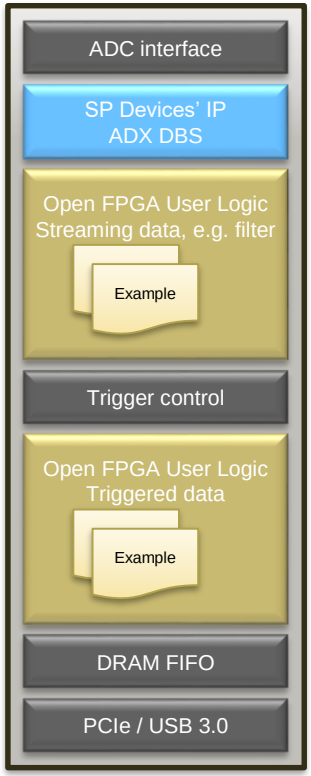
VIVADO™

- FPGA resource utilization varies between models, but as an example the dual-channel, 2 GS/s model ADQ14-2X utilization is:
  - DSP48E multipliers : 5%
  - Logic slices : 21%
  - Logic LUTs : 32%
  - RAMB36 memory : 31%





FPGA Dev Kit - Block diagram



Standard Teledyne SP Devices signal conditioning functions.

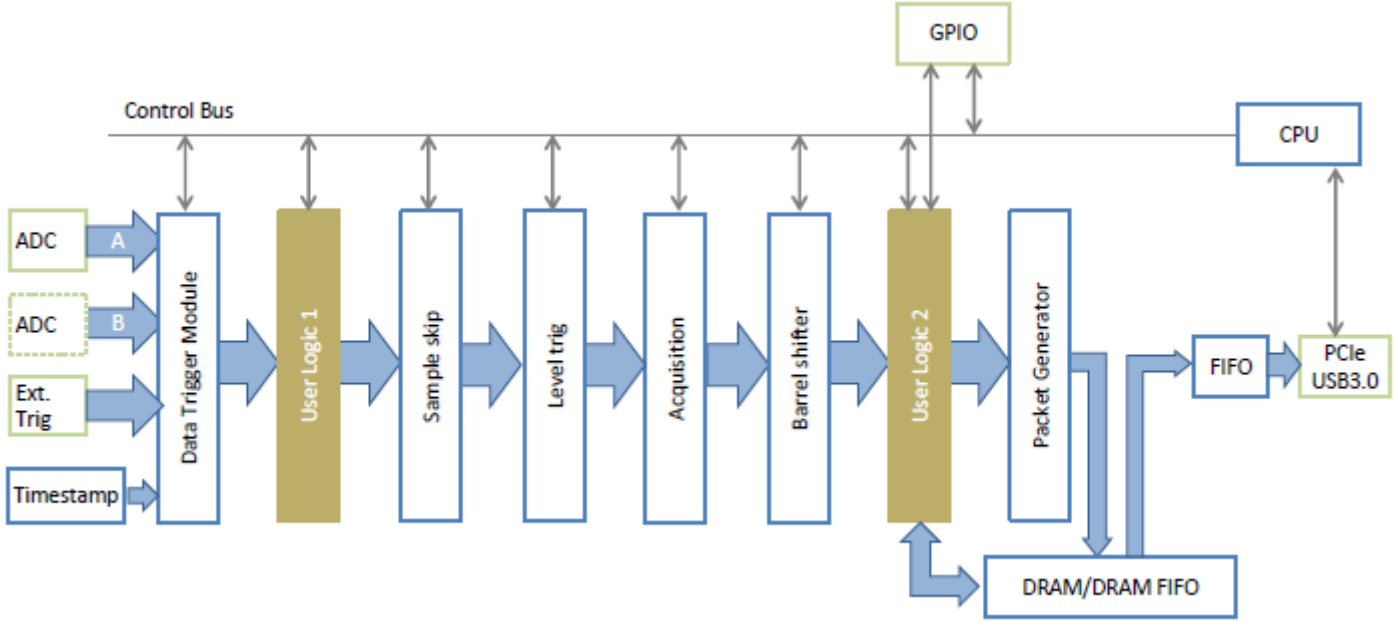
Data is streaming through and accessible in real-time.
Place streaming functions like filters and data flow triggers here.

Trigger data to form records.

Data is packaged in records relative to a trigger.
Place data records analysis like peak detection and data discrimination here.

Buffer data and send to the host PC using standard acquisition modes.

FPGA Dev Kit - Block diagram



User Logic 1: Data is streaming through and accessible in real-time.
Place streaming functions like filters and data flow triggers here.
User Logic 2: Data is packaged in records relative to a trigger.
Place data records analysis like peak detection and data discrimination here.

- Digitizer definition and application
- Firmware FWDAQ for standard acquisition and triggering
- Firmware FWATD for advanced noise filtering
- Firmware FWPD for pulse data capture and analysis
- Development Kit for open FPGA access
- **Conclusion**

Conclusion

- Teledyne SP Devices digitizer offer wide range of firmware option and function enabling many applications
- Firmware options dedicated to noise optimization (FWATD) and pulse data capture and analysis (FWPD) are available
- The development kit offers access to the FPGA for the most specific and demanding applications
- See a demonstration of an ADQ14 digitizer in our booth 214

Thank you