
# ADI Radio Solutions to Enable 5G MIMO and Small Cell

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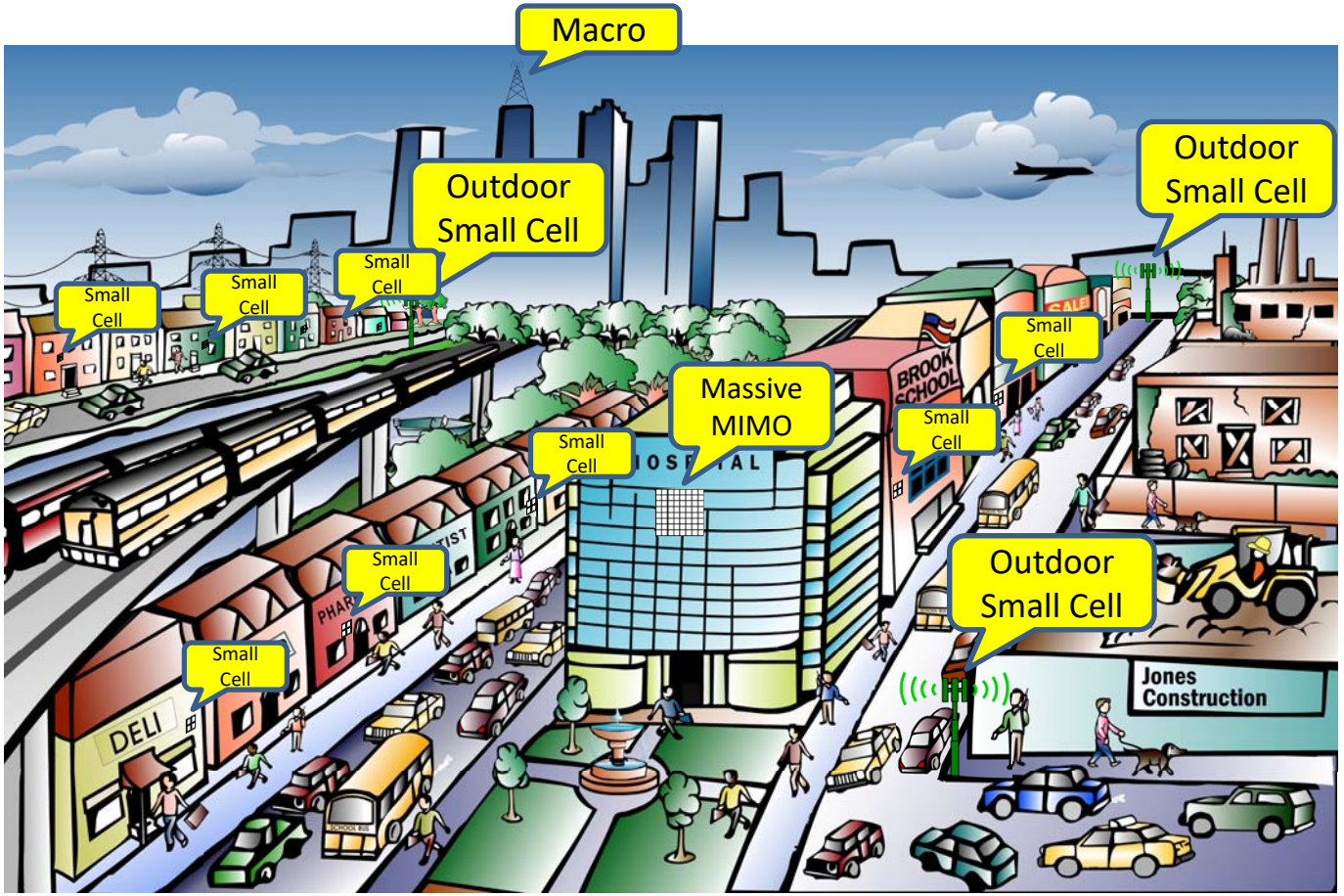
# Abstract

For 5G, there are many new systems, like MIMO and small cells, needed to support new businesses. They have more antenna channels than before (MIMO), or much higher power/size constraints (small cell), at the same time operating with a wider spectrum. This workshop explains ADI's latest radio technology, which brings multi-channel converters, LOs, RF front ends and digital front ends together to greatly improve the integration level while maintain performance. In addition, ADI developed power over Ethernet, attached power, clock, and RF solutions around its Integrated radio product to make it easeir to build a 5G solution.

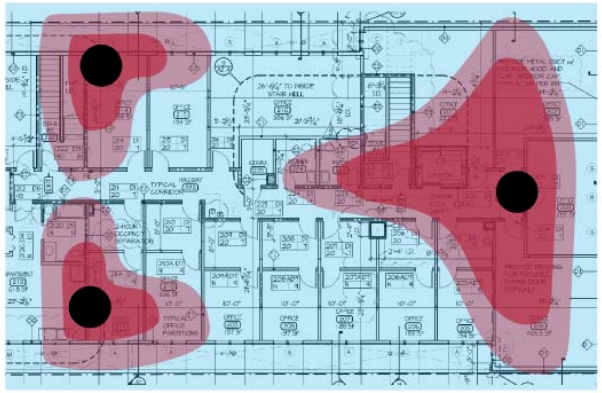
# 5G is about Coverage & Capacity



# Small Cell

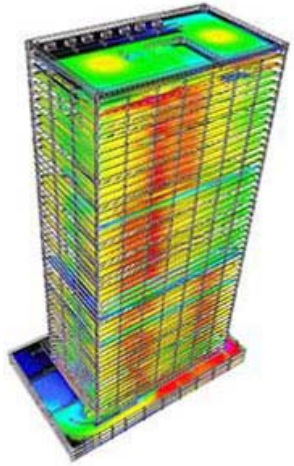
**Benefits**

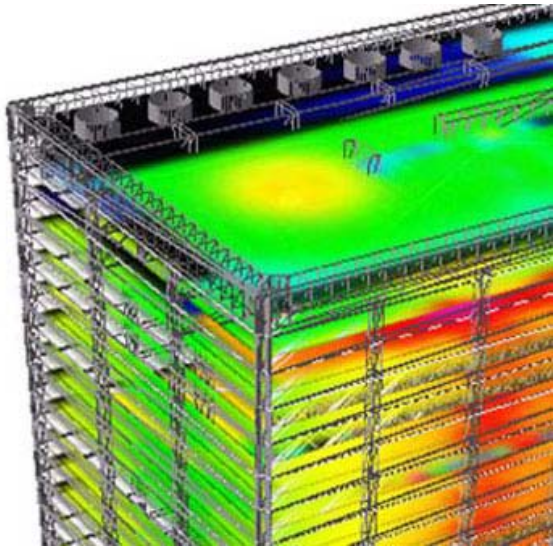
- Enables consistent coverage in difficult to reach locations
- Improve capacity in densely populated areas like offices, arenas and residential areas.



**Challenges**

- Large number of deployment sites drives
  - Cost point
  - Power dissipation requirements
  - Size
  - Weight restrictions





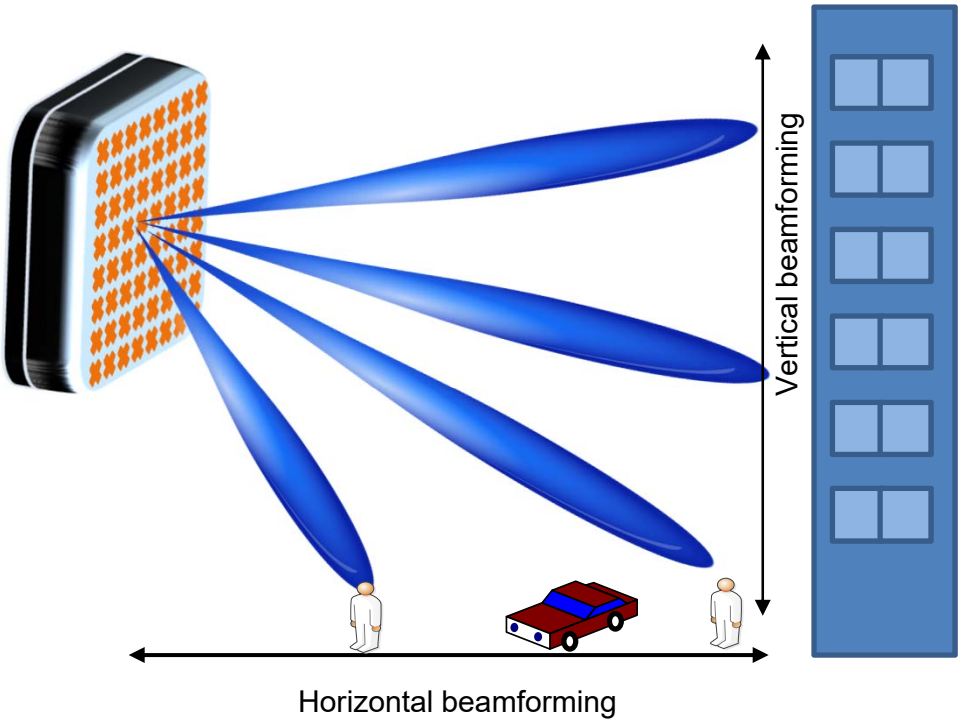
# Massive MIMO

**Benefits**

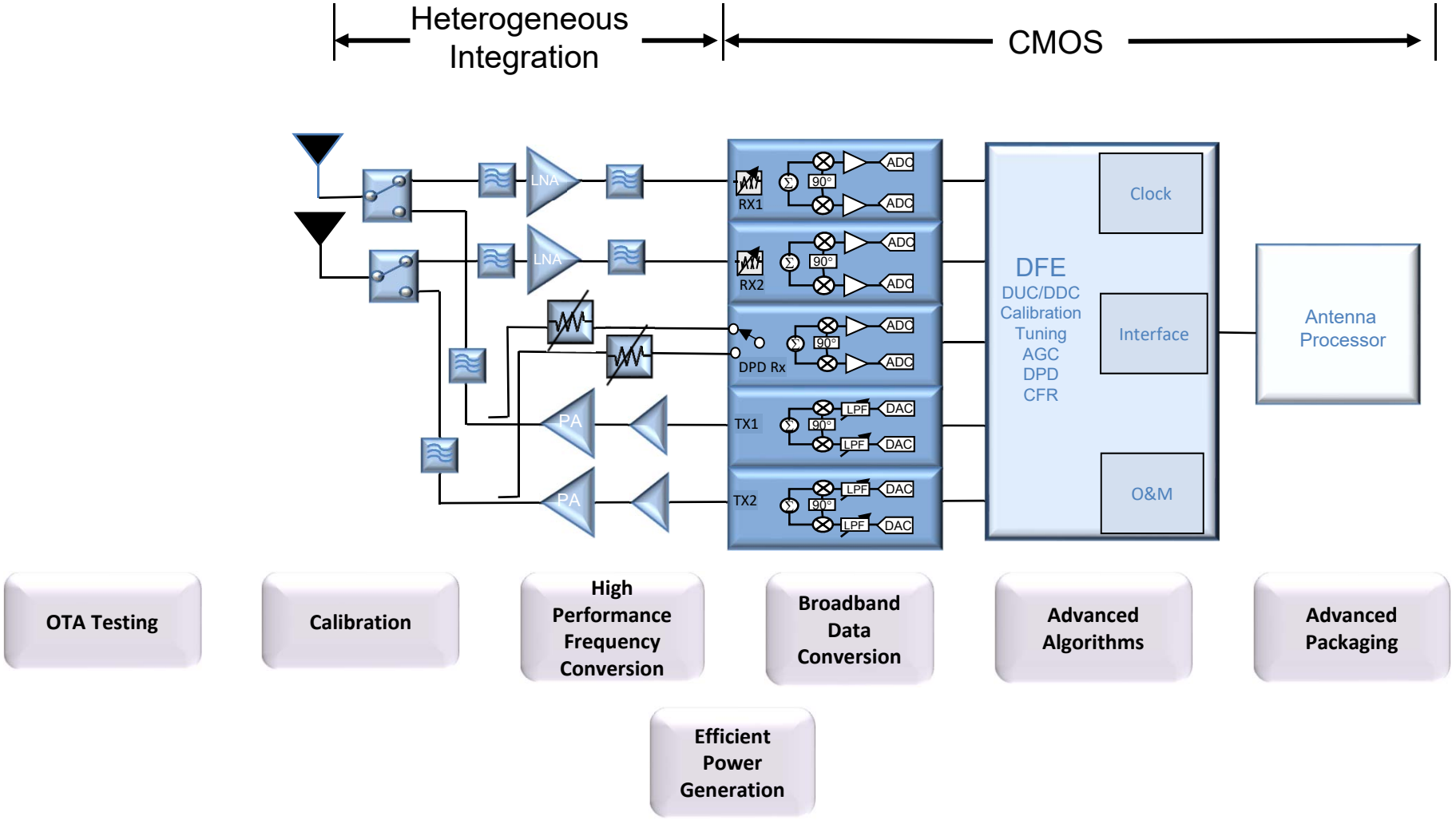
- Increased capacity through spatial diversity in both azimuth and elevation
- Improves coverage by focusing RF energy directly to the user
- Spectral management supports improved efficiency and user allocations.

**Challenges**

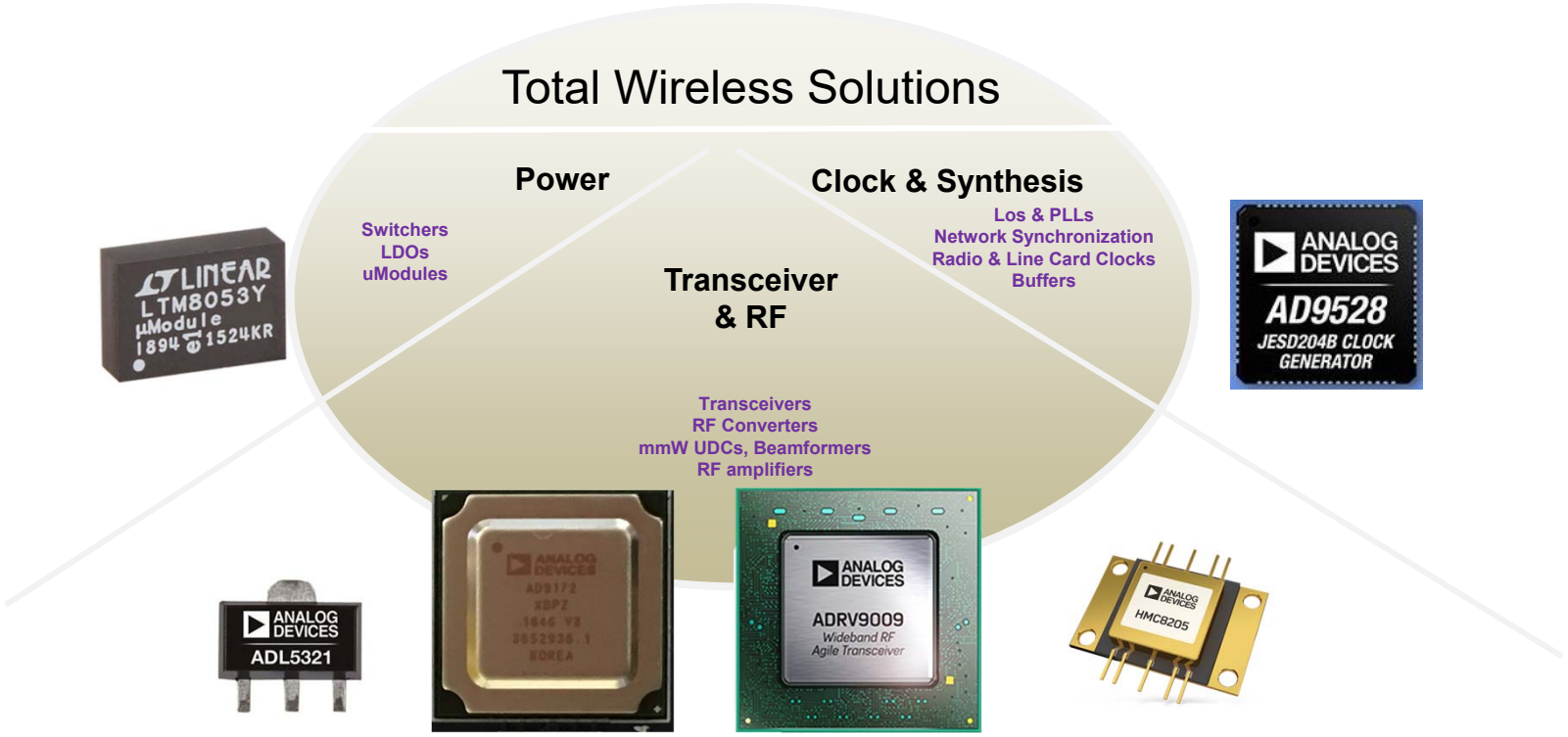
- Large number of radio units per site require
  - Low cost radios
  - Small size to facilitate system integration
  - Low weight required to ease of installation
  - Low power required for thermal management



# The Right Innovation



# Comprehensive Solution



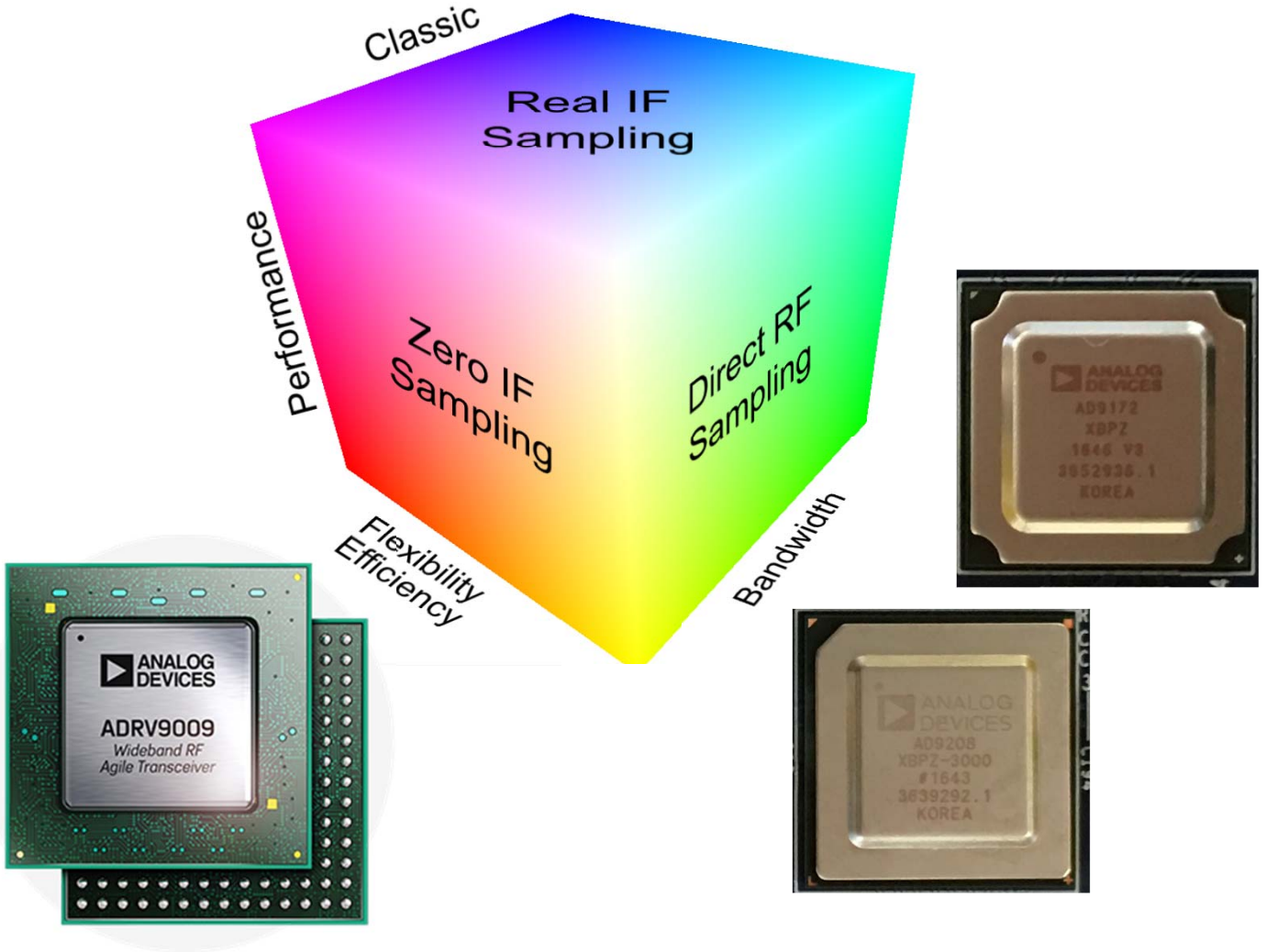

Co-operative solutions encompassing all aspects of the signal chain

# Radio Solutions

- Flexible
- Efficient
- Wideband
- Low Power
- Scalable
- Configurable
- Integrated
- Cost efficient
- High Density

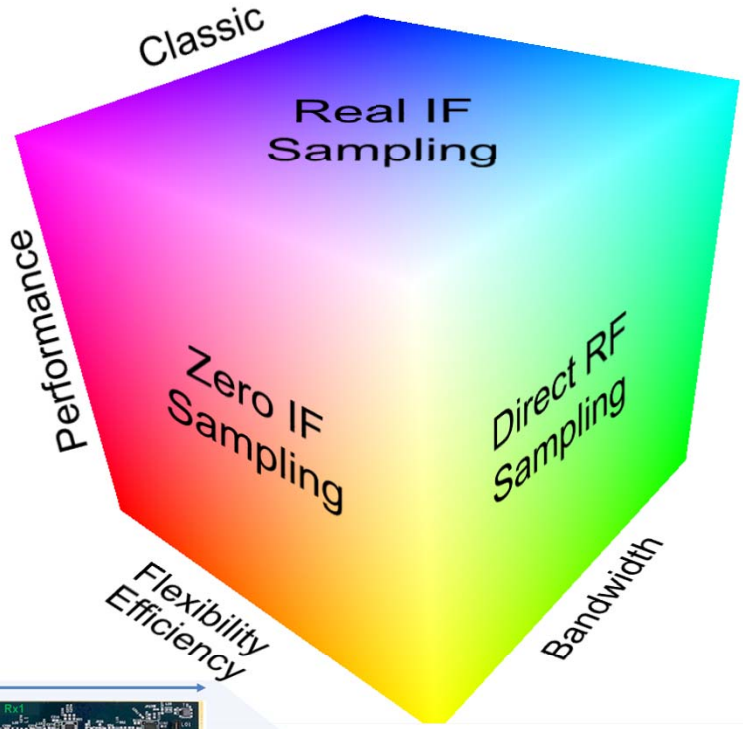


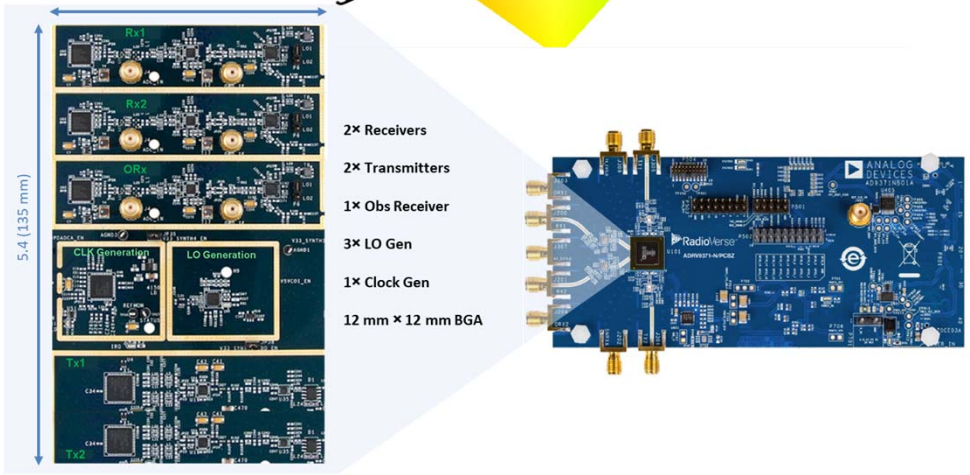
# The Right Architecture Choices



# The Right Architecture Choices

- Overwhelming choice of solutions for wireless designs
- Architecture must be carefully selected to achieve the desired goals. Each architecture comes with tradeoffs to be made.
  - RIF
    - Not flexible and requires a lot of filtering
  - Direct RF Sampling
    - Widest bandwidth but highest power
  - Zero IF
    - Most efficient with good performance, scalability & flexibility
- Small Cell & Massive MIMO requires an efficient solution. ZIF achieves:
  - 50% less system cost
  - 50% less system power
  - 67% smaller overall footprint

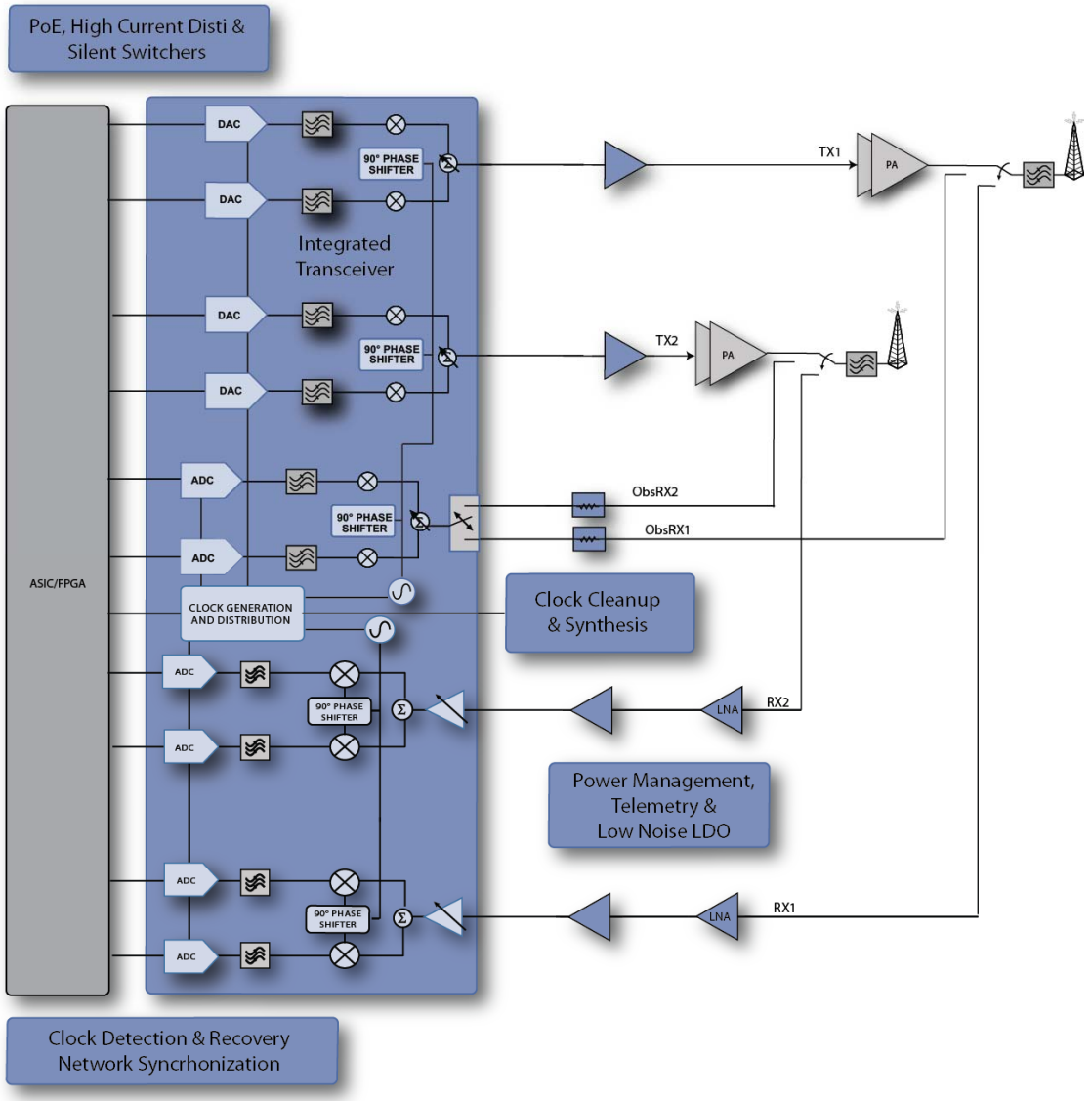


# Complete RF, Clock and Power Management

- RF Amplifiers complement the transceiver
- Transceiver enable the standard
- Power enables an efficient solution
- Clocking keeps the system synchronized and meeting performance.

RF signal chains work best when the components are designed to work together

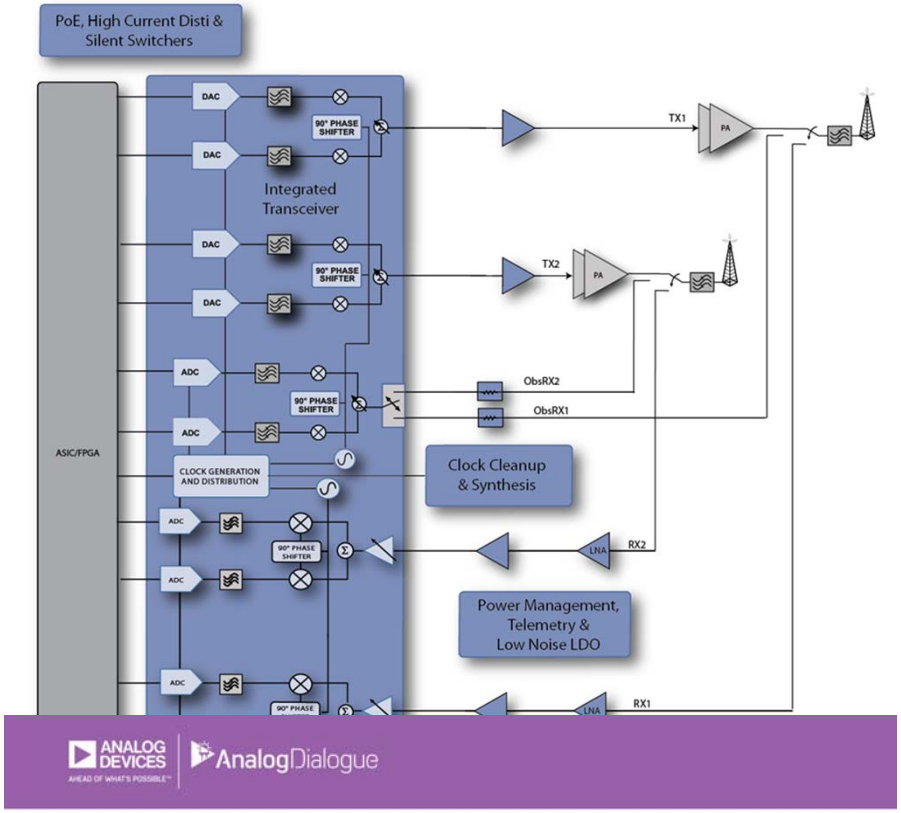


# The Right Architecture

- Configurable Radio technology platform
- Reduce the complexity of the RF design
- Architect the radio to reduce or eliminate bulky external components
- Leverage digital algorithms to improve performance of overall RF chain

Minimize Cost, Size,

Weight and Power




## Where Zero-IF Wins: 50% Smaller PCB Footprint at ⅓ the Cost

By **Brad Brannon**

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### Introduction

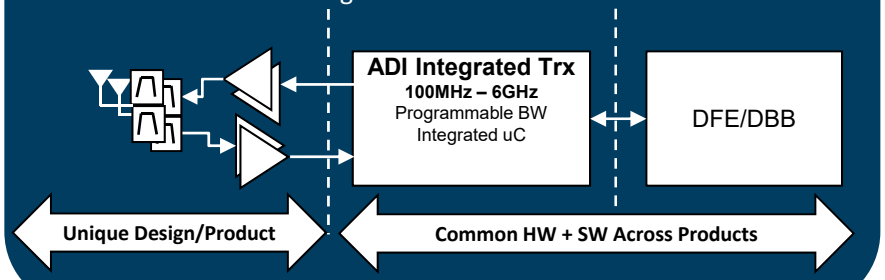
Zero-IF (ZIF) architecture has been around since the early days of radio. Today the ZIF architecture can be found in nearly all consumer radios, whether television, cell phones, or Bluetooth® technology. The key reason for this wide adoption is that it has proven time and again to offer the lowest cost, lowest power, and the smallest footprint solution in any radio technology. Historically, this architecture has been withheld from applications that demand high performance. However, with the demand for wireless growing around us and the rapidly crowding spectrums, a change is required in order to continue economically deploying radios in the infrastructure that and carrier aggregation leads to multiband radios. This all leads to more radios, with higher performance, requiring better out-of-band rejection, improved emissions, and less power dissipation.

While the demand for wireless is rapidly increasing, the power and space budgets are not. In fact, with an ever increasing need to economize both in power and space, reducing both the carbon footprint and the physical footprint are very important. To achieve these goals, a new perspective on radio architectures and partitioning is required.

# Wideband RF Transceiver Benefits

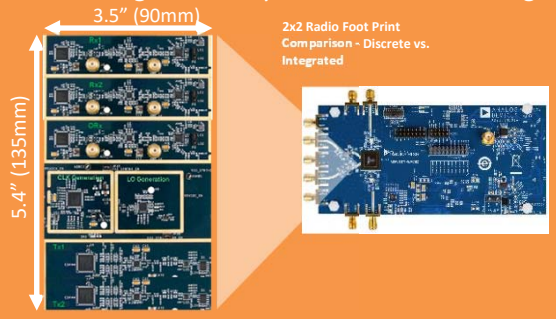
## Highly Reconfigurable

Enables reduced time to market through common HW & SW Small Signal Radio Platform




## Highest Level of Integration

Enables higher density radio architectures e.g. M-MIMO

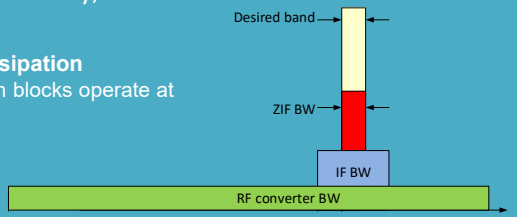



## Lowest Power Consumption

Reduce thermal density, enable lower SWAP radios

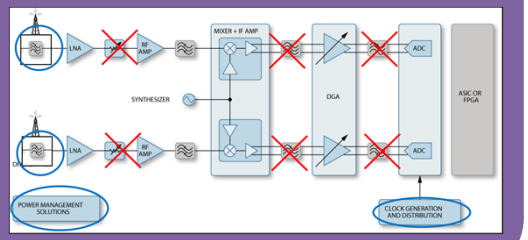
**Lowest possible power dissipation**

- Highest power consumption blocks operate at minimum bandwidth



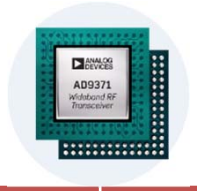

## Lowest System Cost

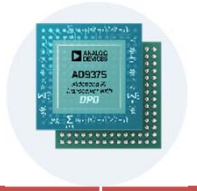
- Components such as IF filters are eliminated
- RF filters are simplified enabled by the elimination of out-of-band images or aliases



# RadioVerse ™ Portfolio



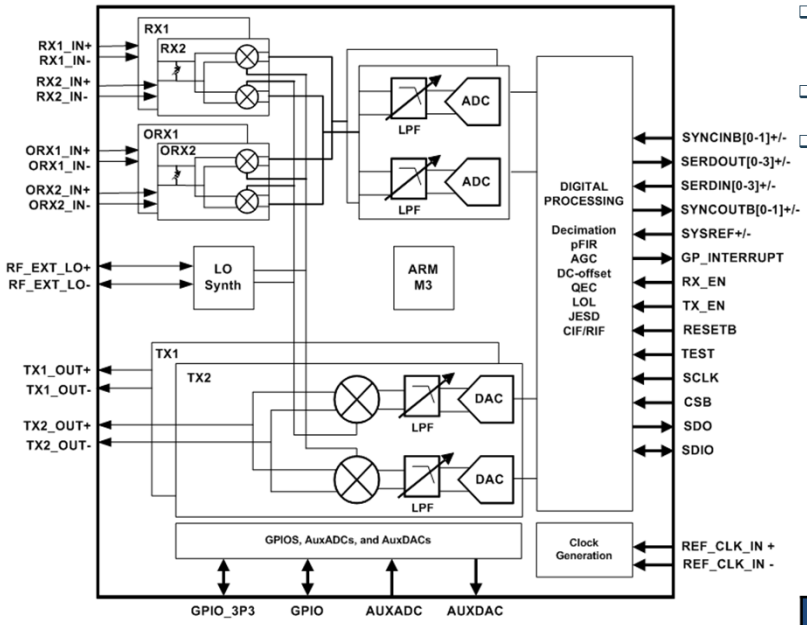


| Part # | Applications | Bandwidth | Functionality | RF Tuning Range | Rx Image Rejection* | Rx NF/IIP3** | Tx OIP3* | EVM | Package Size | Data Interface | DPD |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AD9361 | 3G/4G Picocell, SDR, Pt-Pt, Satcom, IoT Aggregator | 56 MHz | 2 Rx, 2 Tx | 70 MHz to 6 GHz | 50B | 3dB/-14dBm | +19dBm | -40 dB | 10 mm × 10 mm | CMOS/LVDS | N/A |
| AD9364 | 3G/4G Picocell, SDR | 56 MHz | 1 Rx, 1 Tx | 70 MHz to 6 GHz | 50dB | 3dB/-14dBm | +19dBm | -40 dB | 10 mm × 10 mm | CMOS/LVDS | N/A |
| AD9363 | 3G/4G Femtocell, UAV, Wireless Surveillance | 20 MHz | 2 Rx, 2 Tx | 325 MHz to 3.8 GHz | 50dB | 3dB/-14dBm | +19dBm | -34 dB | 10 mm × 10 mm | CMOS/LVDS | N/A |
| AD9371 | 3G/4G Macro BTS, Massive MIMO, SDR | 100MHx Rx, 250MHz Tx/ORx | 2Tx, 2Rx Orx & SnRx | 300 MHz to 6GHz | 75dB | 13.5dB/+22dBm | +27dBm | -40 dB | 12 mm × 12 mm | 6GHz JESD204B | N/A |
| AD9375 | 3G/4G Small Cell, 3G/4G Massive MIMO | 100MHx Rx, 250MHz Tx/ORx | 2Tx, 2Rx Orx & SnRx | 300 MHz to 6GHz | 75dB | 13.5dB/+22dBm | +27dBm | -40 dB | 12 mm × 12 mm | 6GHz JESD204B | Linearization BW up to 40MHz |
| ADRV9009 | Macro BTS, Massive MIMO, Active Antenna, Phased Array Radar, Portable Test Equipment | 200MHx Rx, 450MHz Tx/Orx | 2Tx, 2Rx | 100MHz to 6GHz | 75dB | 12dB/+15dBm | +27dBm | -43 dB | 12mm x 12 mm | 12GHz JESD204B | N/A |

* typical performance @ 2.6GHz
** typical performance @ 2.6GHz, AD9361 assumes internal LNA; AD937x and ADRV9009 no internal LNA.

# ADRF9009 1-Chip 5G TDD Transceiver

- **Integrated Dual Traffic Rx and Tx**
  - Tuning Range: 75MHz < Fc < 6GHz
  - TDD Operation only
- **Receivers**
  - Max Rx BW = 200MHz
- **Transmitters**
  - Max Tx BW = 450MHz
- **Integrated Observation Rx**
  - Max ORx BW = 450MHz
    - Shared inputs with Rx
- **Total Power (@ max bandwidth)**
  - Dual Rx = 3.5W
  - Dual Tx = 3.7W
  - Tx+ORx = 5.6W
- **Analog/Digital/Software Features**
  - 16bit ADC/DAC
  - Frequency Agility
  - LO phase synchronization
  - Rx: DC offset, QEC, AGC
  - Tx: QEC, LO leakage
  - Programmable FIRs
  - 12GSPS JESD204-B interface
  - Embedded ARM





## Applications

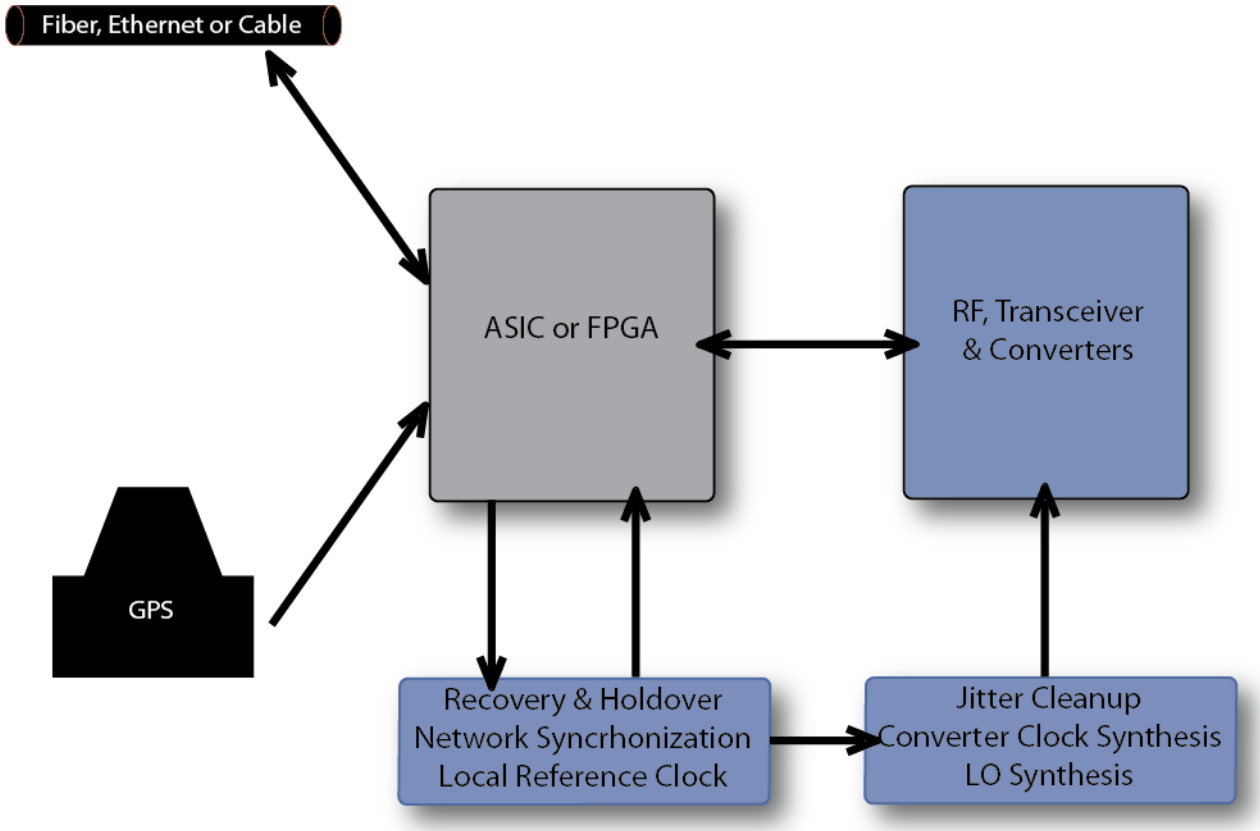
- COMS: MC-GSM, 3G/4G/5G Macro BTS, Massive MIMO
- ADEF: Radar, EW, MilCom, SigInt
- ETM: SDR, Portable Test Equipment

| Package | Interface |
|---|---|
| 12x12 BGA | 12G JESD204B |

# RadioVerse ™ Tools

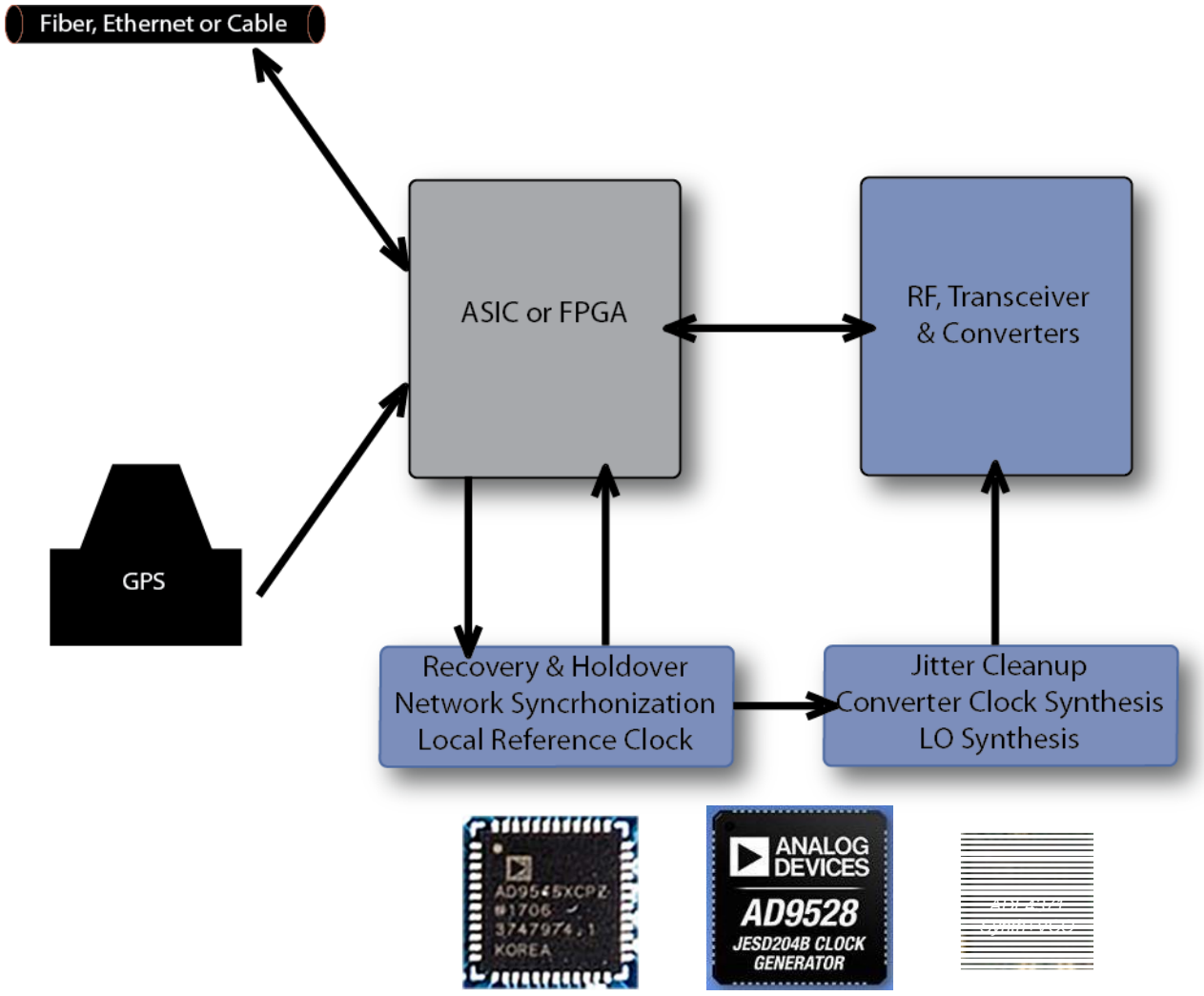
| | Cellular Comms | Aerospace & Defense | Wireless Video Transmission | SDR | IoT End Node, IoT Gateway |
|---|---|---|---|---|---|
| **Technology** | AD9361<br>AD9371<br>AD9375<br>ADRV9008/9 | AD9361<br>AD9364<br>ADRV9008/9 | AD9361<br>AD9363 | AD9361<br>AD9364<br>AD9371<br>ADRV9009 | ADF7030,<br>AD9361 |
| **Ecosystem & Tools** | Xilinx and Intel FPGA Carrier Platforms, Mathworks Matlab® Simulink® Models,<br>Eval Boards, Filter Wizard, Software Tools, PA tools, Prototyping Platforms, IoT Design Kits | | | | |
| **Partners** | Benetel, NXP, Skyworks, HJX, Nanosemi | Epiq, Ettus, Vadatech, Panateq | SIHID, Simpulse, Taisync, Longwo | Epiq, Ettus, Vanteon, HJX, Simpulse, Arrow, Panateq, Rincon | Simpulse, Vanteon |
| **ADI Reference Designs** | ADRV-DPD1 Small Cell Radio Reference Design | | | ADALM-Pluto<br>ADRV9361,<br>ADRV9364,<br>ADRV9009 SOM | |
| **3rd Party COTS** | | Epiq Sidekiq/Maveriq, VadaTech AMC597/VPX597/FMC214 | 4 wireless video/data link solutions based on AD936x | NI USRP series, ARRadio, Epiq Sidekiq M2/X2/X4 | Vanteon vPrisum, vChameleon |

# The Right ‘Time’



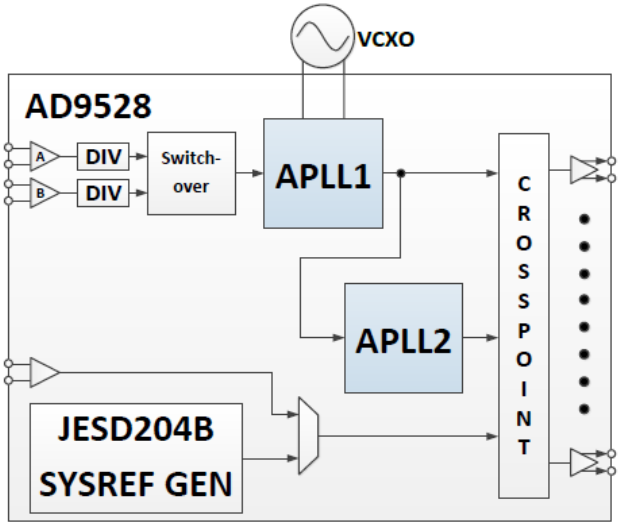

- Multi-source time reference
- Clock recovery, cleanup & holdover
- Local reference
- Low jitter synthesis
- System clock distribution

# The Right ‘Time’

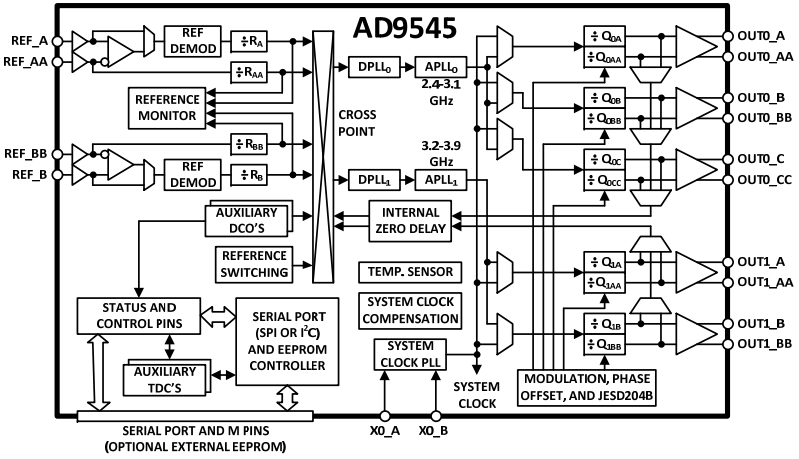


# Clock Solutions

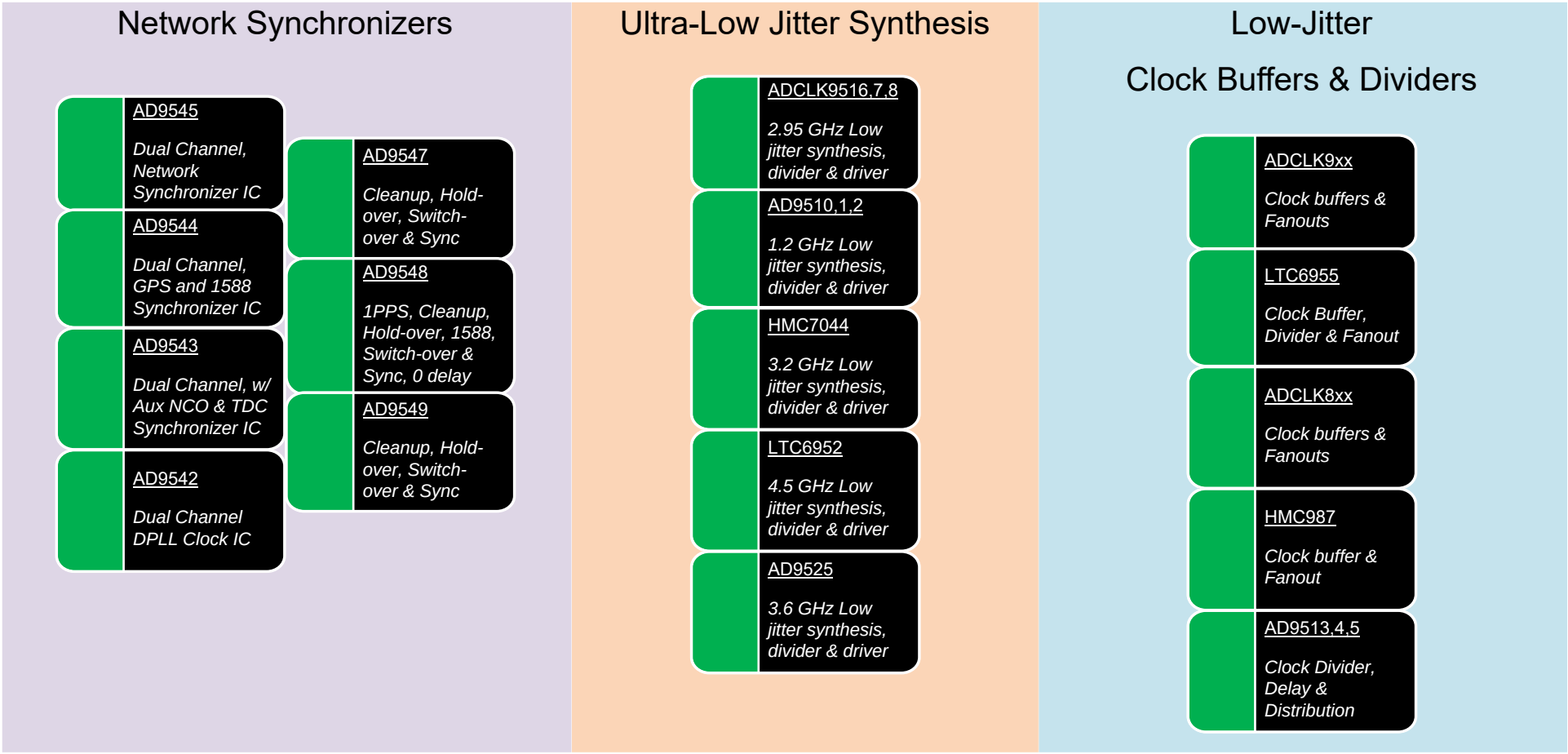
- Network clock recovery
- Low jitter synthesis
- Hitless switchover
- Temperature compensation on phase offset
- Hold over capability
- Low power consumption
- Capable buffering & distribution
- Connectivity between networking, baseband and RF Front Ends








# Clock Portfolio



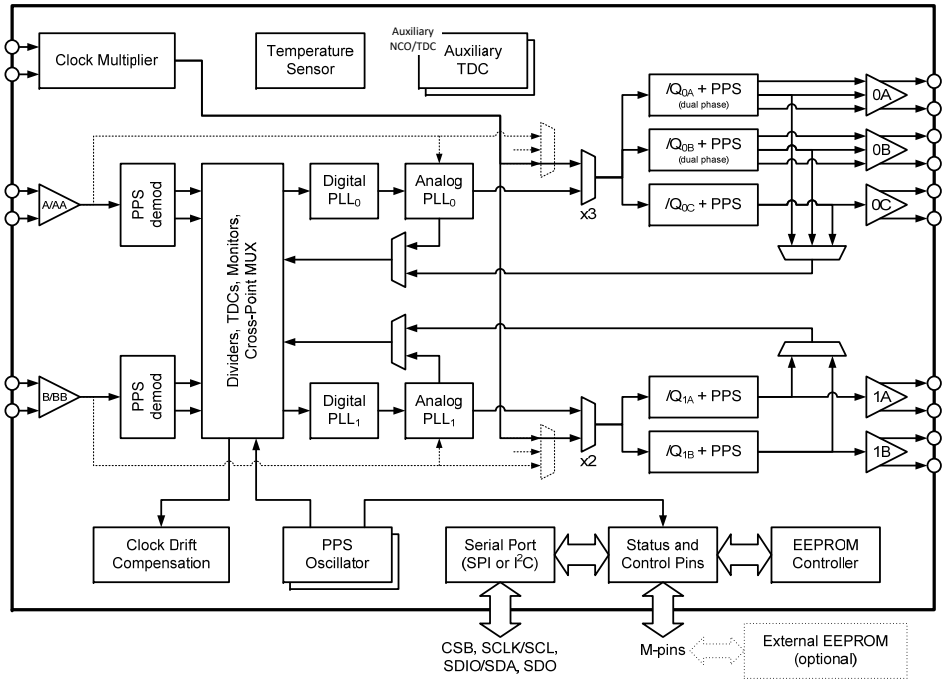
# AD9545 – Network Synchronizer & Adaptive Clock Translator

## Value Proposition

- GPS, IEEE1588v2, and Sync-E jitter cleaning and network synchronization
- Fast Locking in 1PPS (1Hz) Ref Input mode
- System Clock Stability Compensation
- DPLL's able to lock with Aux NCOs as inputs
- Jitter 210fs (12k – 20MHz)
- DPLL paired with Servo software to form 1588 solution

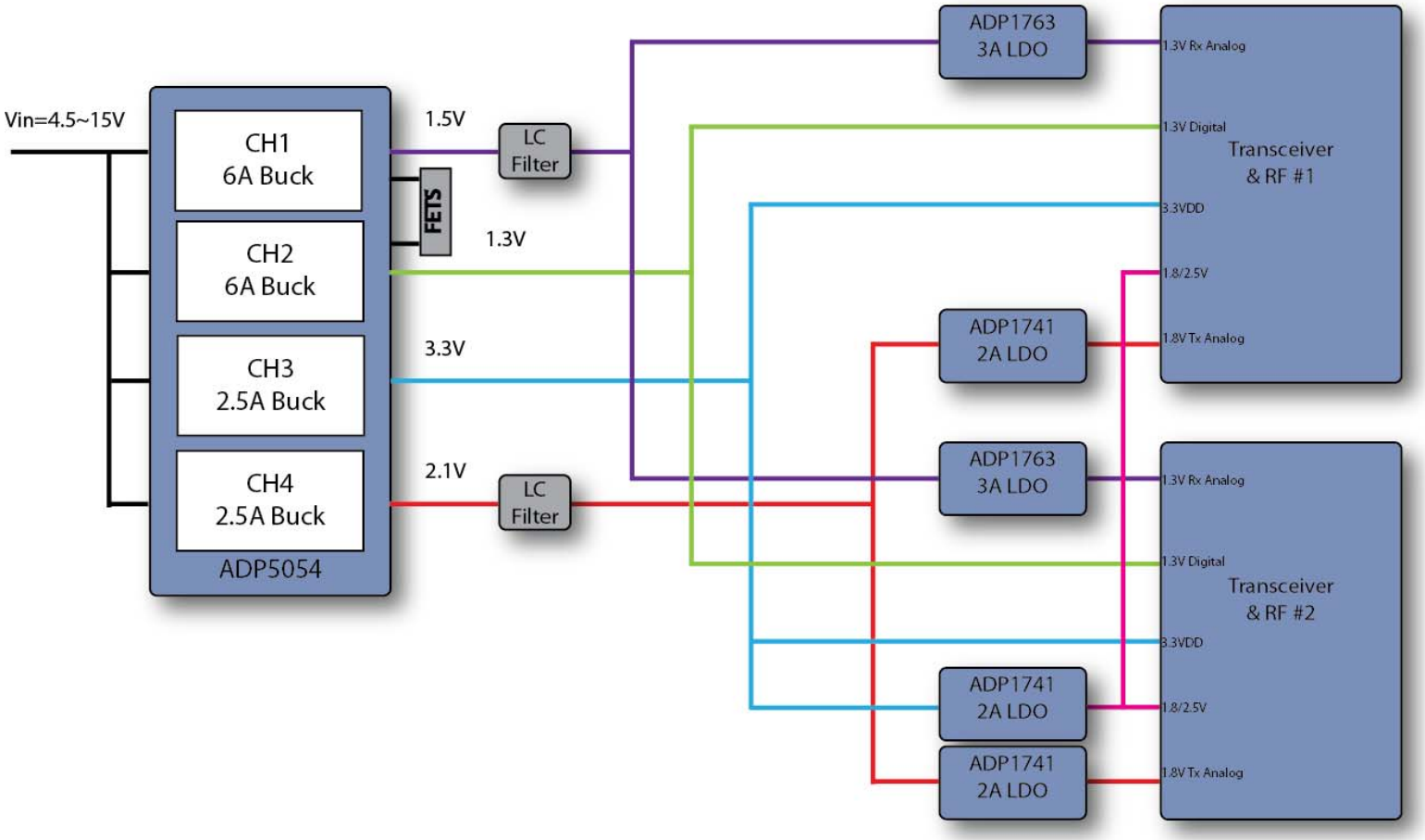
## Positioning

- Network Synchronizer Supporting:
  - IEEE 1588 support
  - SyncE
  - GPS 1PPS processing
- Aux NCOs/TDCs enable flexible configurations to adapt to various system architectures.
- WLS Apps – Baseband clocking, future RRH connected to packet switched Front Haul, e.g. eCPRI.
- WRD – Timing Cards in OTN, Switches




| Package | Status |
|---|---|
| 7x7mm<br>48 pin LFCSP | Released |

# The Right Power



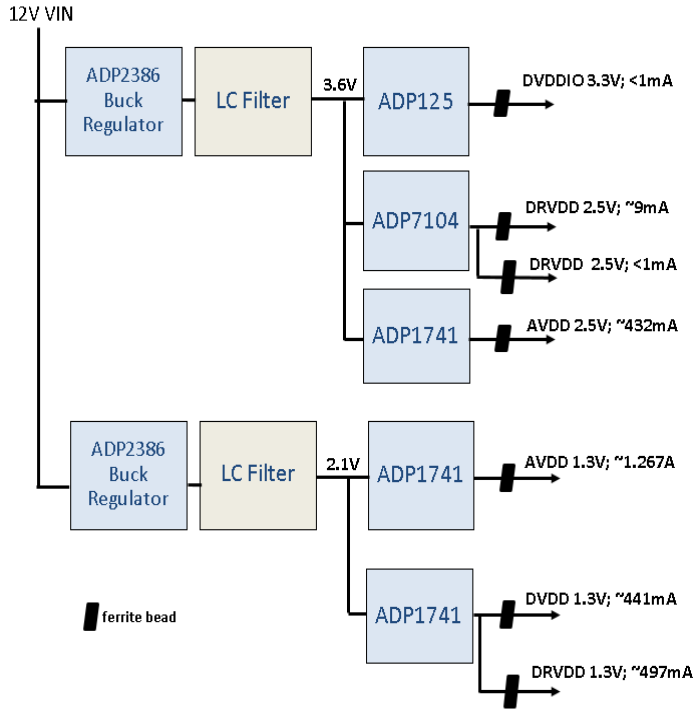

Excess Power = Money Wasted

A poorly designed power tree cost money to operate

~$1 / Watt / Year

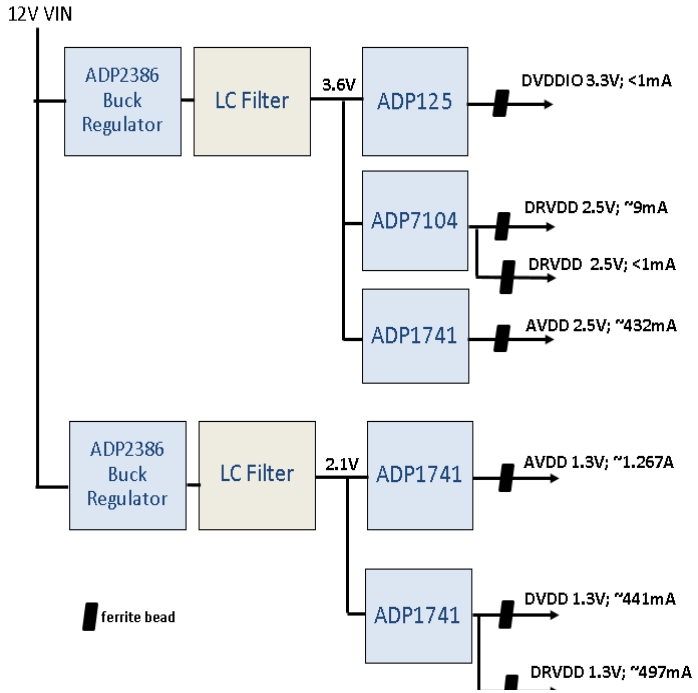
∴ An efficient power tree is key to minimizing operating cost

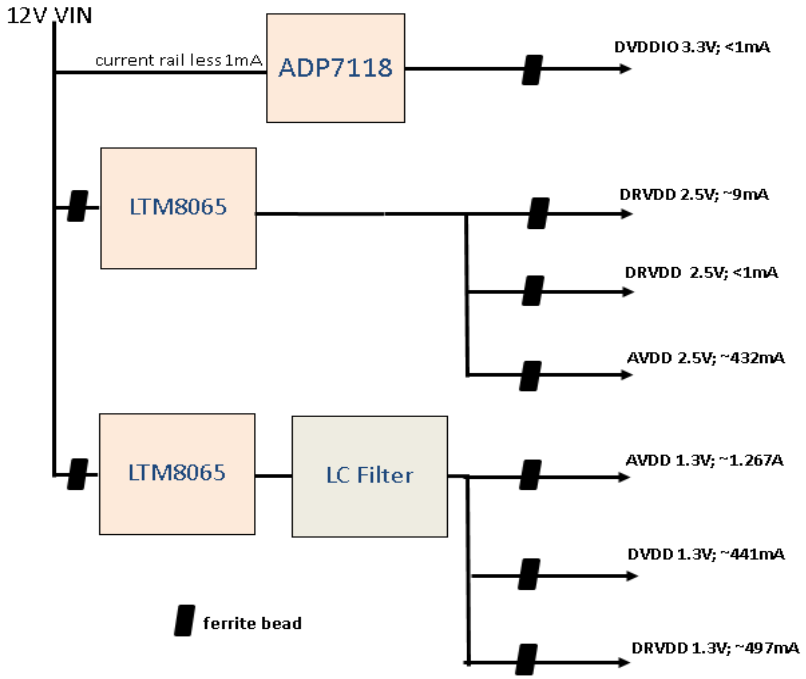
# Reference Design Study


- Great Performance
- 48% Power Efficiency
- Thermals Could Be Better
- Board Area Could Be Smaller

# An Optimal Power Solution




| Baseline Power Supply | | Voltage (V) | Current (A) | Power (W) |
|---|---|---|---|---|
| PIN | | 11.729 | 0.676 | 7.929 |
| POUT | AVDD_1.3V | 1.268 | 1.222 | 1.549 |
| | DRVDD_1.3V | 1.301 | 0.521 | 0.678 |
| | DVDD_1.3V | 1.305 | 0.406 | 0.530 |
| | AVDD_2.5V | 2.589 | 0.408 | 1.056 |
| | DRVDD_2.5V | 2.590 | 0.0047 | 0.012 |
| | DVDD_2.5V | 2.590 | 0.0001 | 0.0003 |
| | DVDDIO_3.3V | 3.301 | 0.0004 | 0.0013 |
| | | | POUT TOTAL: | 3.827 |
| | | | **Efficiency (%):** | **48.26** |

| LTM8065 Version 2 | | Voltage (V) | Current (A) | Power (W) |
|---|---|---|---|---|
| PIN | | 11.885 | 0.442 | 5.256 |
| POUT | AVDD_1.3V | 1.303 | 1.308 | 1.704324 |
| | DRVDD_1.3V | 1.302 | 0.531 | 0.691 |
| | DVDD_1.3V | 1.305 | 0.459 | 0.599 |
| | AVDD_2.5V | 2.486 | 0.440 | 1.094 |
| | DRVDD_2.5V | 2.494 | 0.005 | 0.012 |
| | DVDD_2.5V | 2.496 | 0.0001 | 0.0002 |
| | DVDDIO_3.3V | 3.301 | 0.0004 | 0.0013 |
| | | | POUT TOTAL: | 4.102 |
| | | | **Efficiency (%):** | **78.05** |

# An Optimal Power Solution

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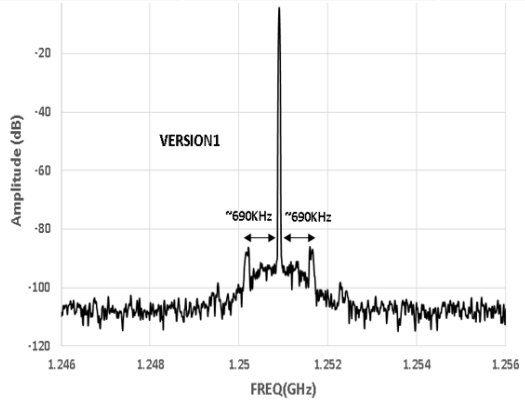
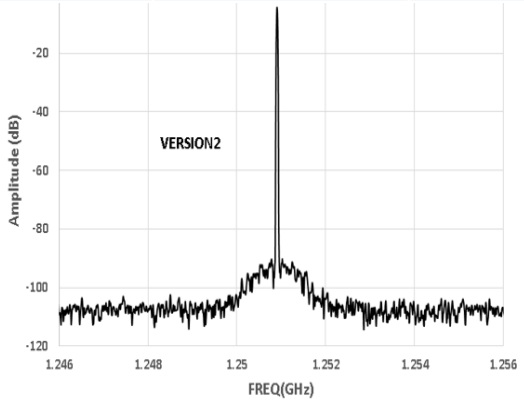
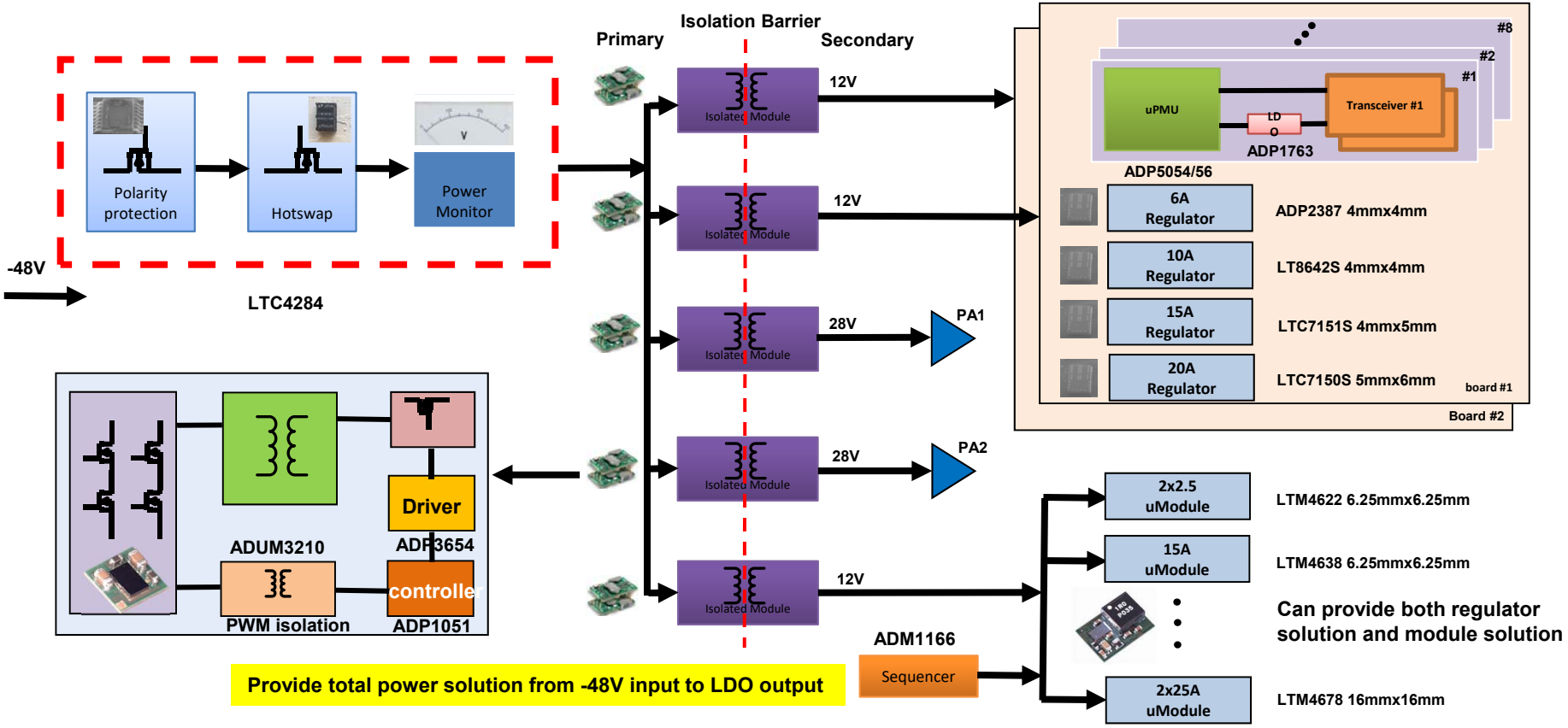
| | | | POUT TOTAL: | 4.102 |
| | | | **Efficiency (%):** | **78.05** |

| AD9625-2.6 GHz Dynamic Performance | | | | |
|---|---|---|---|---|
| Input Frequency (MHz) | SNRFS (dB) | | SFDR (dBc) | |
| | Baseline Power Supply | LTM8065 Version 2 | Baseline Power Supply | LTM8065 Version 2 |
| 729 | 57.01 | 57.01 | 79.87 | 80.11 |
| 1346 | 56.53 | 56.54 | 78.41 | 80.77 |



# The Right Power

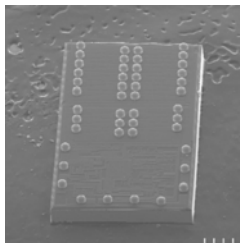


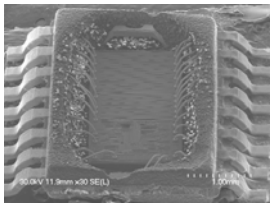

Big savings in a small part of the design scales across the design

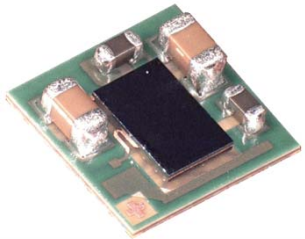
Smart power design in the full system reduces temperature & save money

Without Sacrificing Performance!!!

# Power shouldn’t be an afterthought








**100A**

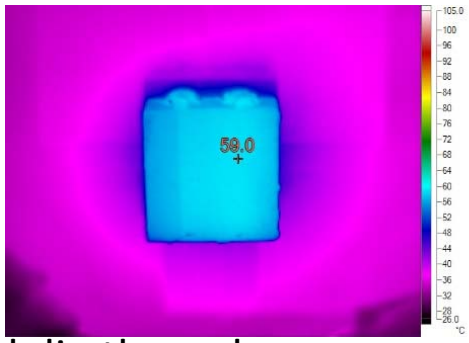
**1 x LTM4700 with *Digital Telemetry***

**(July 2018)**

**100A**

**12 x LTM4601**

**(5 years ago)**




- Power solutions available in all levels of packaging from bumped die through application specific modules.
- Power technology is evolving as fast as signal chains
- Power solutions should be a key part of efficiency and thermal management

# The Right (Smart) Partition


- Algorithm placement has a big impact on total resource required
- Algorithms in the FPGA/ASIC
  - Too many algorithms in the FPGA/ASIC increases the interface requirements
  - Too many algorithms in the FPGA reduces overall efficiency and increases cost & power
- Algorithms in the radio
  - Placing the right algorithms in the radio can significantly reduce the interfacing requirements (8 lanes to 4 lanes saving 600 mW on 2T2R)
  - Algorithms in the radio improve efficiency & performance (1/10$^{th}$ the power or 900 mW savings on 2T, tighter loops)
  - Algorithms in the radio free up space in the FPGA for other functions or smaller FPGAs; lower cost!

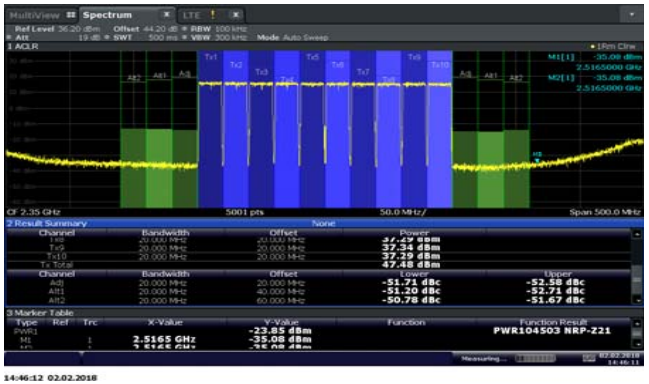
# Algorithm Partitioning

- Higher modulation order and new PA materials require more sophisticated algorithms
  - Modulation orders continue to increase towards 256QAM driving demand on EVM
  - New amplifiers like GaN introduce new errors like charge trapping which can impact inband EVM but not ACLR requiring more complicated DPD models.
- Algorithms must balance the tradeoffs between performance and implementation cost
  - A practical DPD must effectively operate under dynamically varying signal conditions.
  - Accounting for the range of conditions is a tradeoff in chip area vs. computation power and memory size vs. the number of pre-calculated models.
- Algorithms must balance complexity without negatively impaction system cost, power or performance
  - Increasing bandwidth and demands for improving efficiency are driving complexity.
  - Algorithms must carefully balancing the tradeoff between linearity and efficiency.
- Algorithms must provide stability, robustness and broad ranging protection
  - Effective algorithms must be adaptive and protect against multiple pathologies that could impact performance and reliability including PA failure.
  - Algorithms must be robust enough for a wide range of operating conditions and yet remain stable.

- **The best way to accomplish this is to integrated radio centric algorithms directly into the radio**
  - **Direct RF ASIC implementation offers the smallest die area, lowest power & lowest cost**
  - **Algorithms associated with radio operation and performance are best implemented within the radio to reduce latency and minimize the number of control loops in the system.**

100MHz: Commercial PA1

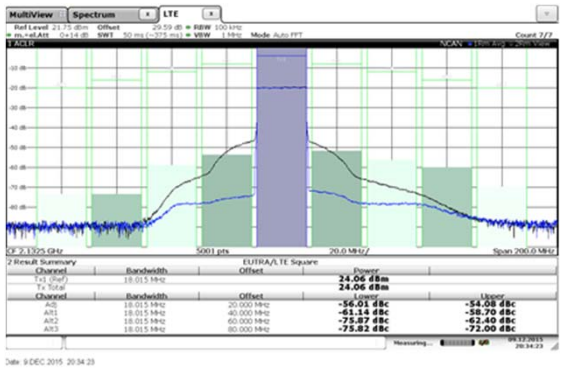
200MHz: Commercial PA 2



# AD9375 Small Cell Reference Design

## (With DPD)

- Single 12V supply. Total dissipation <10W. Full power management included.
- Contains all components: transceivers, PAs, LNAs, filters, power solution
- Small Form Factor: 83mm x 88mm
- Broadband design. BOM covers band 7; other bands achievable by BOM change.
- High efficiency PA SKY66279 (29% PAE)
- 2x2 20 MHz LTE, ¼ Watt
- ACLR <-54 dBc typical @ 24 dBm Pout



- Please visit analog.com/radioverse for more information and full reference design support (HW, SW, configuration)

# Conclusion

- Roll out of 5G (FR1 & FR2) will require significant amounts of new hardware throughout the network.
- This new hardware must be properly partitioned and requires careful consideration of integration.
- Partitioning and architectures chosen will greatly impact power consumption.  A proper architecture will facilitate the lowest system power.
- Minimizing cost is about looking at the overall solution to find the right partition and architecture to minimize solution cost.
- RF Performance is optimized by selection of components and algorithms that are designed to work together.