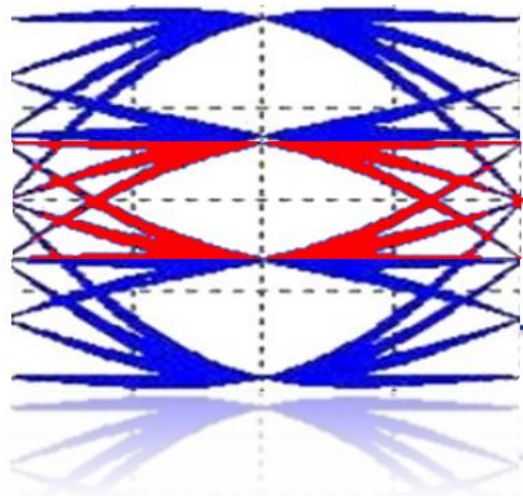


56Gb/s 4-pulse amplitude modulation signal integrity design key points

Zhang Ying, Sugon SI
zhangying@sugon.com

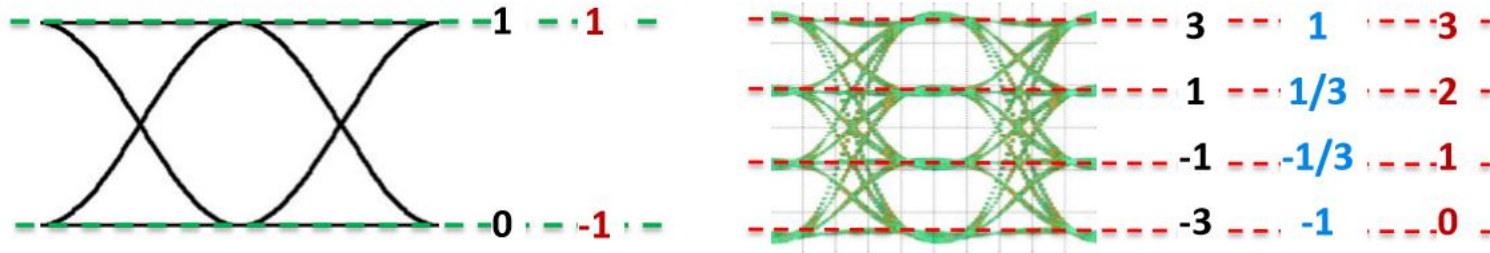
Outline



- 56G PAM4 Signal Characteristics
- BGA Field Optimization
- Routing Line
- Compensate Method
- Others
- Case sharing

56G PAM4 Signal Characteristics

- ✓ PAM4 : 1 symbol, 2 bits, 3 eyes, 4 levels and Sensitive



- ✓ PSD: $SPAM4(f) = 10 \cdot \log_{10} (abs(sinc^2(2f/DataRate)))$
- ✓ $f_{Nyquist} = 56/4 = 14$ GHz

◆ Advantages: Bandwidth

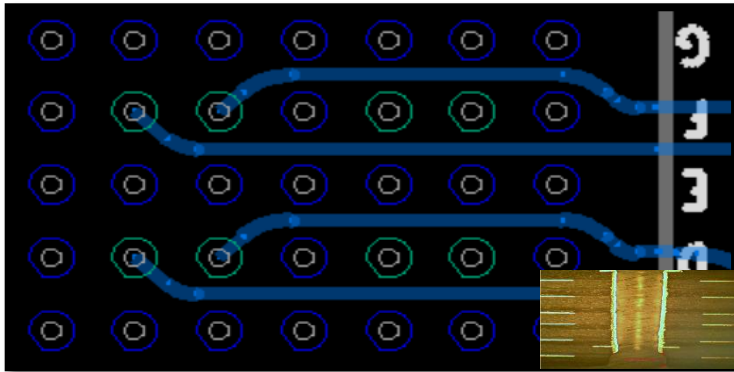
- Reduced Loss Requirements
- Link Topology Diversity
- Cost Reduction

◆ Disadvantages: SNR

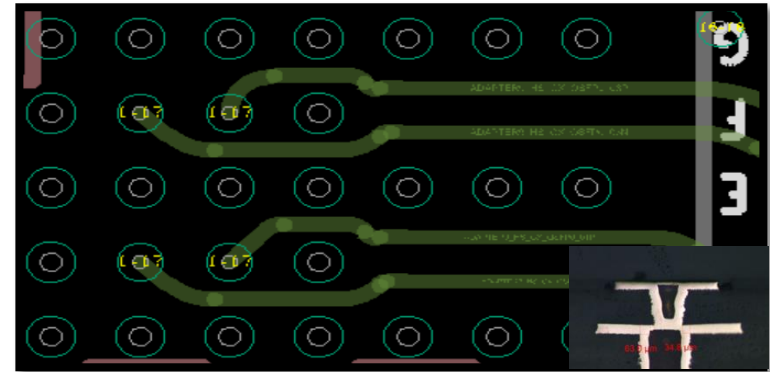
- Reflection
- Crosstalk
- Mode Conversion
- Three vertical eyes are asymmetrical

BGA Field

- Layout:



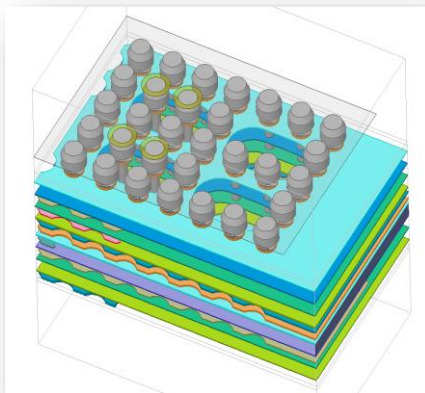
VS



Thru hole + Backdrill + SE line

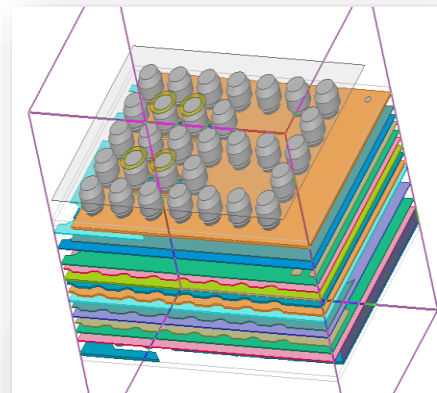
HDI process+ DF line

- Result:



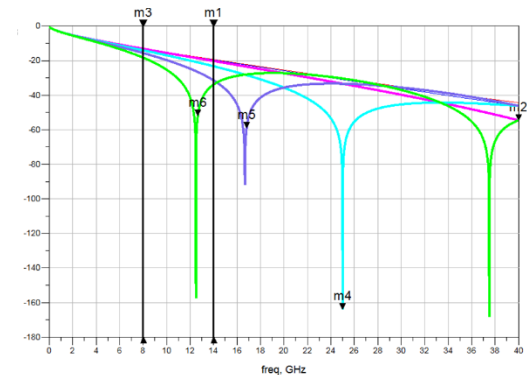
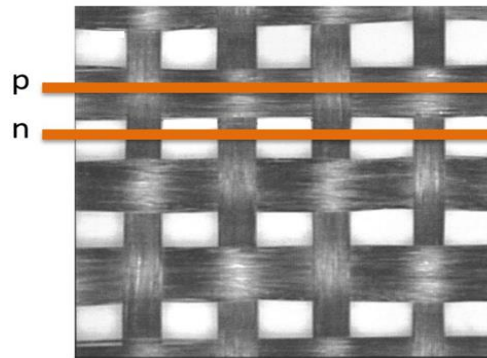
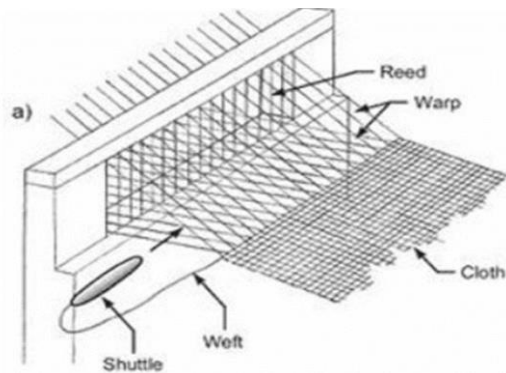
0 Stub — Impedance continuity,
reduce Reflection

DF Line — Reduce Xtalk & Mode
conversion & EMI influence



Routing Line

- Stripline & Pin map & Layer distribution
- Inner pair skew (rotation & stackup design)



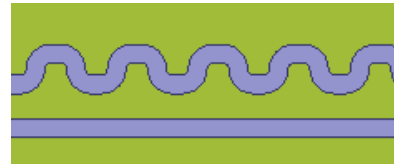
- TX/TX&RX/RX or TX/RX spacing (NEXT/FEXT control)
- Conductor Bends (Radiation reduction)
- Keep distance from other Nets & Vias (Noise avoid)
- GND vias shielding (Be careful)
- Return path complete and clean (Reference plane distance & Xtalk)

Compensate Method

- Compensation Continuity & Compensation Efficiency



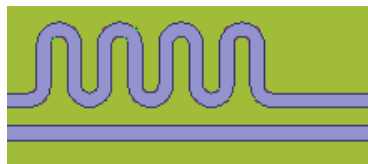
0x0



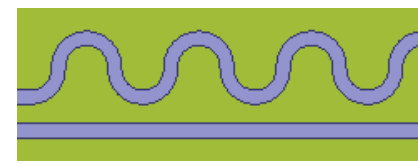
1x1



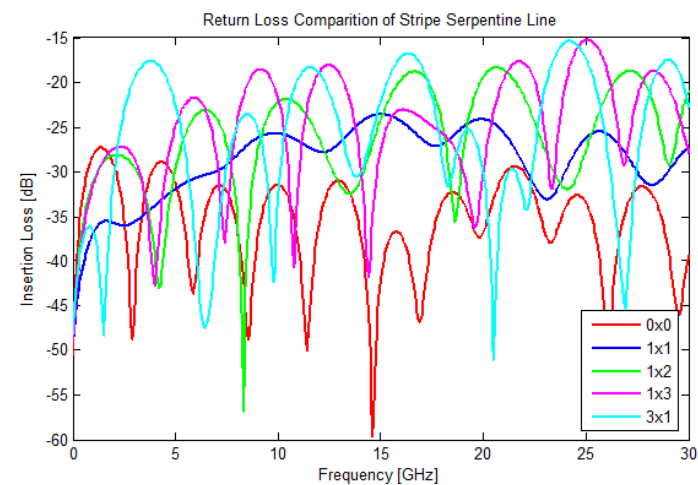
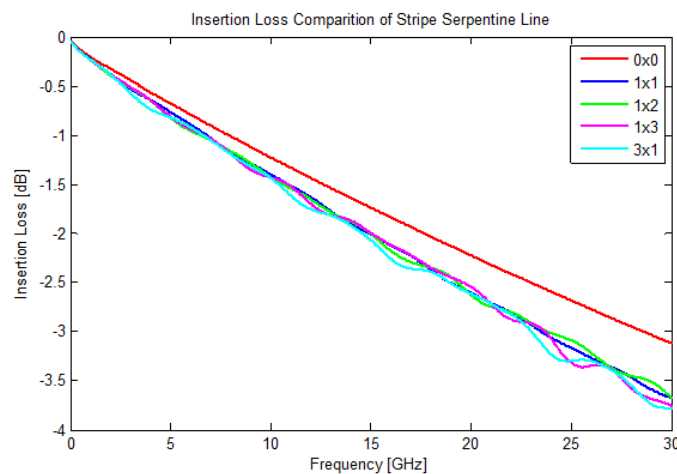
1x2



1x3

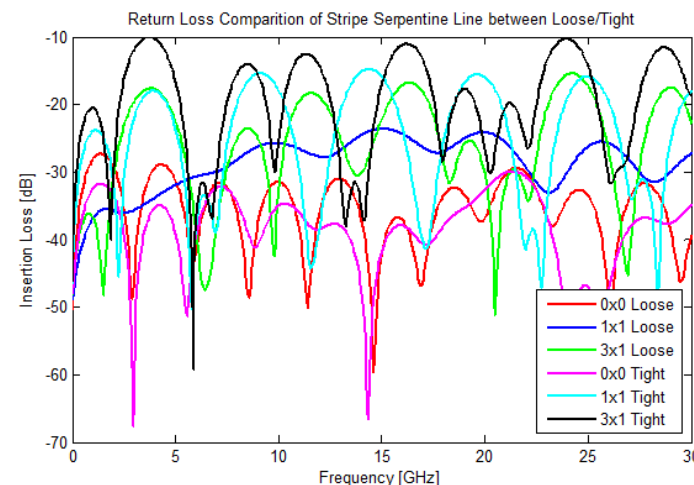
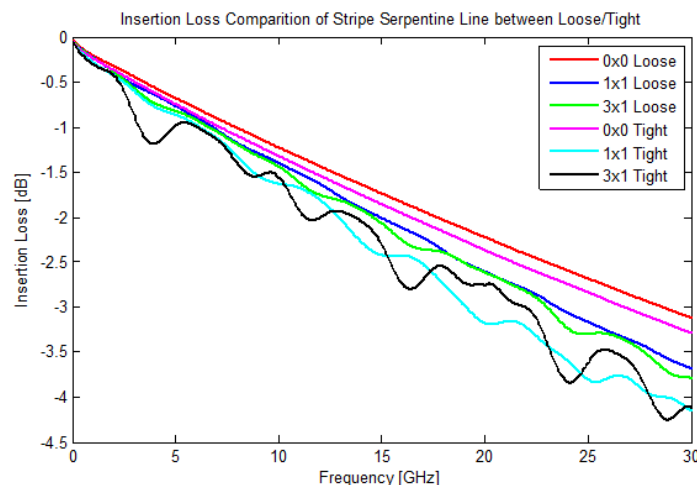


3x1

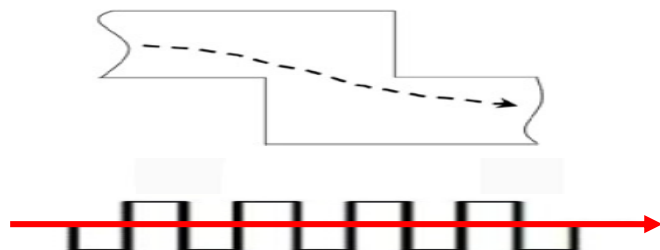


Compensate Method

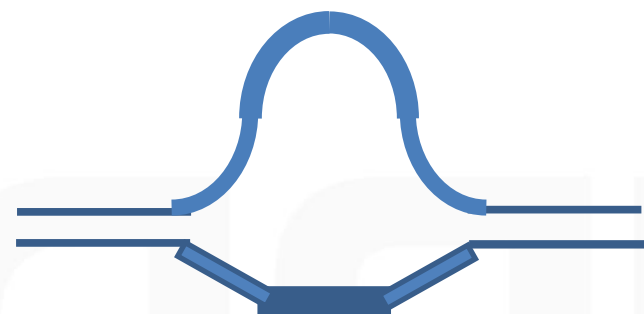
- Loosely coupled differential design



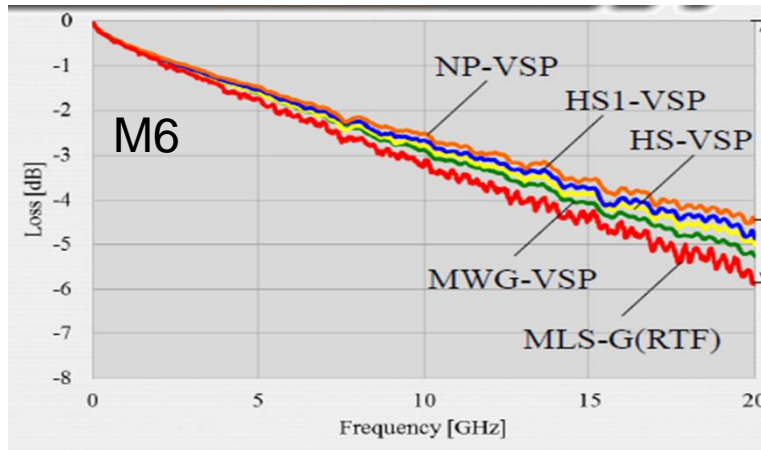
- The purpose of compensation is **isochronous transmission** rather than physical length.



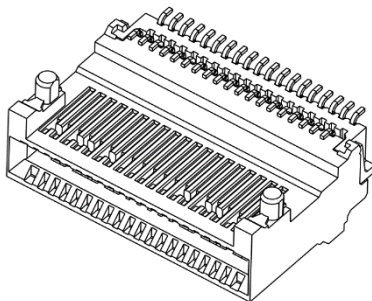
- Increasing Linewidth and Optimizing Impedance



- Stackup design consideration (Material & Copper & h)



- CNT choose and optimization



- Package
- Performance
- Pin delay
- Antipad opt.
- cost

- POFV process

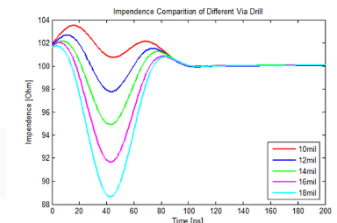
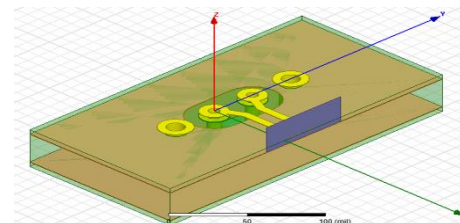
- Solve the problem of insufficient design space
- Shorten discontinuous structure
- Need to pay attention to the **processing reliability**

- PCB & PCBA Production

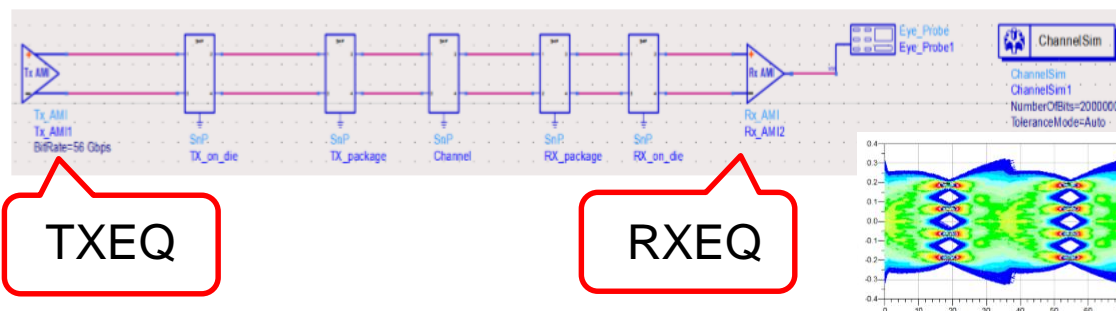
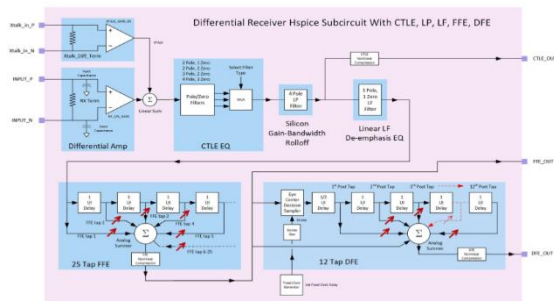
- Accuracy & Reliability

- Via / CAP optimization (Z target)

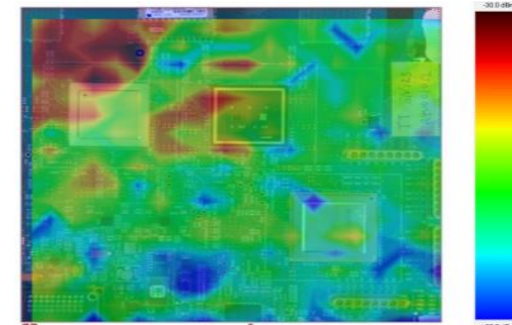
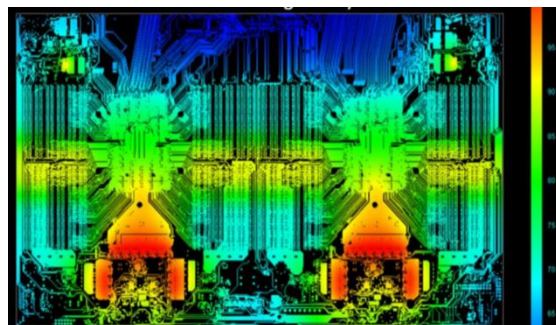
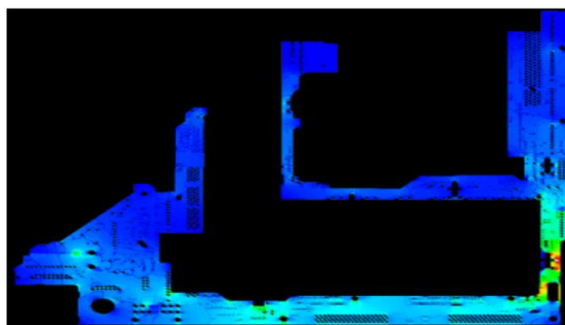
- Return path & Antipad variation



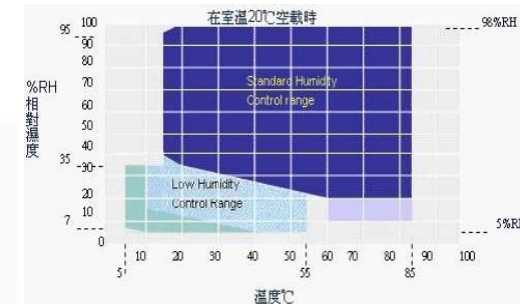
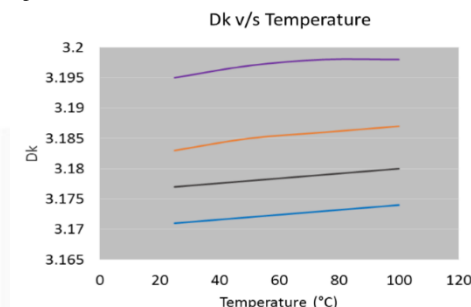
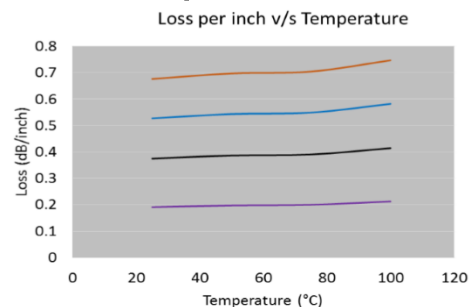
● Chip Part & SERDES parameters tuning



● Power & Thermal & EMI Co Influence

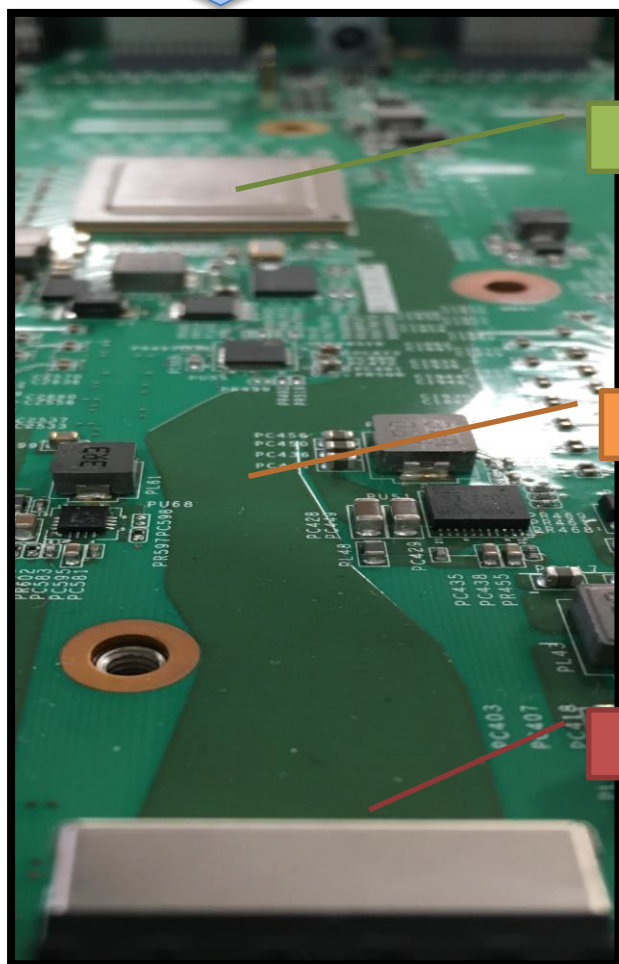


● Temperature & Humidity Influence



Case sharing

200G Board:



Chip

Line

CNT

Link Test Result:

Send Buffer on HOST (H) and Receive Buffer on HOST (H)

Size Bandwidth (MB/s)

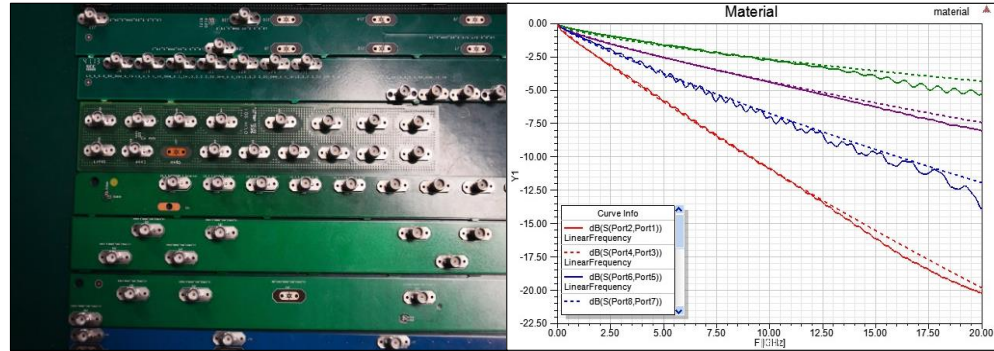
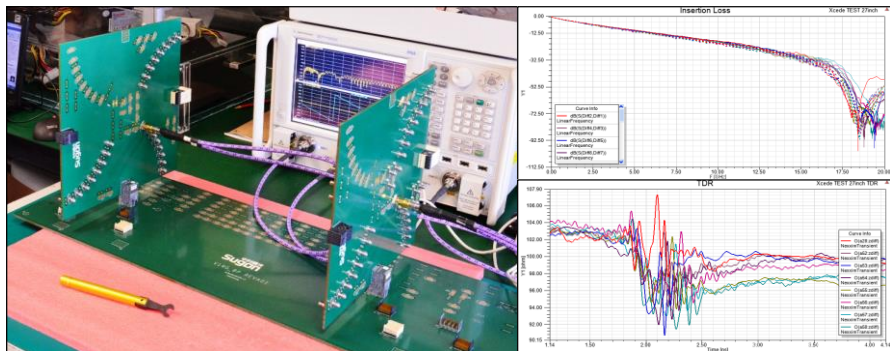
1	3.45
2	6.93
4	14.01
8	28.38
16	57.93
32	116.53
64	231.87
128	448.00
256	799.28
512	1374.63
1024	1887.92
2048	2852.19
4096	4388.39
8192	5386.34
16384	5888.36
32768	8826.55
65536	19074.26
131072	19007.71
262144	19305.81
524288	19733.70
1048576	20435.66
2097152	22406.60
3145728	21459.43
4194304	24499.62
5242880	24512.87
6291456	24511.64
7340032	24519.45
8388608	24523.30

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Sugon SI Lab



Server

Storage

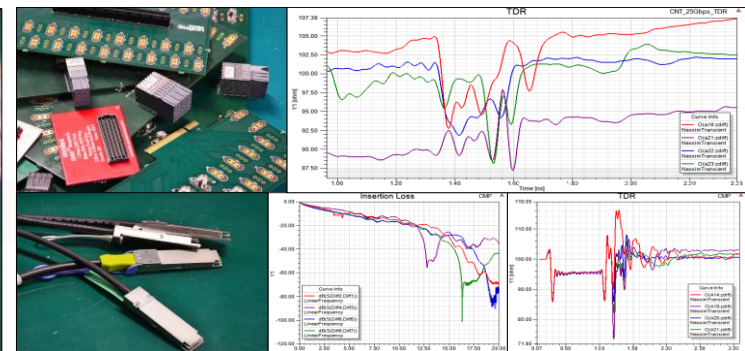
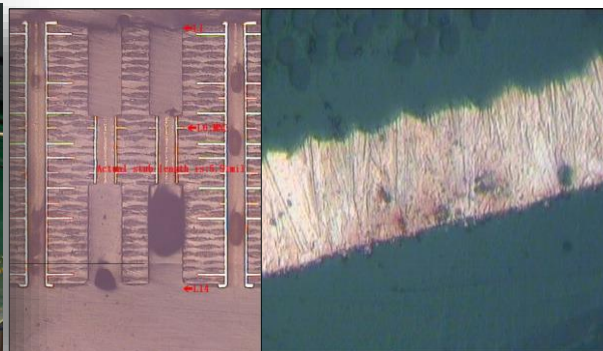
HPC



Cloud

Data Center

Security



Summary

- The ideal 56G PAM4 design is signal links are continuous and symmetrical and transmit in an ideal environment.
- In order to be close to the ideal, design needs focus on:
 - Stackup design
 - Special production process
 - Optimization of discontinuous structure
 - Noise
 - Mode conversion
- The design points included in this article are comprehensive and thorough, that can be used as a design guide for 56G or other project.