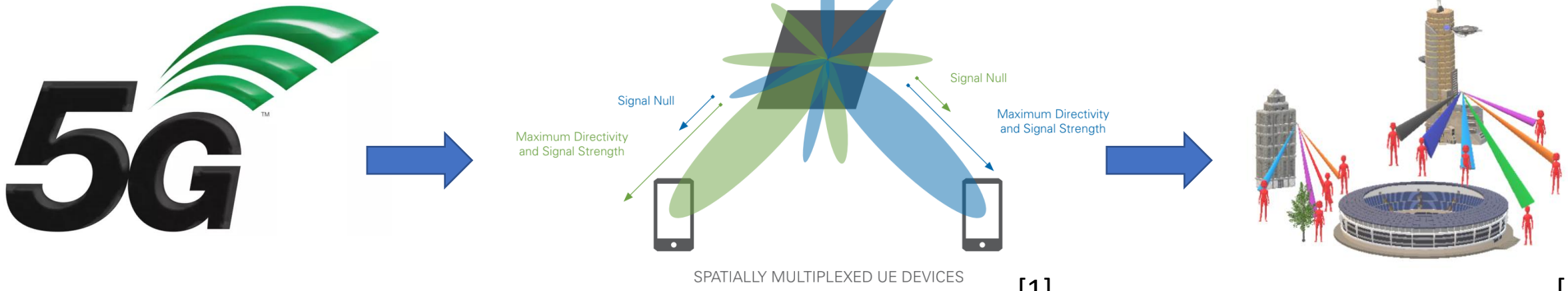
Mini-Circuits®
ISO 9001 ISO 14001 AS9100 Certified

Advances in High Frequency Packaging

April 2019

LEVERAGING OUR SUCCESS

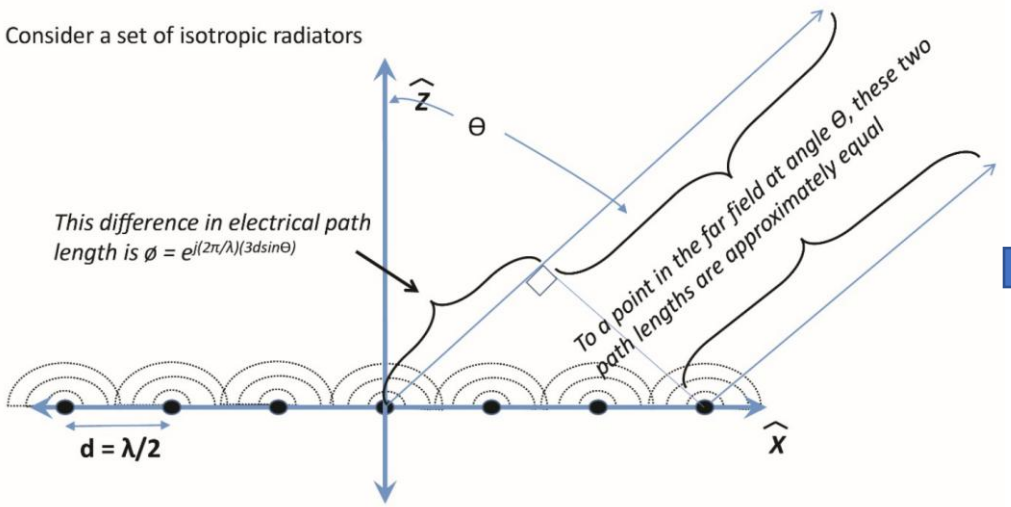
Motivation



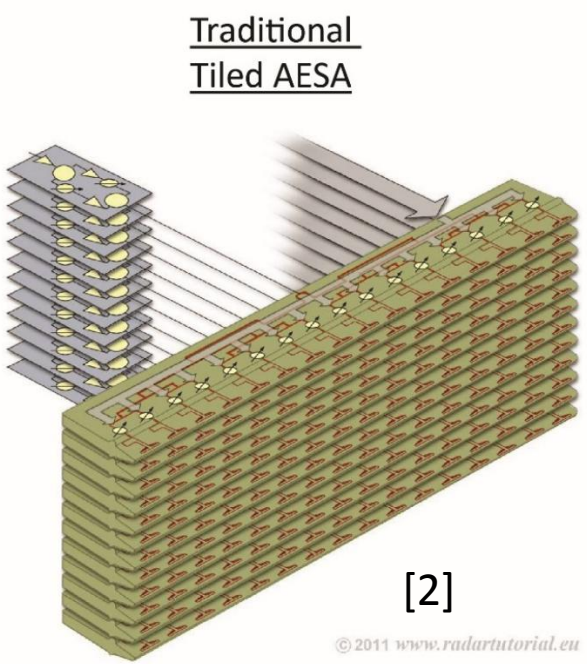
[1] [1]

- Expected global mobile data usage to grow from 11.2 (back in 2017) to 48.3 Petabytes/month (in 2021)
- Rethinking of mobile data access is required and 5G has emerged as a strong proposal to achieve a 1000X increase in mobile data capacity connecting 7 billion people and 7 trillion devices required to be energy efficient and almost zero downtime
- 5G is aiming to employ phased arrays as a mean to direct beams in specific directions and this is necessary because backhaul and access links will share the same air channel, so all network elements (BS, Aps, Ues) will inevitably require directional, steerable antennas for spatial aggregation

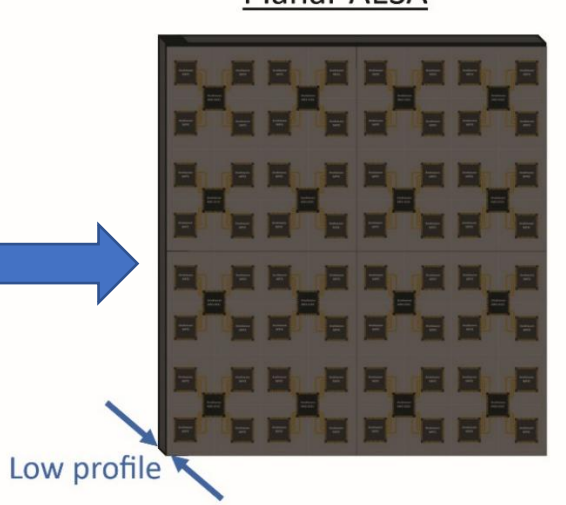
Motivation



[2]



[2]

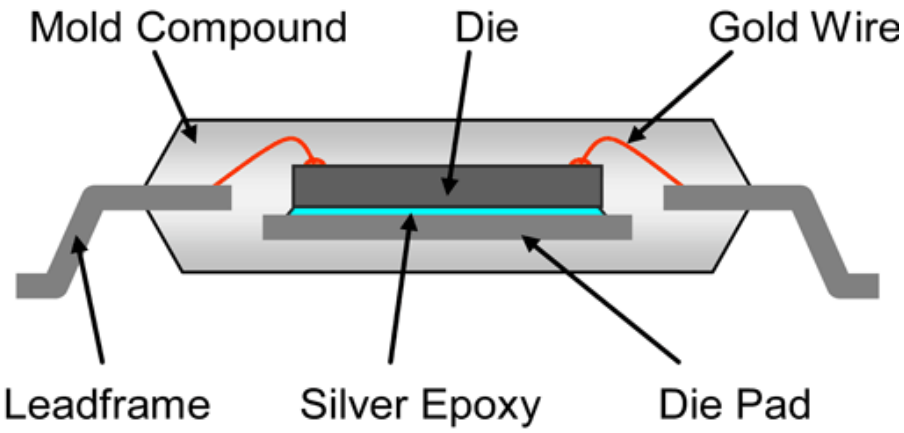


[2]

- Active Electronically Scan Array (AESA) constitute a kind of phased array architecture where there is a T/R module per antenna element
- Those T/R modules will eventually require some sort of packaging and this is going to be challenging because of the space constraints imposed by the “Lattice Spacing” which determines among others, the maximum beam steering angle or “field of view”
- Lattice spacing sets the packaging density in the array, influencing mainly the cross-coupling between circuits and thermal dissipation properties of the assembly

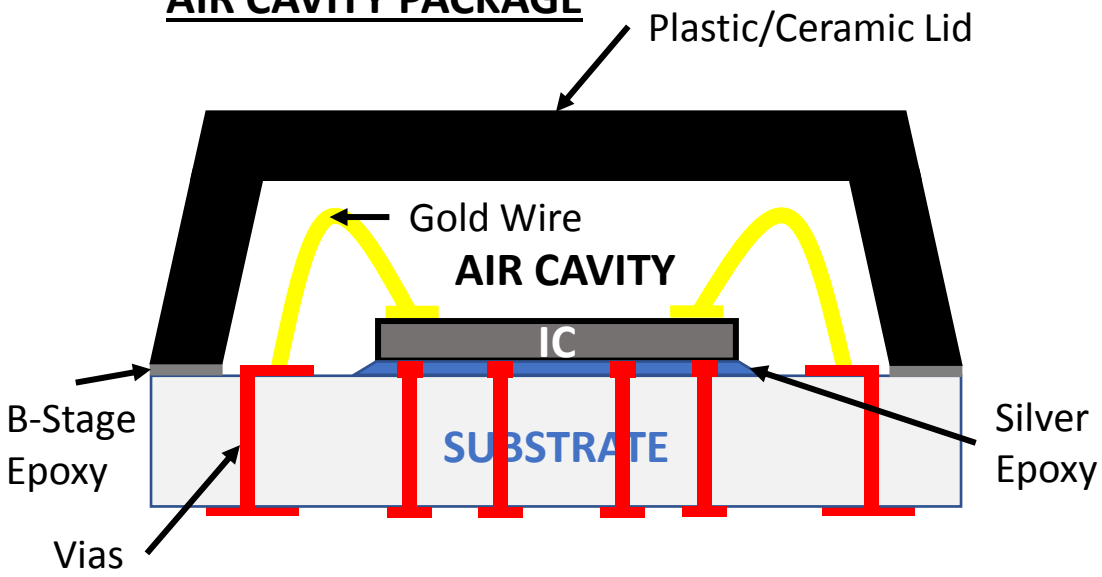
Molded vs Air-Cavity Packaging

MOLDED PACKAGE



- Very mature technology
- Very low cost
- High losses, high parasitics
- Not suitable for packaging ICs with air bridges
- Not suitable for mmWave applications

AIR CAVITY PACKAGE

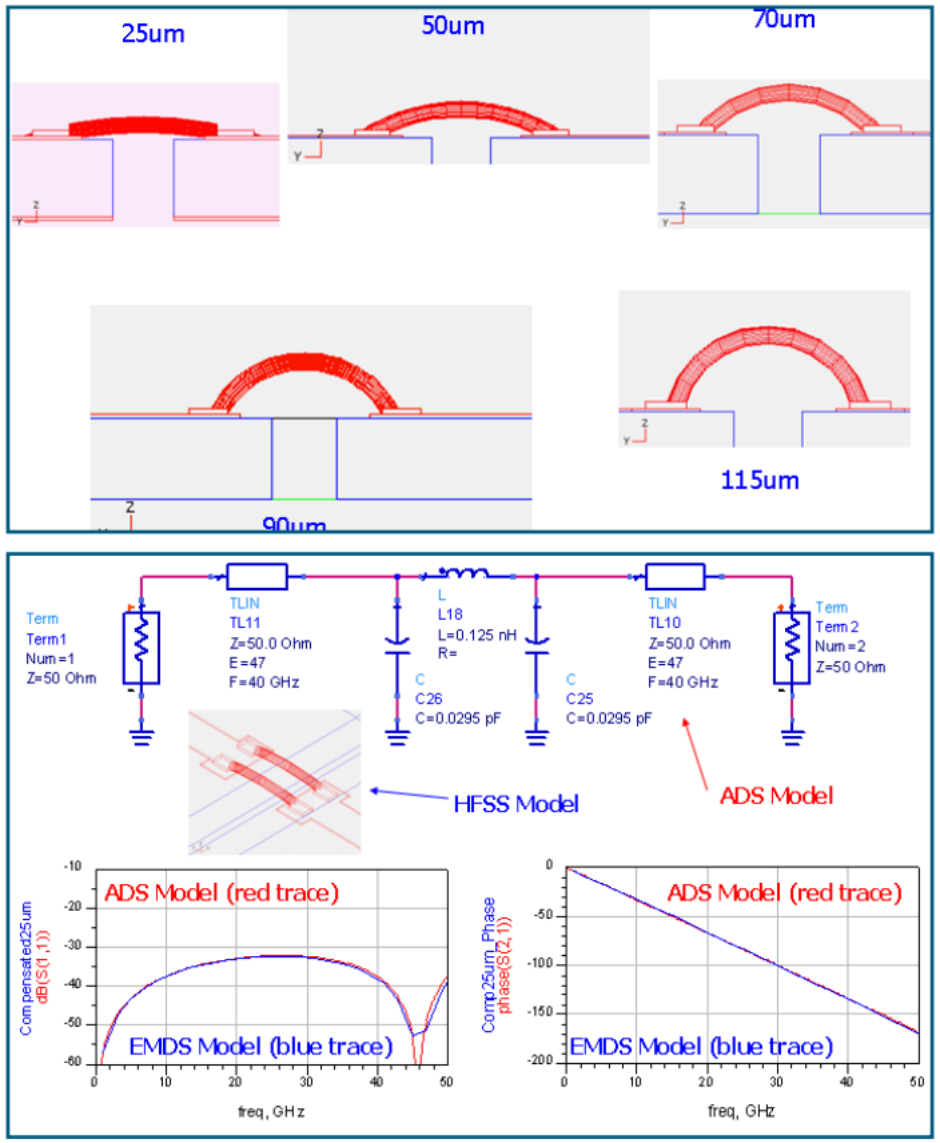


- Mature technology
- Higher cost
- Lower losses, lower parasitics
- Suitable for packaging ICs with air bridges
- Suitable for mmWave applications provided some modifications

Why is packaging at mmWaves so difficult?

- In general, a package design needs to address the following concerns no matter at what frequency is it intended to operate:
  - Material compatibility (wirebondability, solderability, laser ablation vs mechanical routing, substrate losses, etc)
  - Reliability
  - Interconnectivity (Wirebonding, flip-chip, etc)
  - Die attachment and lid/sealing methods (die handling employing collets, encapsulation, seam sealing,etc)
  - Hermiticity (or protection of internal cricuits
  - Thermal design
- On top of the above concerns, the following additional issues arise whenever dealing with mmWave packaging designs:
  - Distributed effects
  - Undesired resonances, parasitic effects and adequate RF grounding
  - Circuit traces that must be treated as TLs
  - Substrate dispersion effects
  - Coupling and cross-talk between circuital elements

Distributed Effects



- Whenever the physical dimensions of circuit elements become a fraction of the wavelength, distributed effects become relevant in one of the following manners:
  - Lumped elements namely resistors, capacitors and inductors no longer behave as such. Their impedance will vary over frequency in ways that no longer can be represented by a single passive component
  - Metal package housings would start to behave a cavity resonators
  - Interconnecting signal traces must be treated as transmission lines
  - Wirebonds need to be modeled as complex networks
  - As frequency increases, wirebonds will resonate or appear as antennas

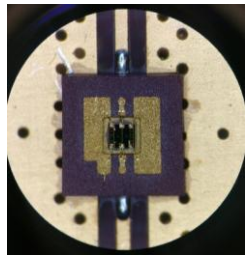
[5]

MCL's LTCC Packages: Technology Roadmap

LTCC Substrate

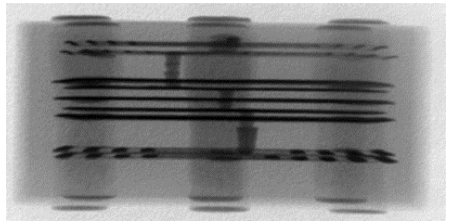
1st and 2nd Level Interconnects

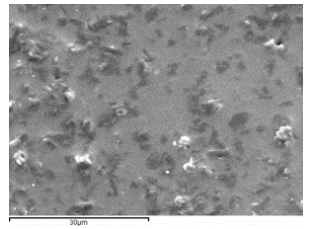
- Ball - Stich
- Wedge –Wedge
- Reverse Bond
- V- Bond
- Ribbon Bond
- Flip Chip



Mat. Characterization

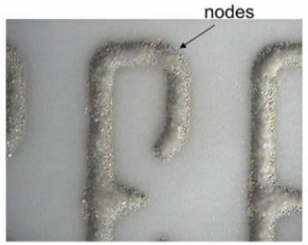
- Er and Tand up to mmWaves
- Dispersion (signal integrity)
- Anisotropy
- Power Handling/Thermal Resistance





Process and technology

- Photo-Imageable process
- Conductor's surface roughness
- Contour definition
- Tightening of line widths and spacings
- Tightening of conductor's dimensions tolerances
- New material systems



Screen printing

Photoimageable process

Multiphysics Modeling

- Circuital analysis and co-simulation
- Method of Moments
- Finite Element Method
- Time Domain Reflectometry
- Thermal Analysis
- Mechanical stress Analysis

Qual and test plans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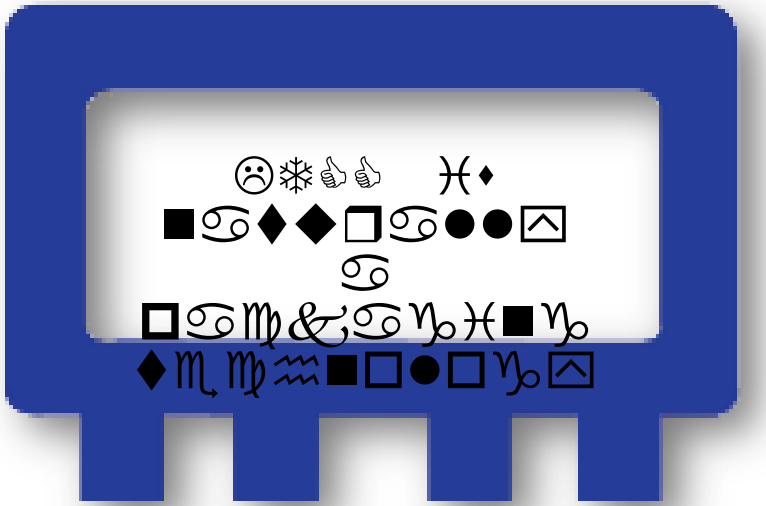

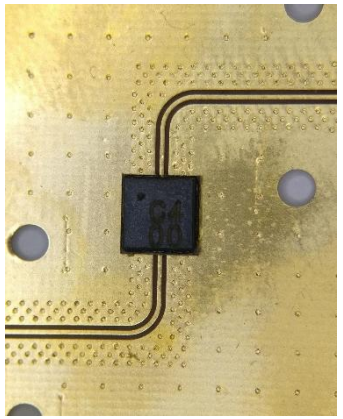


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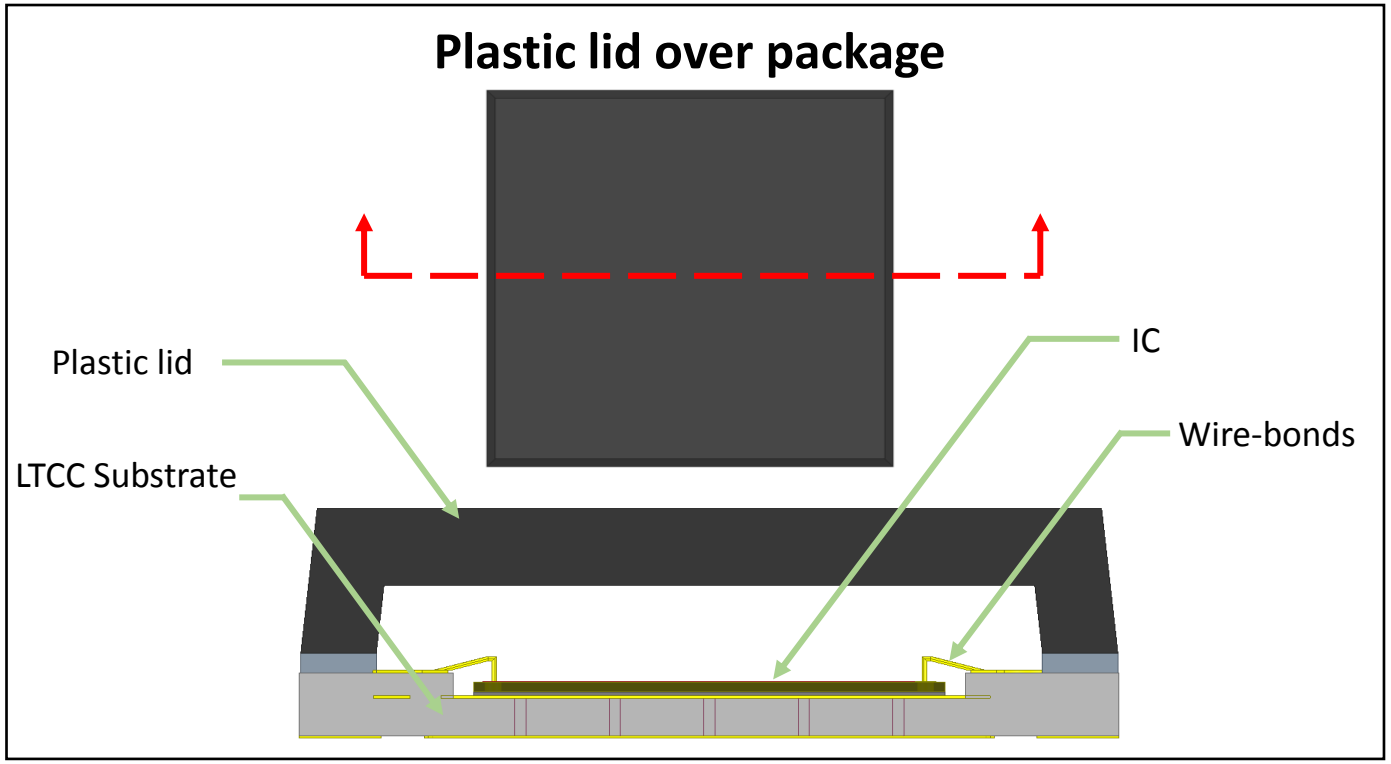
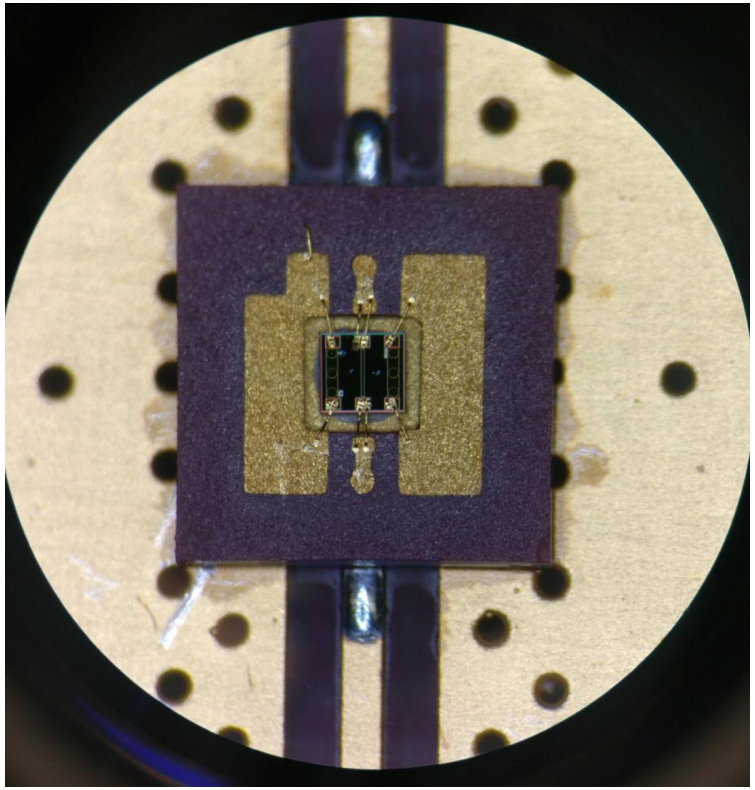
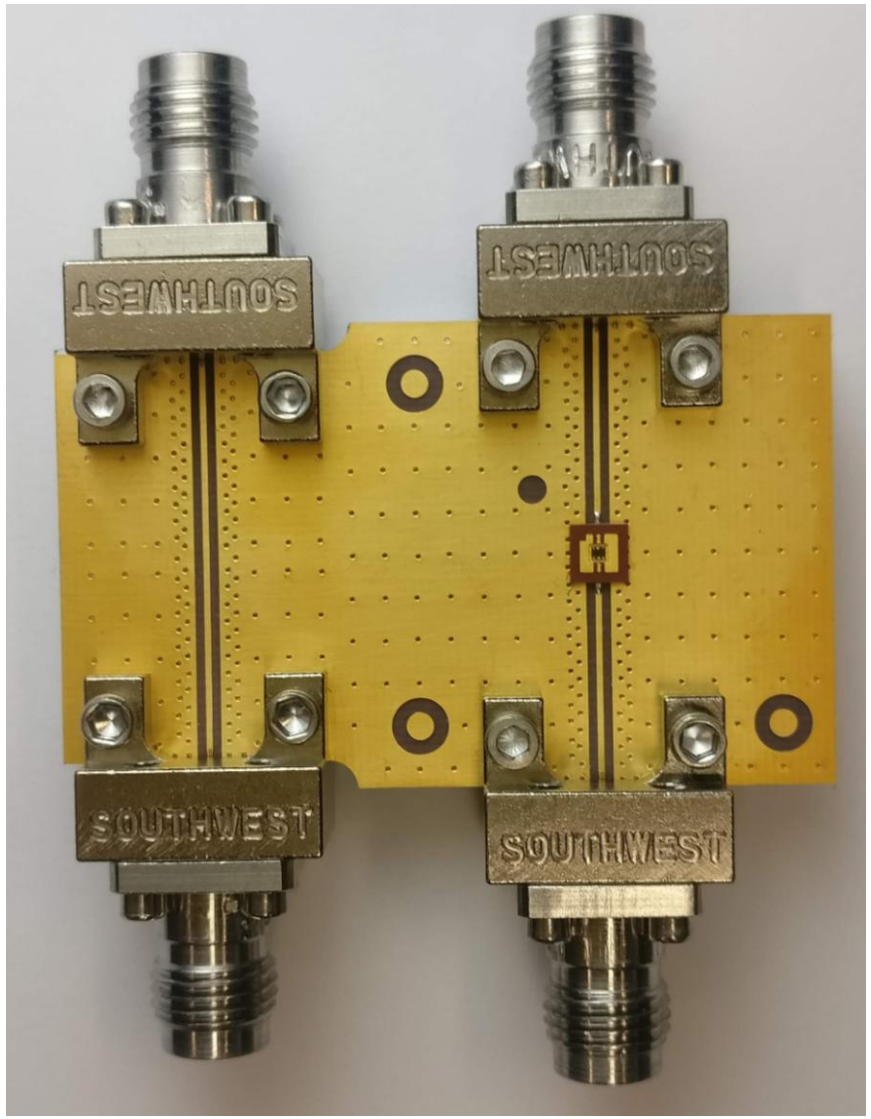
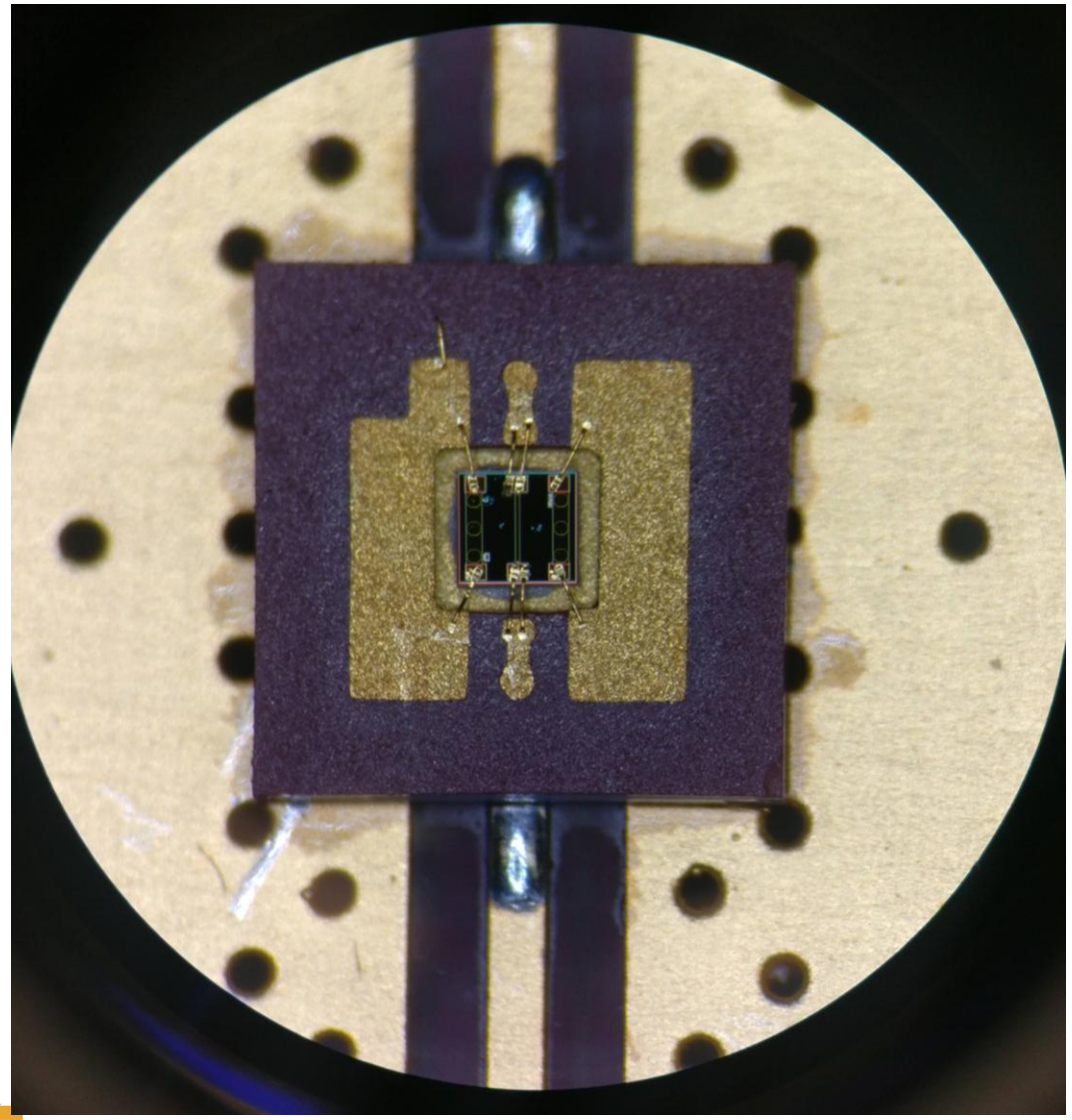
LTCC mmWave Packaging Solutions



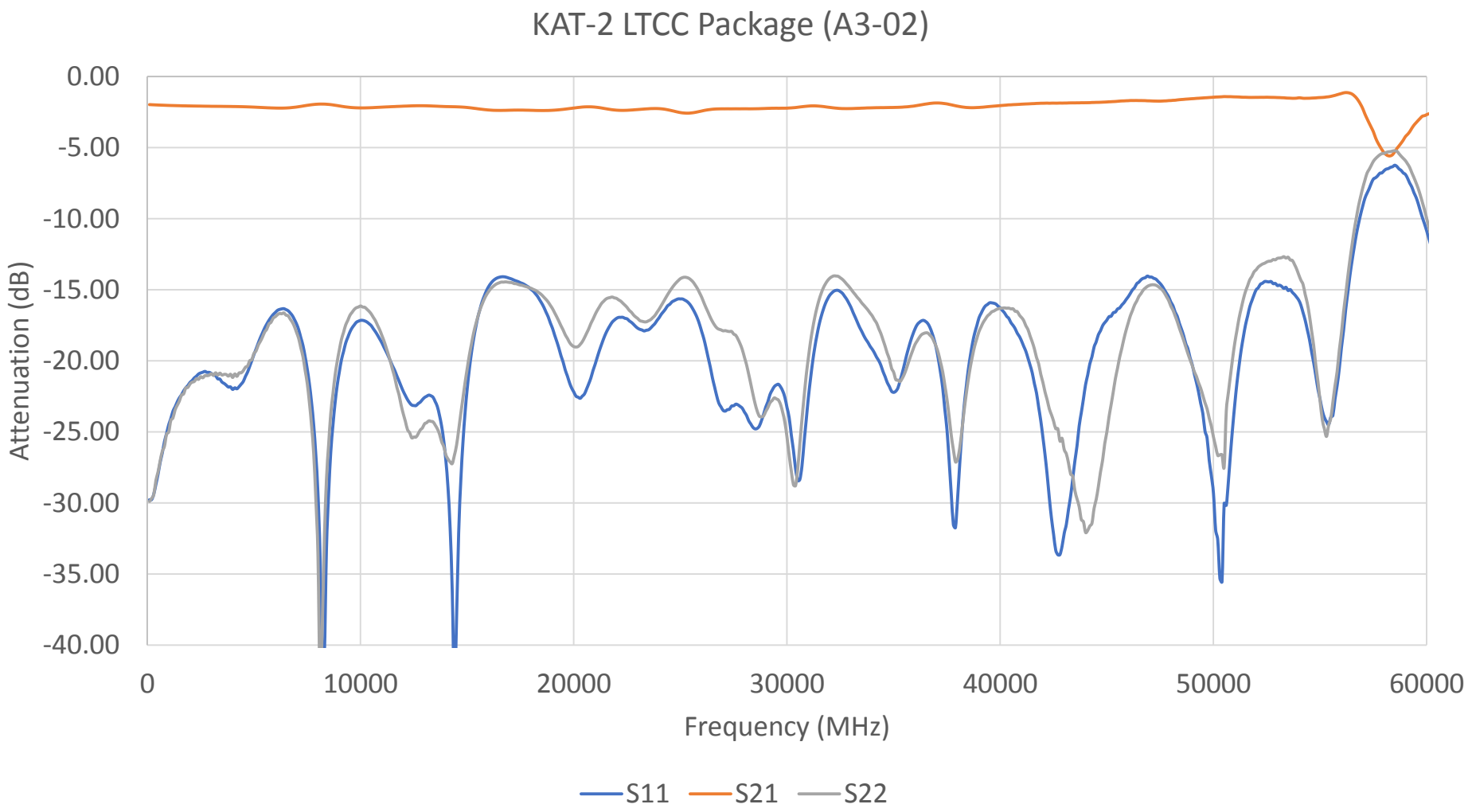


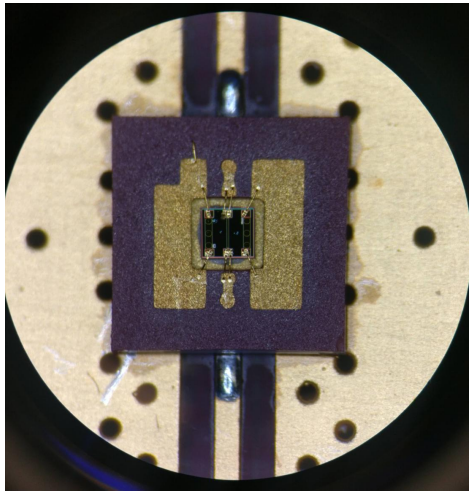
LTCC mmWave Packaging Solution

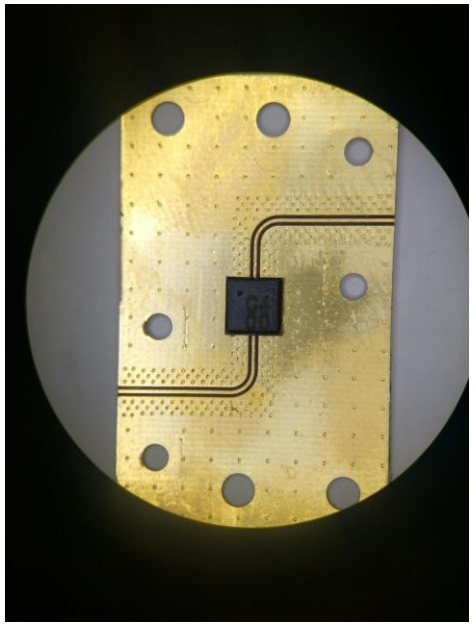




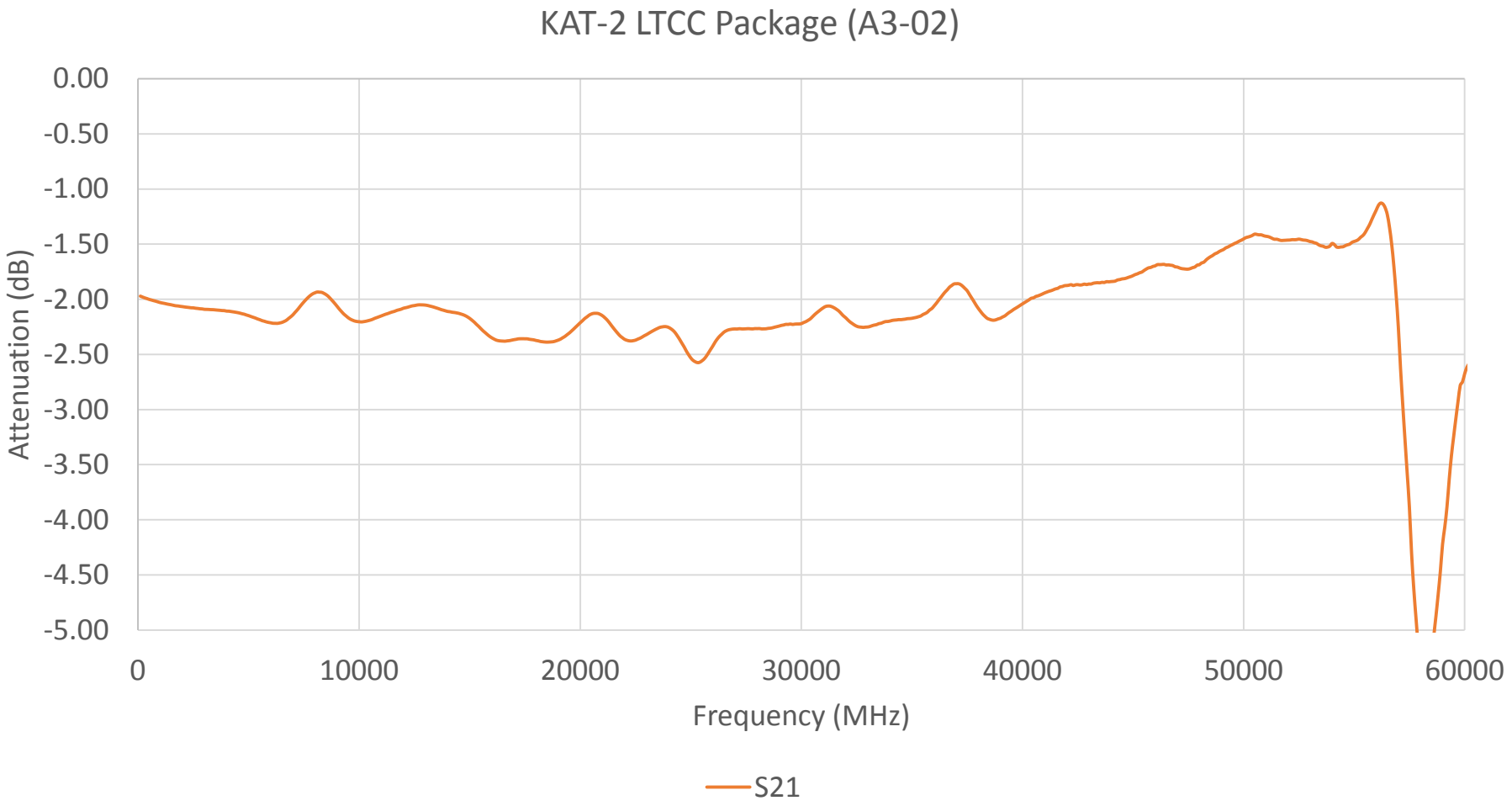
LTCC mmWave Packaging Solution

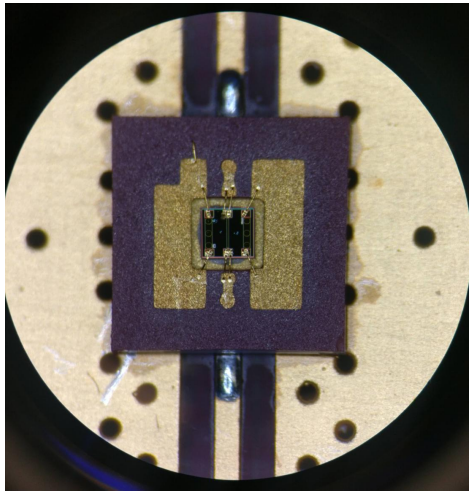


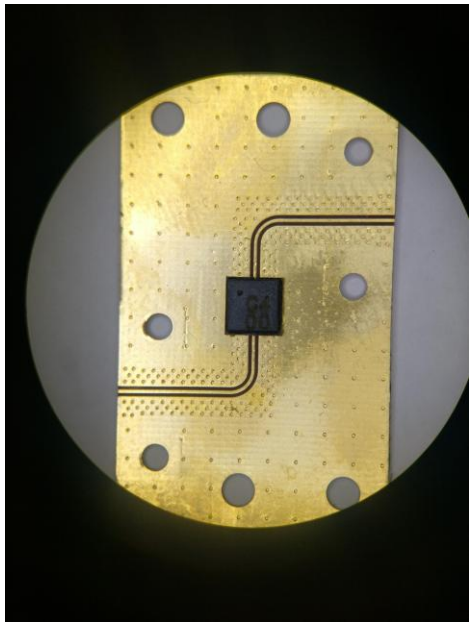




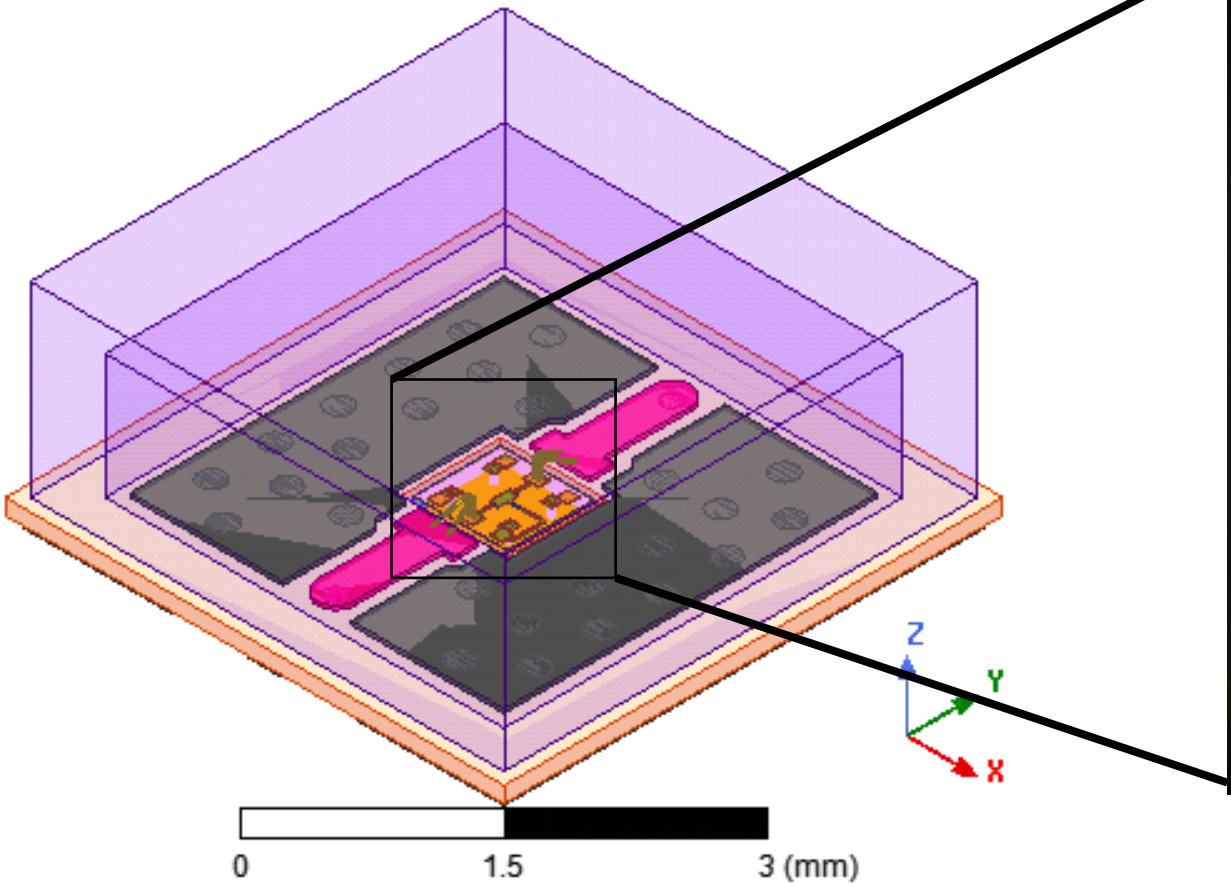
LTCC mmWave Packaging Solution



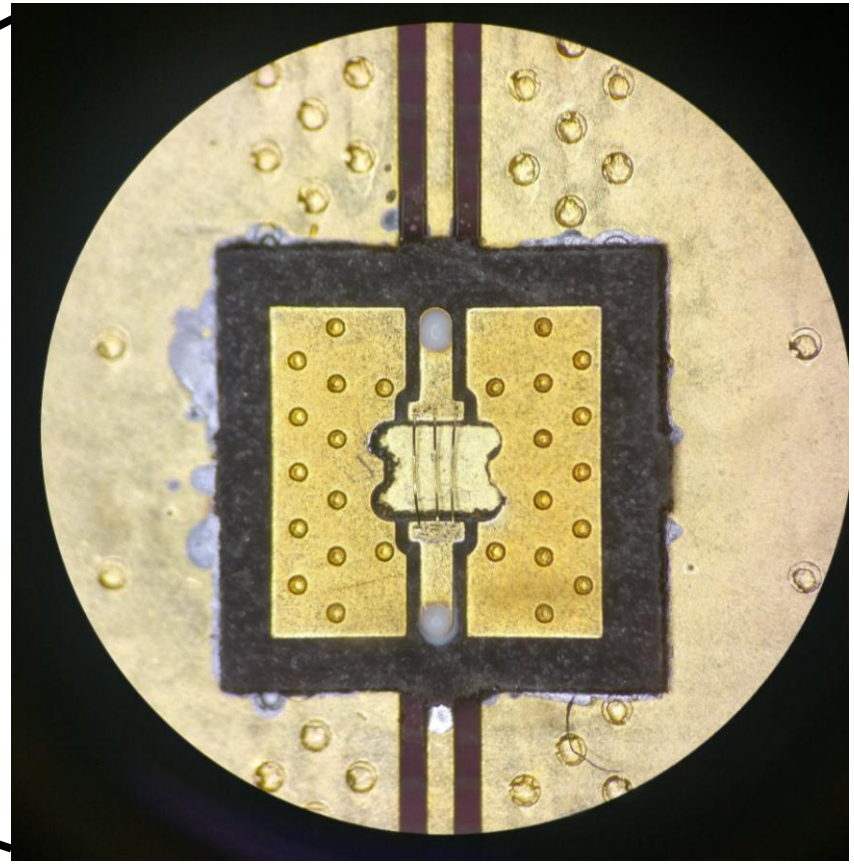




Organic PCB mmWave Packaging Solutions

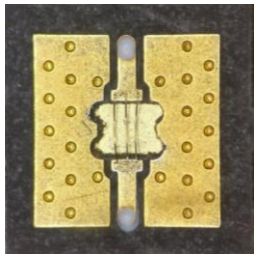


ISOMETRIC VIEW

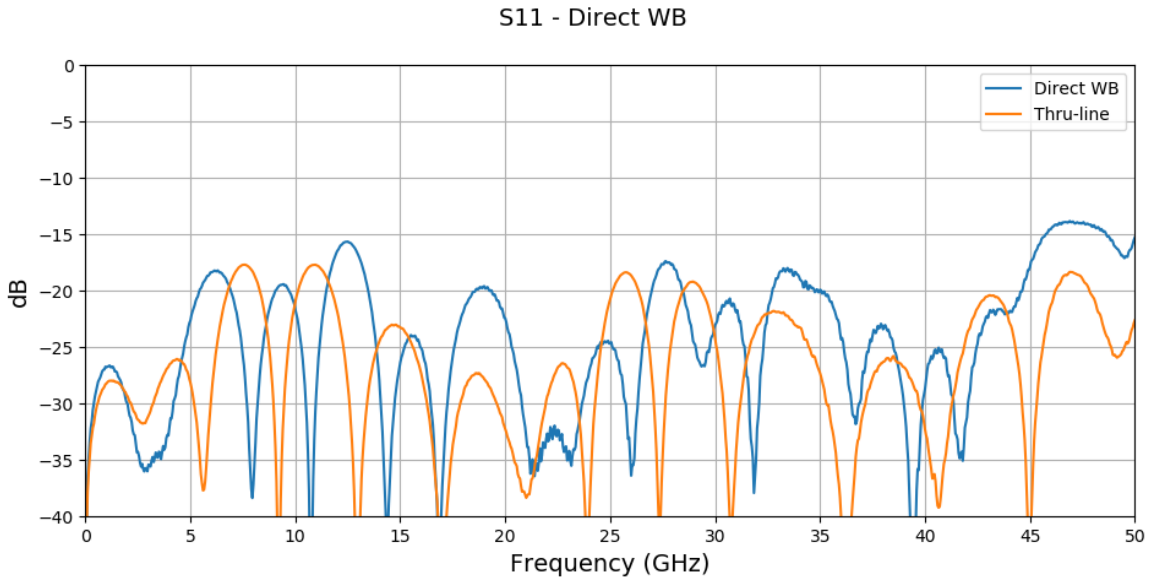


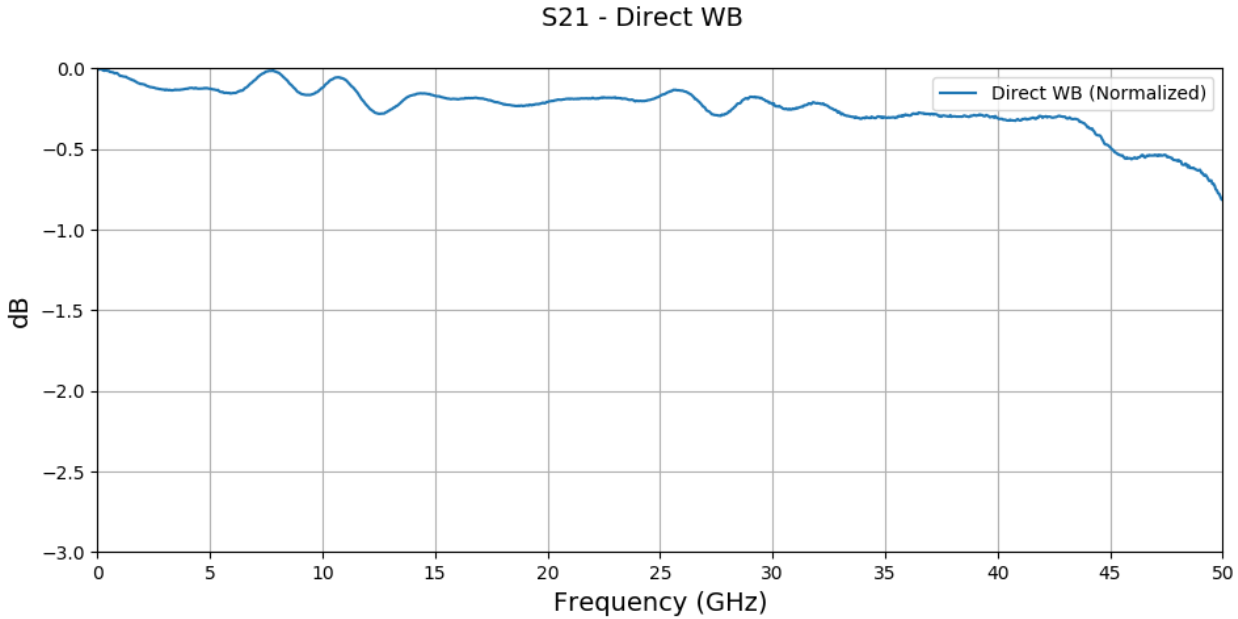
Drop in die

Organic PCB mmWave Packaging Solutions



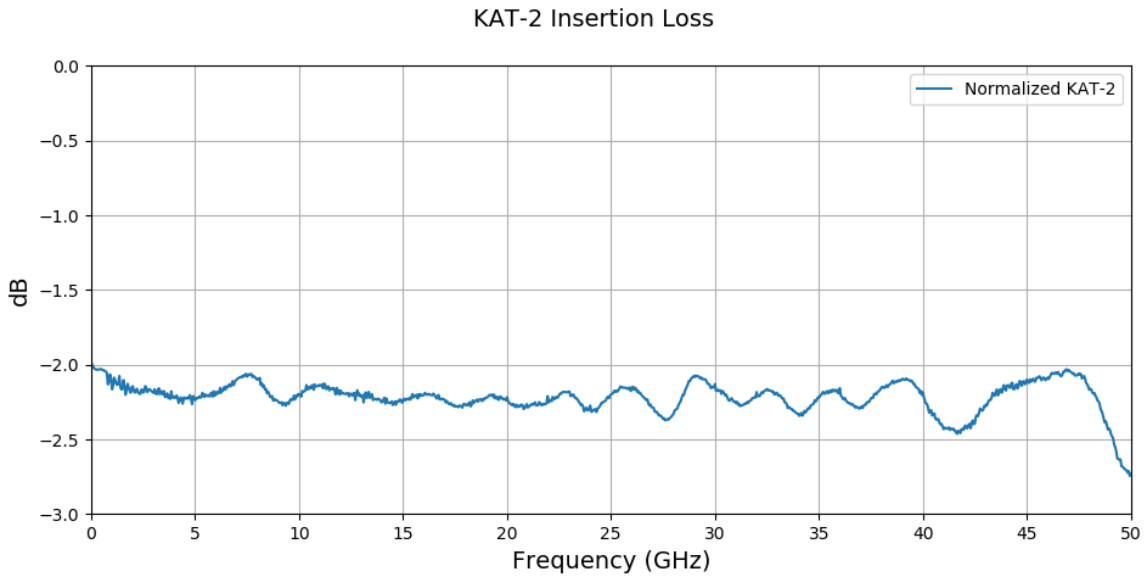
Package's thru performance

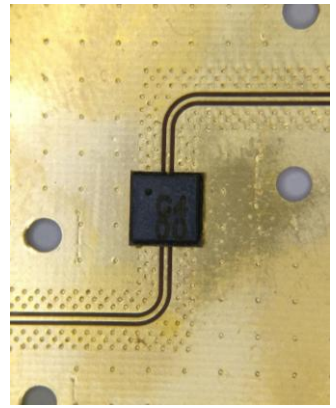


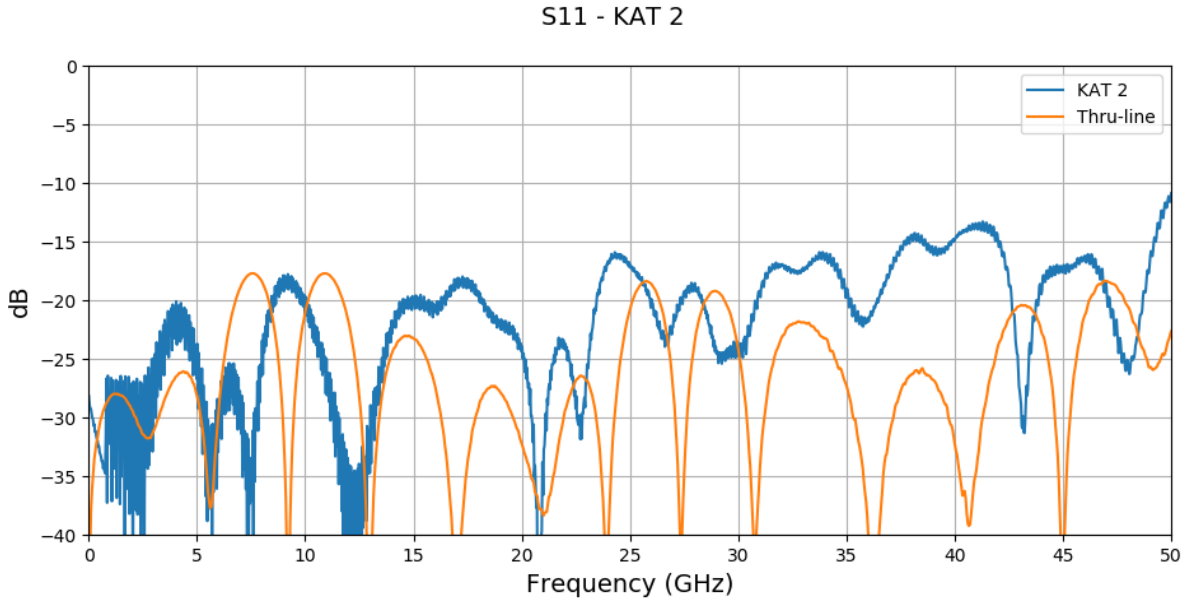


Organic PCB mmWave Packaging Solutions

Packaged KAT-2+ performance

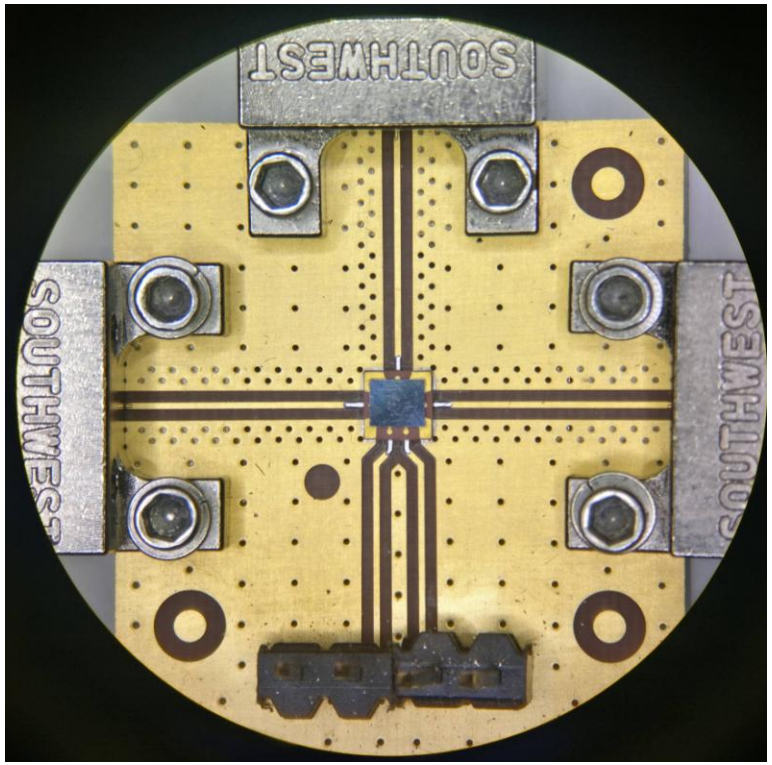






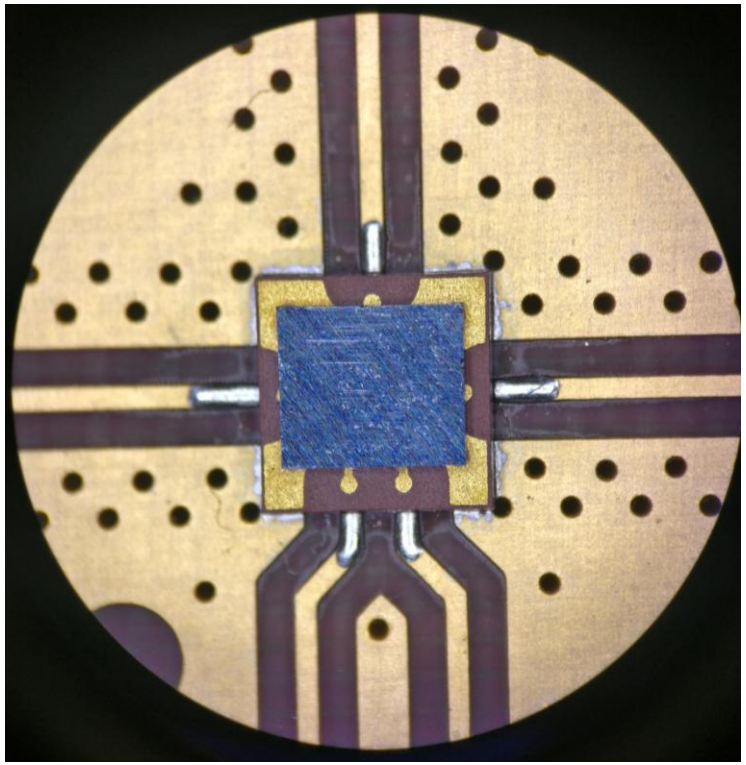
Flip – Chip Packaging Solutions

SPDT Flip – Chip switch assembly



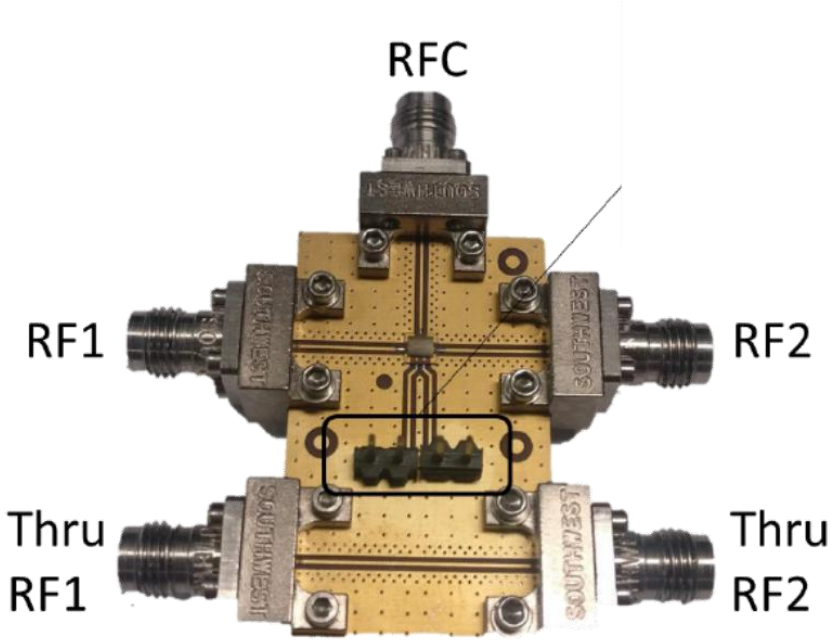
SPDT Die size:
2.495mm x 2.149mm

Package Dimensions:
3.0 x 3.0mm



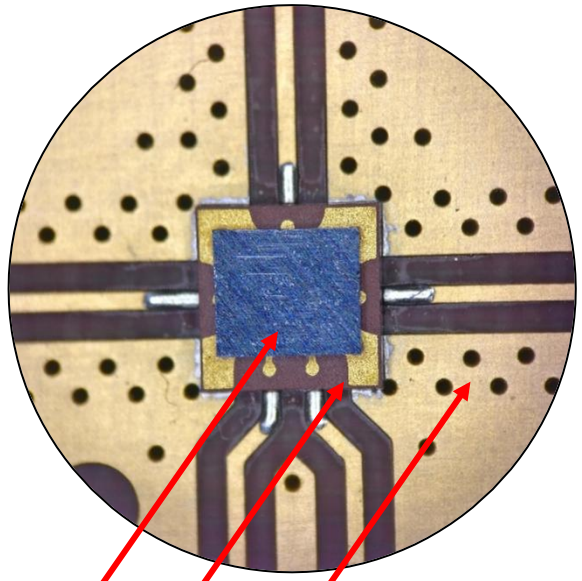
SPDT Switch - Assembly

Test board*

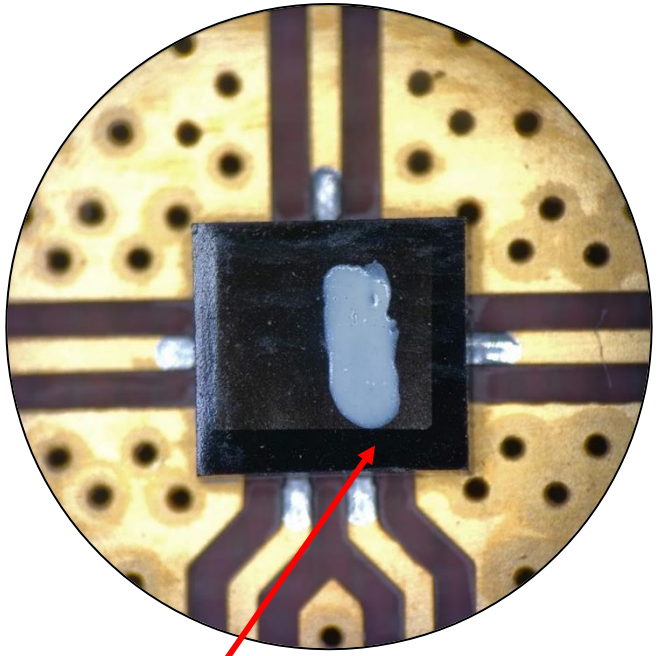


*TLY-5, 5mil thick substrate

Open die on LTCC



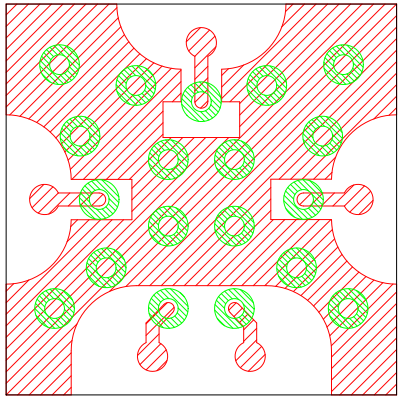
Over-molded die on LTCC



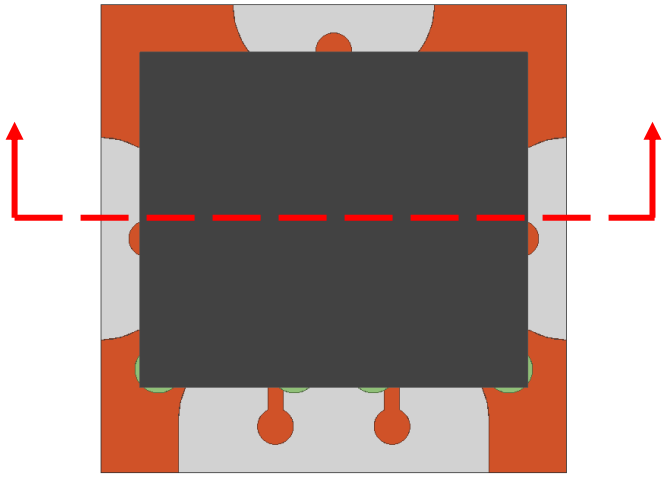
SPDT Switch - Units measured

A0: Open die on LTCC B14-L2-P1A+
A1: Over Molded die on LTCC P/N B14-L2-P1A+
A2: Over Molded die on LTCC P/N B14-L2-P1A+
A3: Over Molded die on LTCC P/N B14-L2-P1A+
HFSS 1: Over Molded die dummy on LTCC B14-L2-P1A+ (assuming no underfill)
HFSS 2: Over Molded die dummy on LTCC B14-L2-P1A+ (assuming underfill)

B14-L2-P1A+

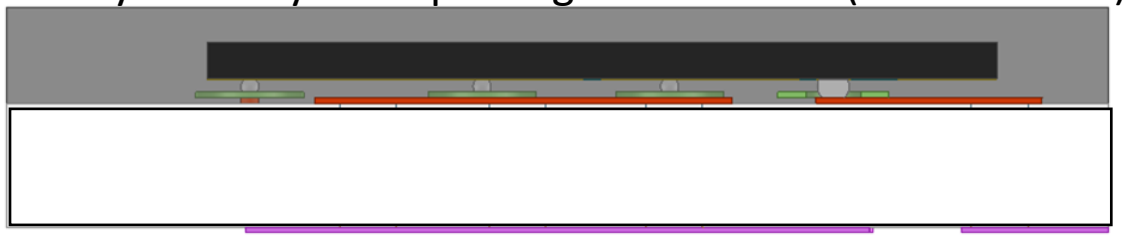


Top View (No molding included)



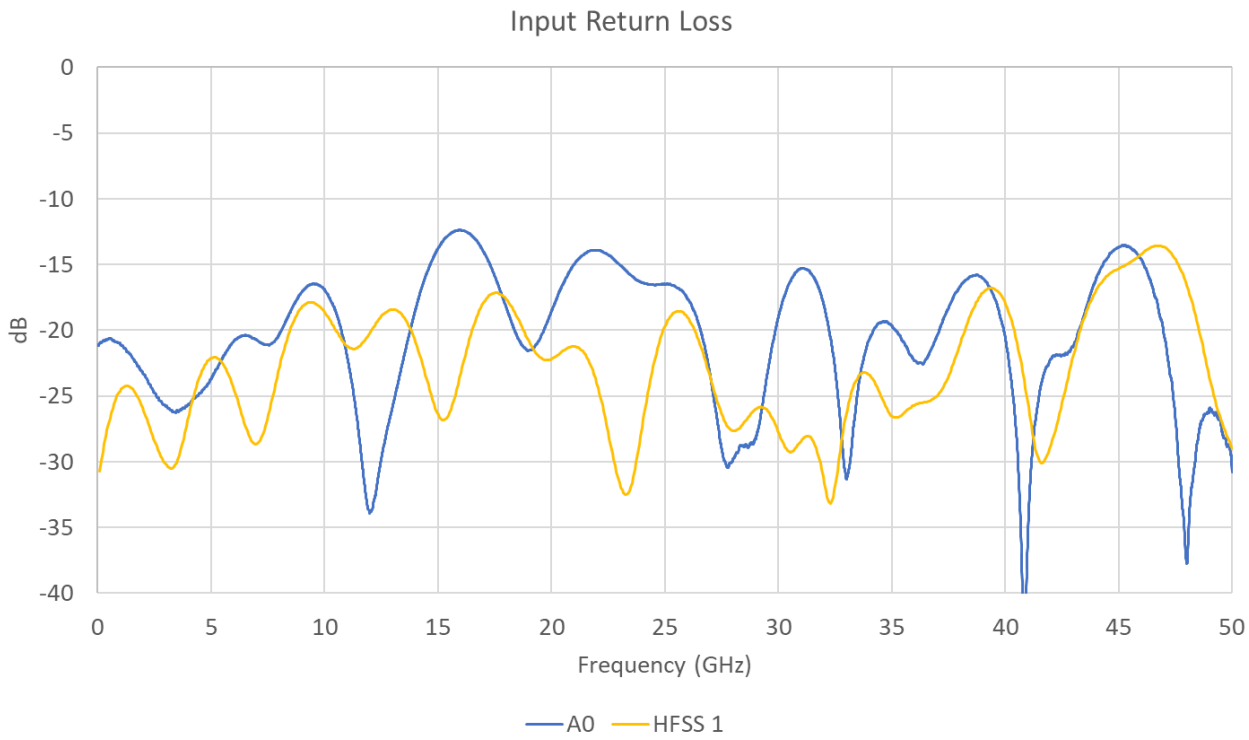
No underfill: Target implementation (HFSS1 model)

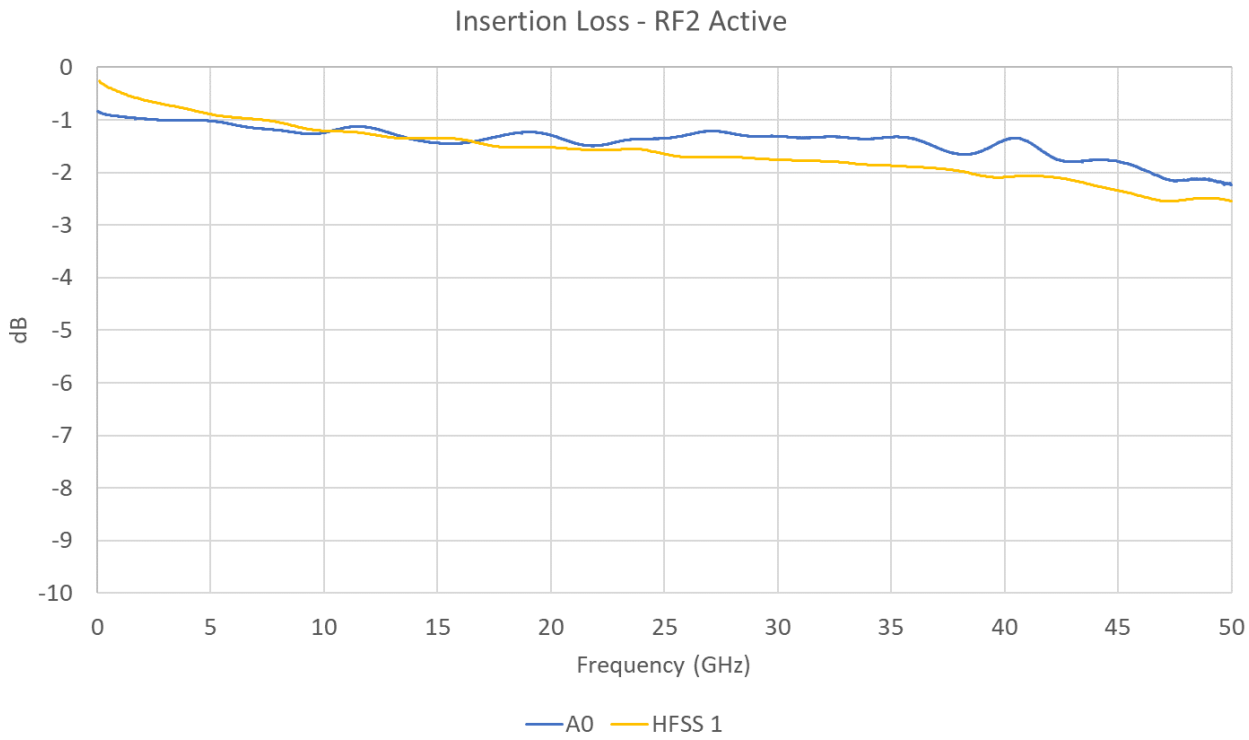
Underfill: Most likely this may end up being the situation (HFSS2 model)



SPDT Switch – Measurements

Open die on LTCC (Tests Data) vs HFSS simulation

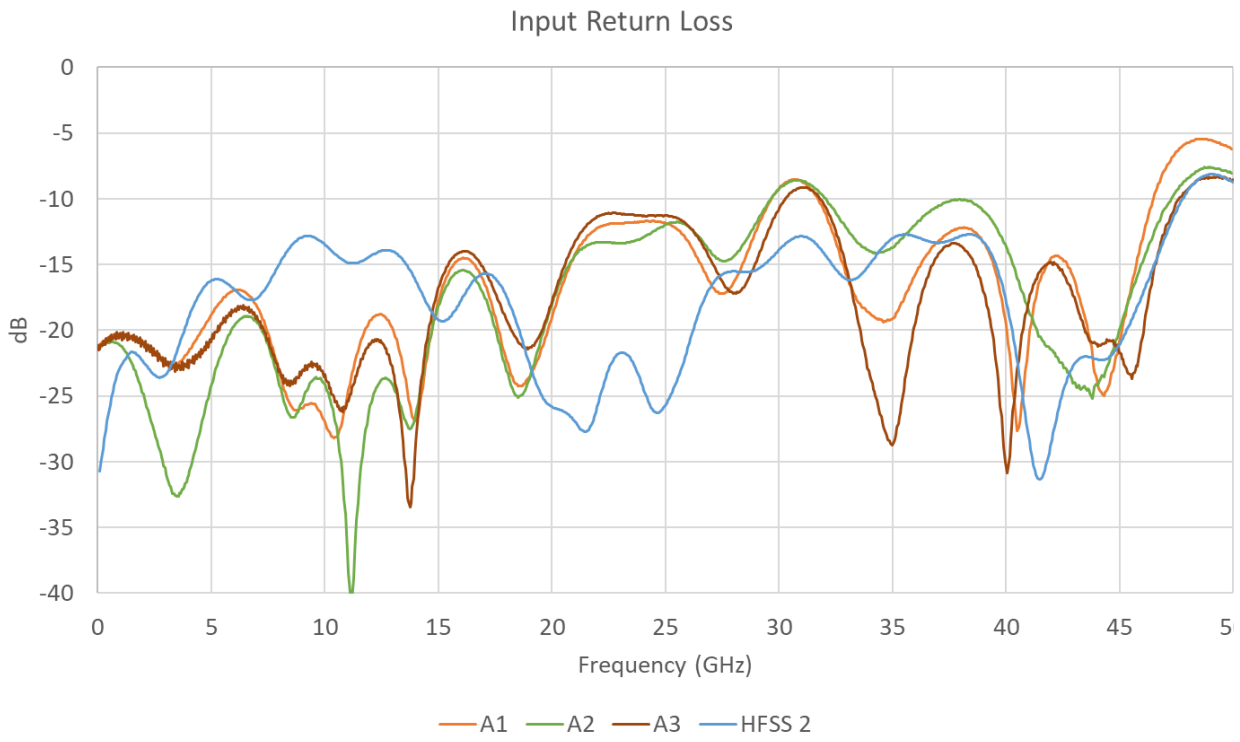


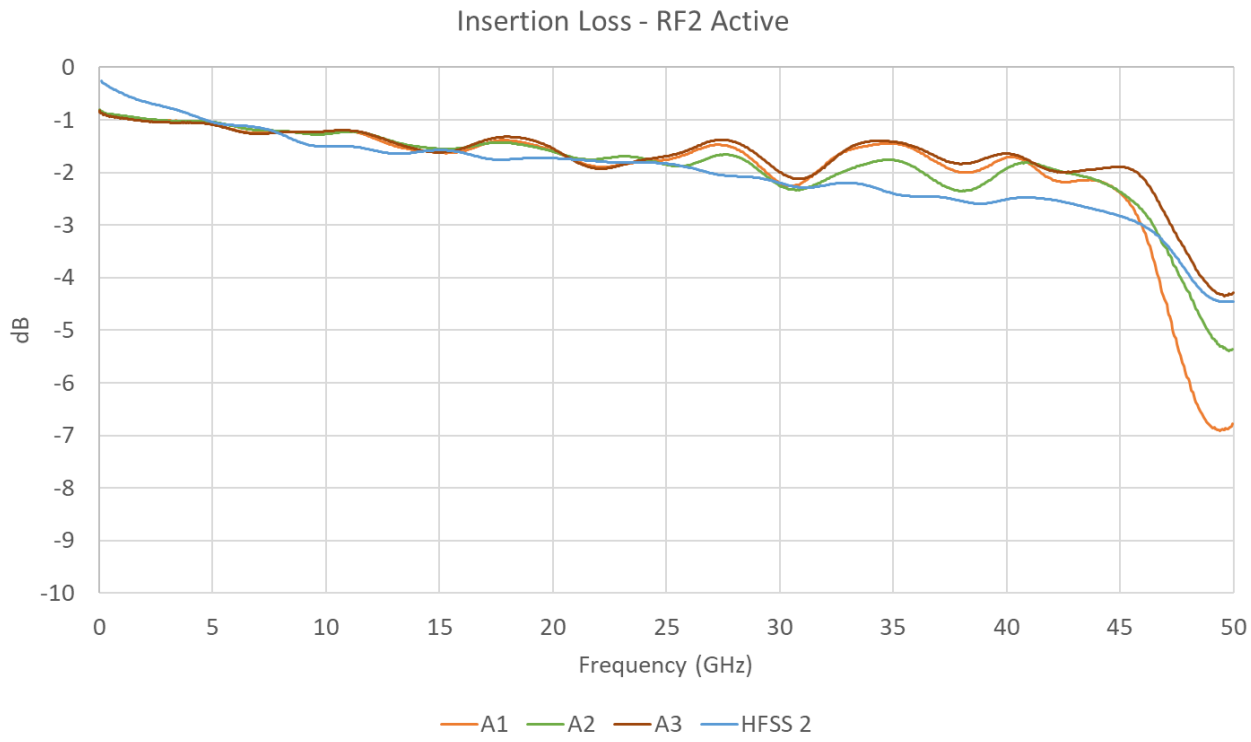


A0 (open die) and **HFSS1** show good agreement. No die underfilling. No molding compound in **A0 (open die)**.

SPDT Switch – Measurements

Over-molded die on LTCC (Tests Data) vs HFSS simulation

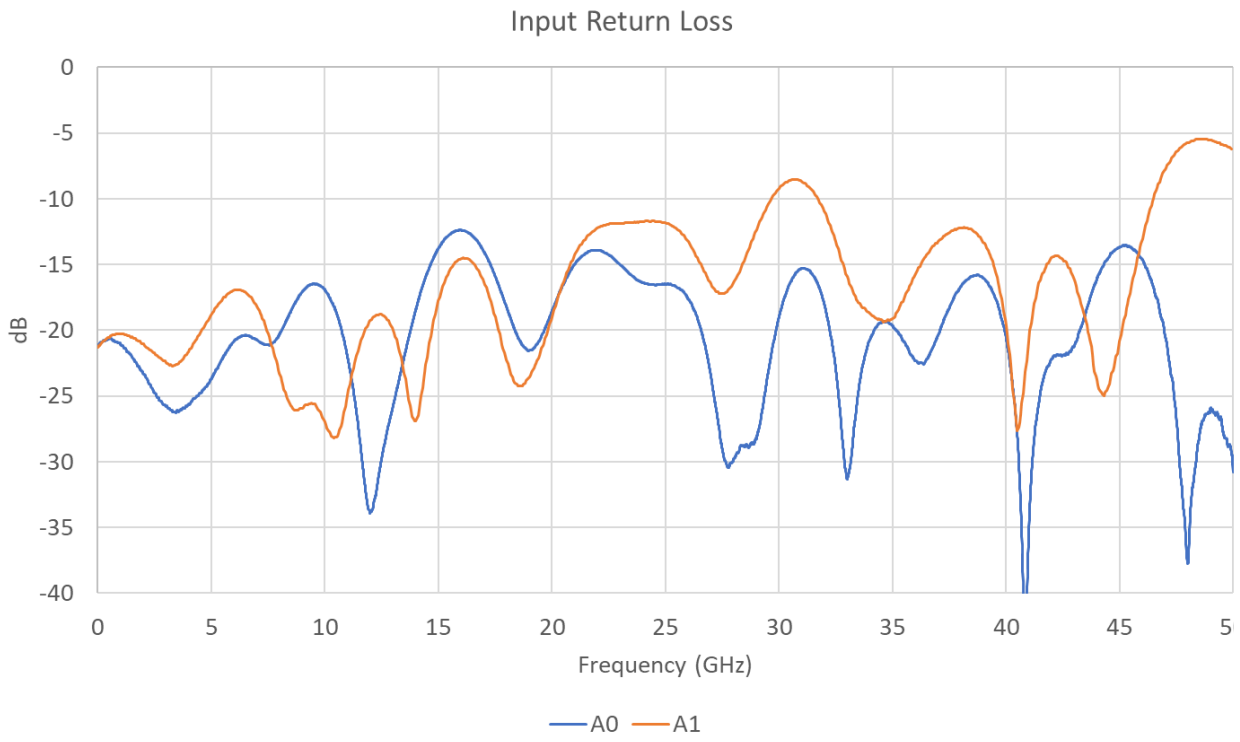


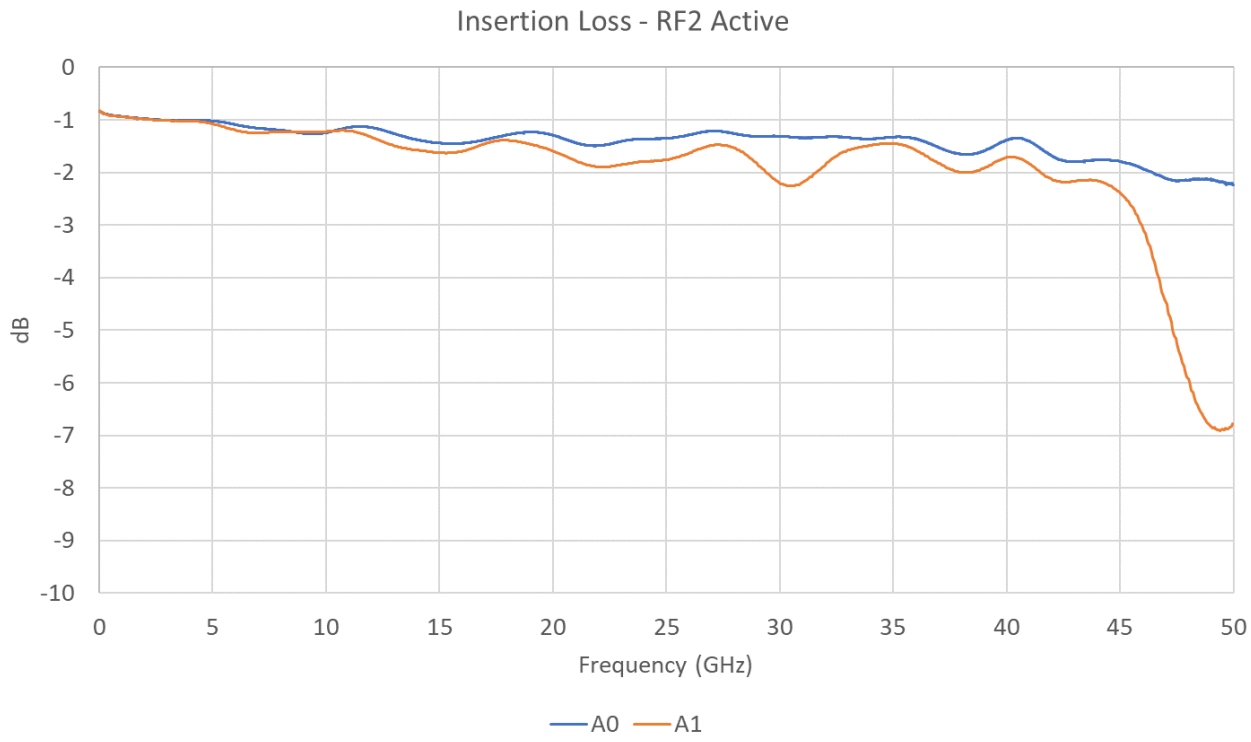


A1 (over-molded) and **HFSS2** show good agreement. Suspected molding underfilling on fabricated unit.

SPDT Switch – Measurements

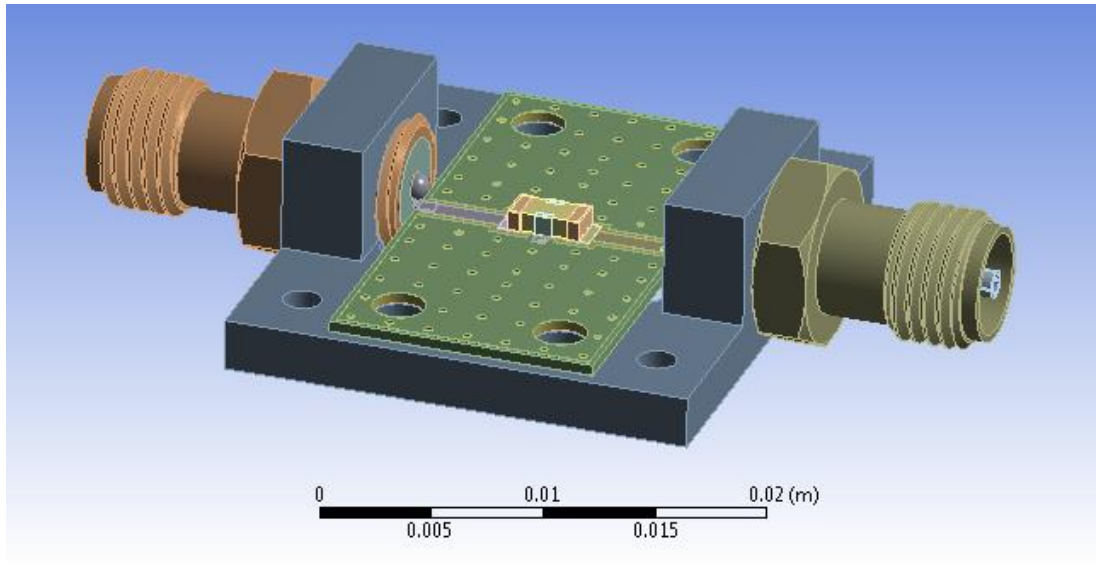
Open die on LTCC (Tests Data) vs Over-molded die on LTCC (Tests Data)

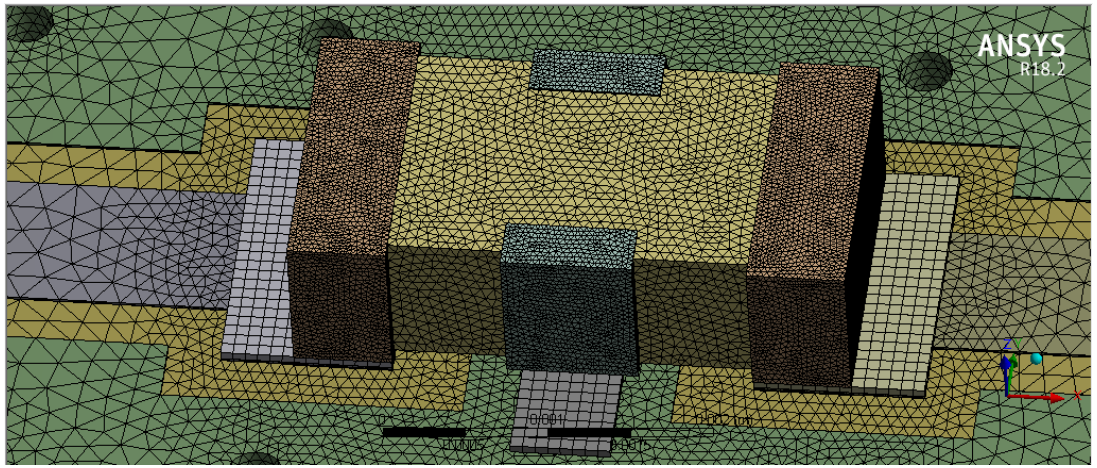


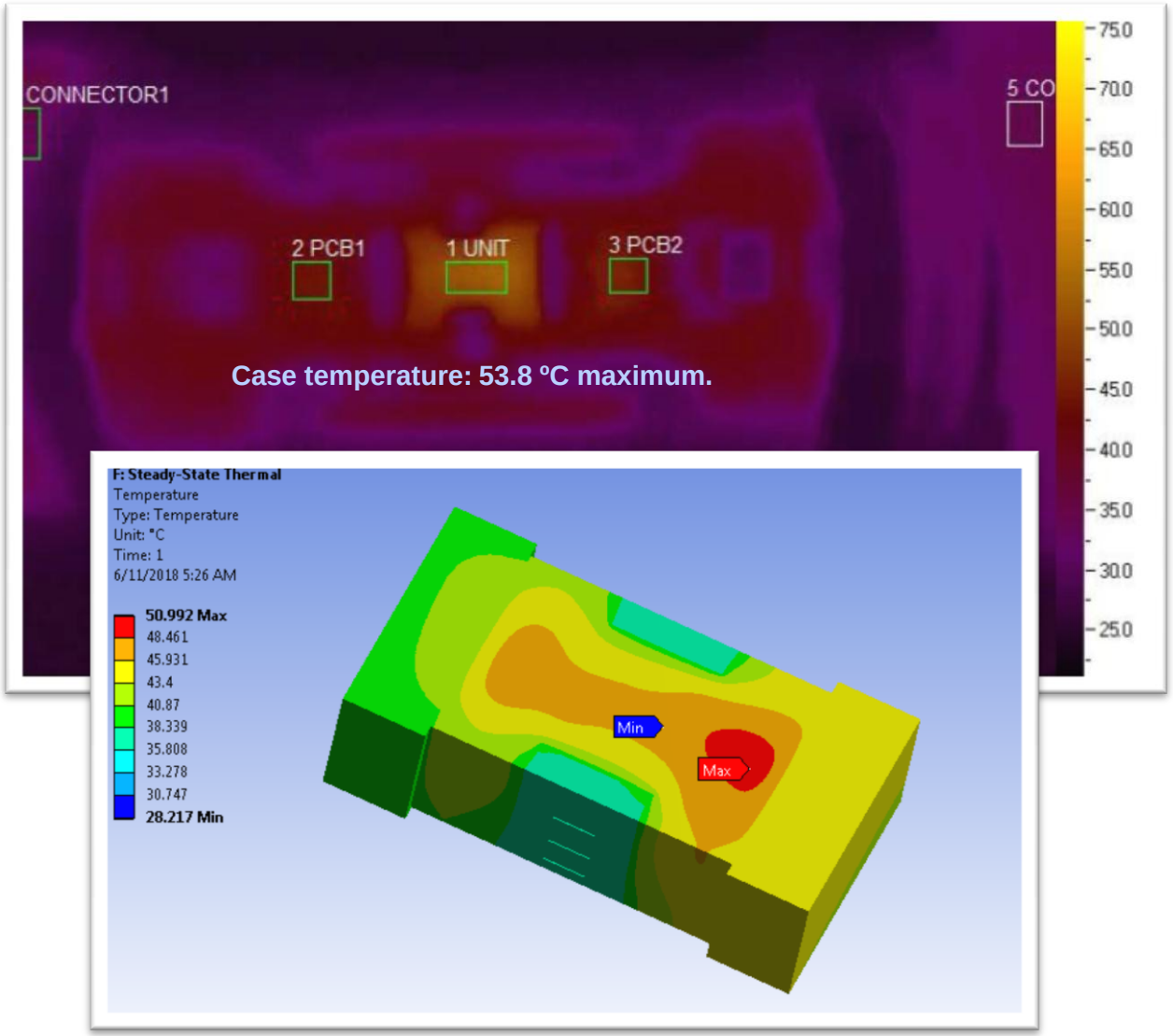


A0 (open die) has better performance than **A1 (over-molded)**

Multi-physics Simulation Capability

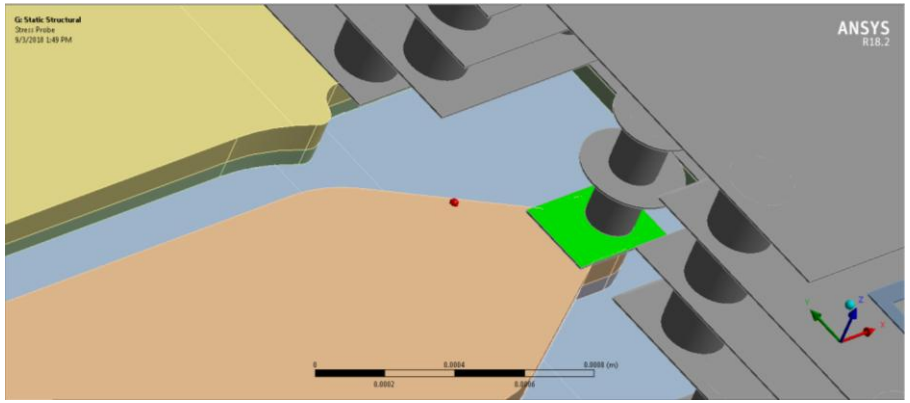






Multiphysics Analysis: Stress Results

Details of "Stress Probe"	
Orientation	Global Coordinate System
Suppressed	No
Options	
Result Selection	Equivalent (von-Mises)
Display Time	End Time
Spatial Resolution	Use Maximum
Results	
Equivalent (von-Mises)	2.0258e+008 Pa
Maximum Value Over Time	
Equivalent (von-Mises)	2.0258e+008 Pa
Minimum Value Over Time	
Equivalent (von-Mises)	2.0258e+008 Pa
Information	
Time	1. s
Load Step	1
Substep	1
Iteration Number	1



Details of "Stress Probe"	
Type	Stress
Location Method	Geometry Selection
Geometry	1 Face
Orientation	Global Coordinate System
Suppressed	No
Options	
Result Selection	Equivalent (von-Mises)
Display Time	End Time
Spatial Resolution	Use Maximum
Results	
Equivalent (von-Mises)	8.2807e+008 Pa
Maximum Value Over Time	
Equivalent (von-Mises)	8.2807e+008 Pa
Minimum Value Over Time	
Equivalent (von-Mises)	8.2807e+008 Pa
Information	

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