Linear Front End Module for 4G/5G Advanced Applications

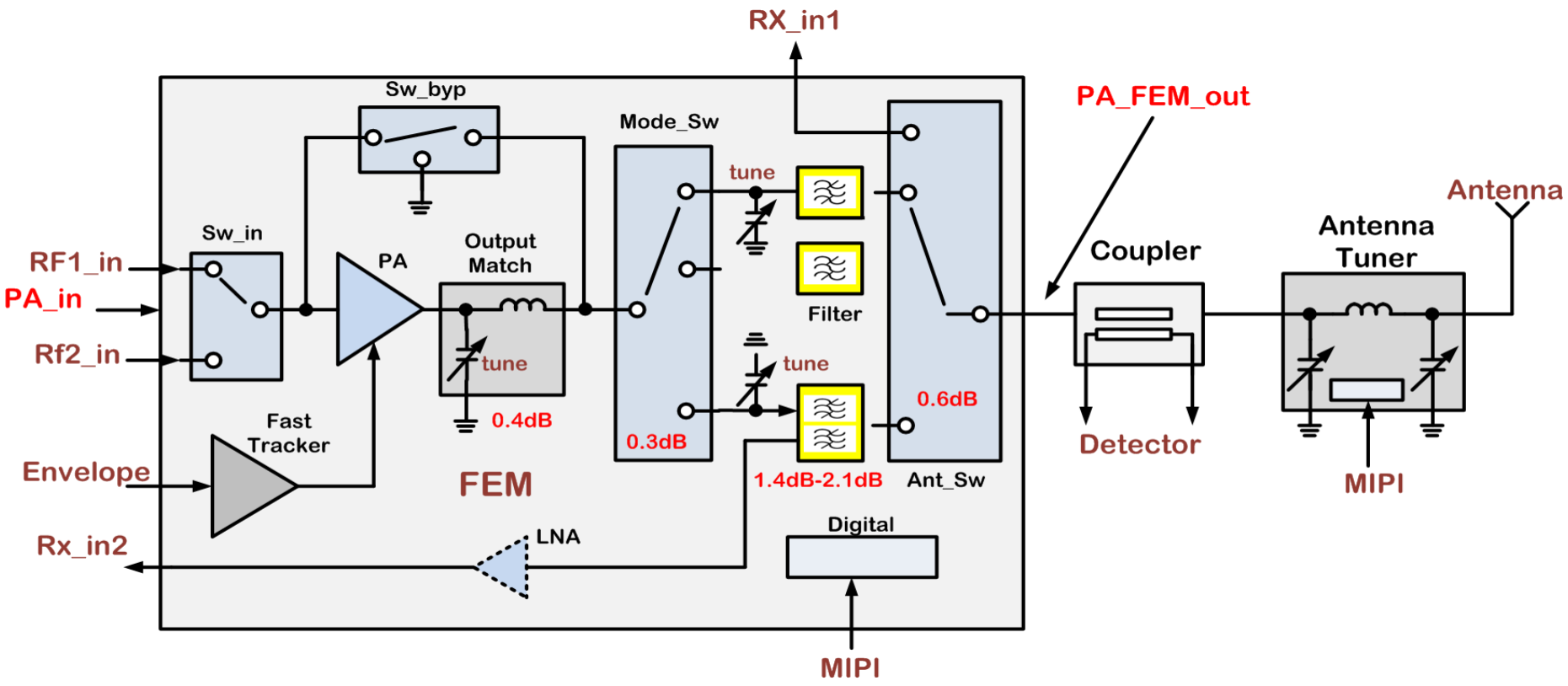
Florinel Balteanu, Skyworks Solutions, USA

florinel.balteanu@skyworksinc.com

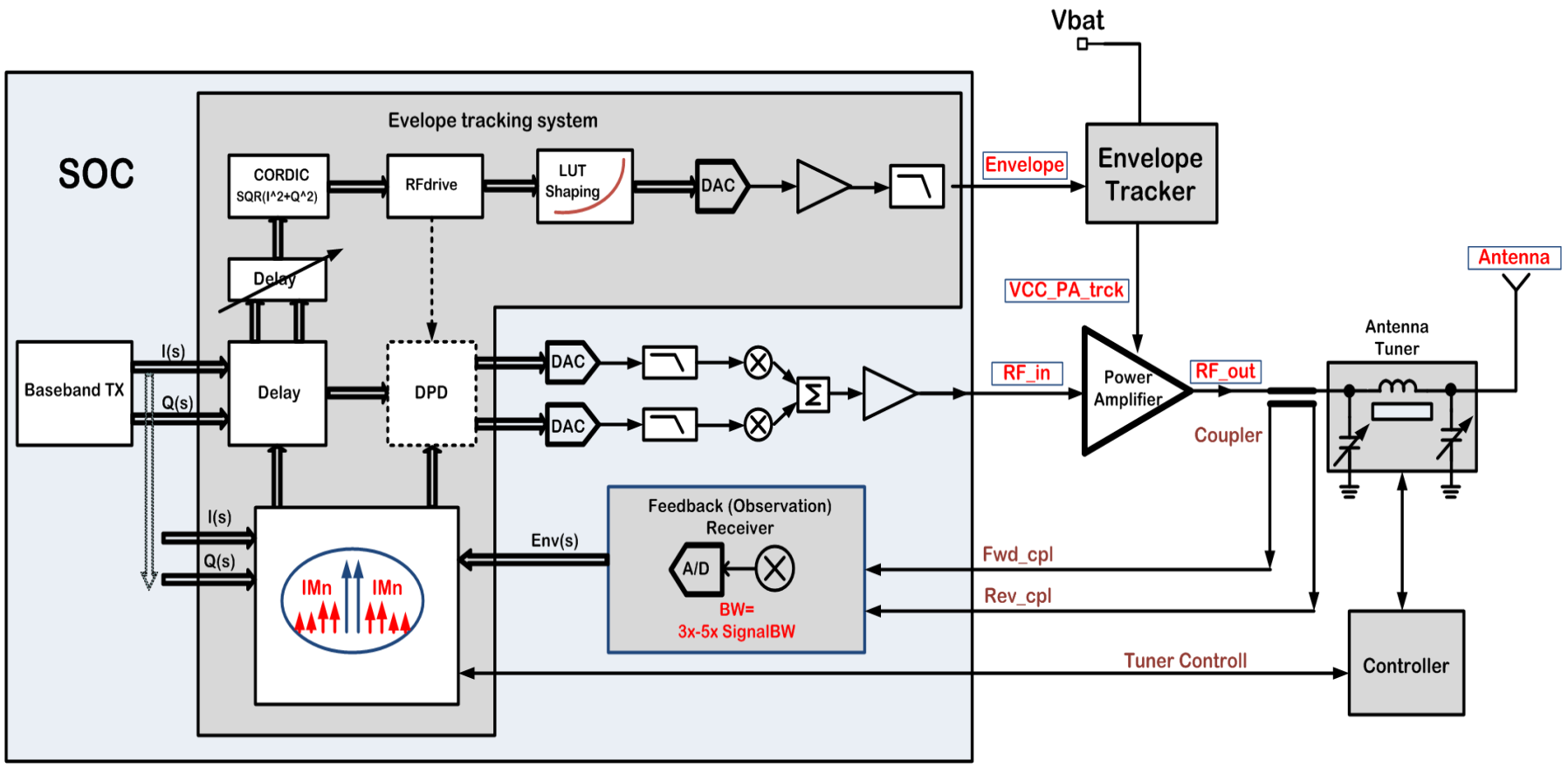
Outline

- Front End Module Structure
- Envelope Tracking Systems
- Envelope Tracking Controllers
- Three Port Power Amplifier
- Noise in Envelope Tracking
- Envelope Tracking for Carrier Aggregation
- High BW Envelope Tracking
- Conclusions

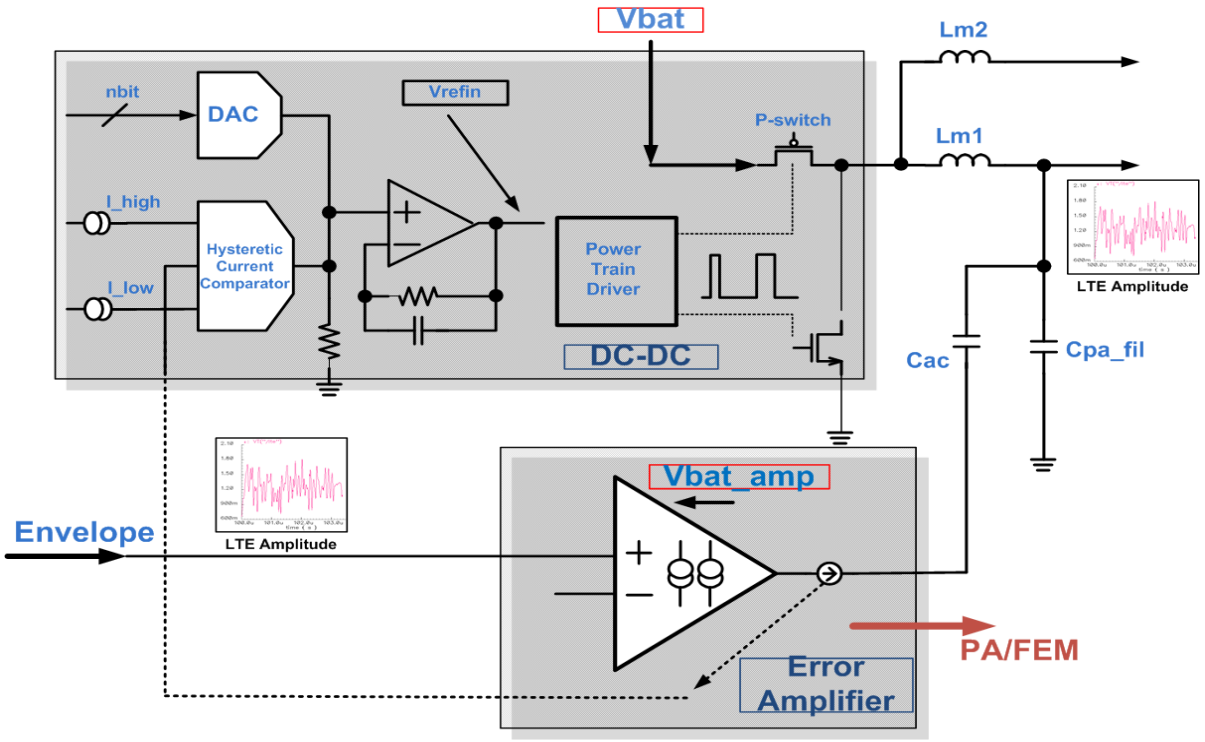
Front End Module Structure



Envelope Tracking System

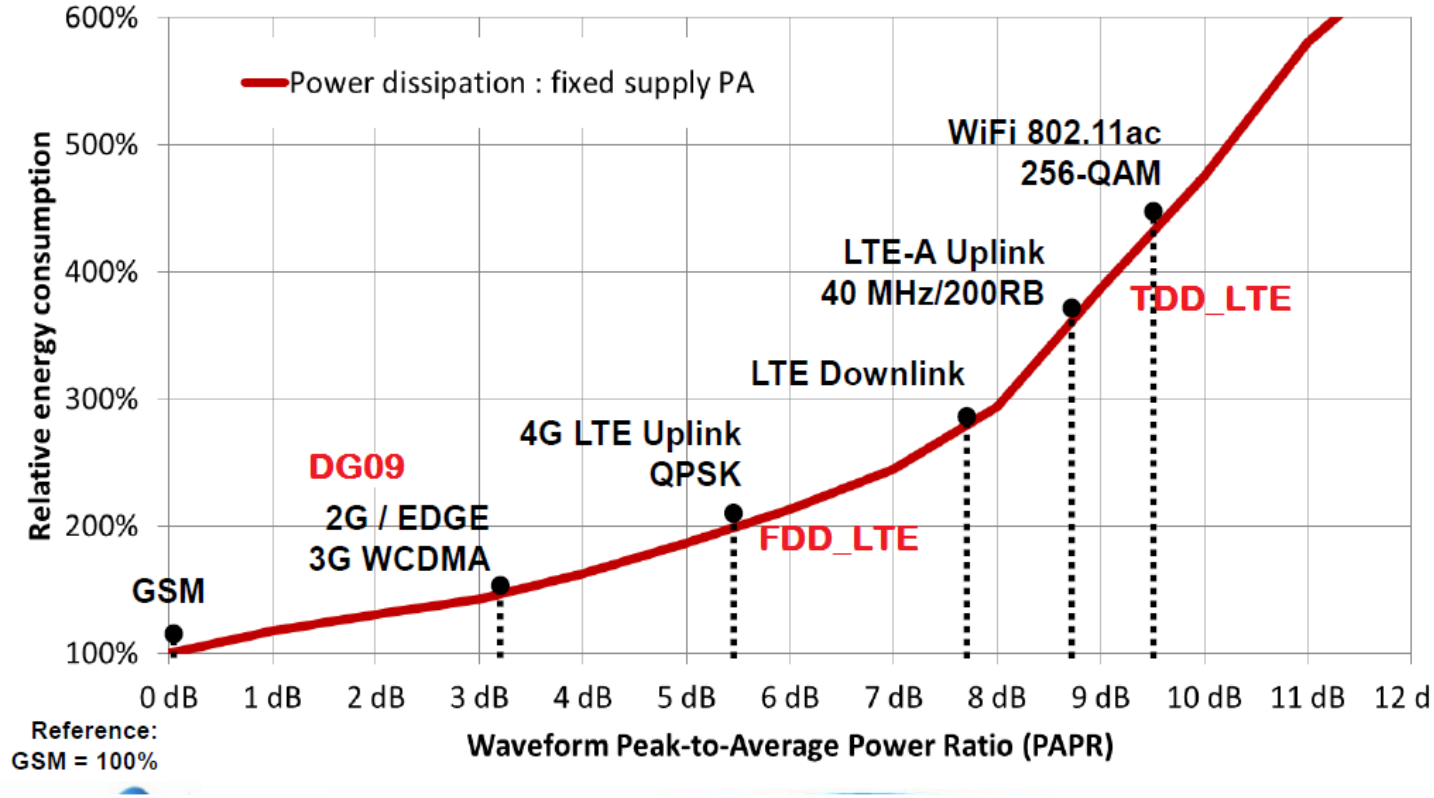


Hybrid Envelope Tracker



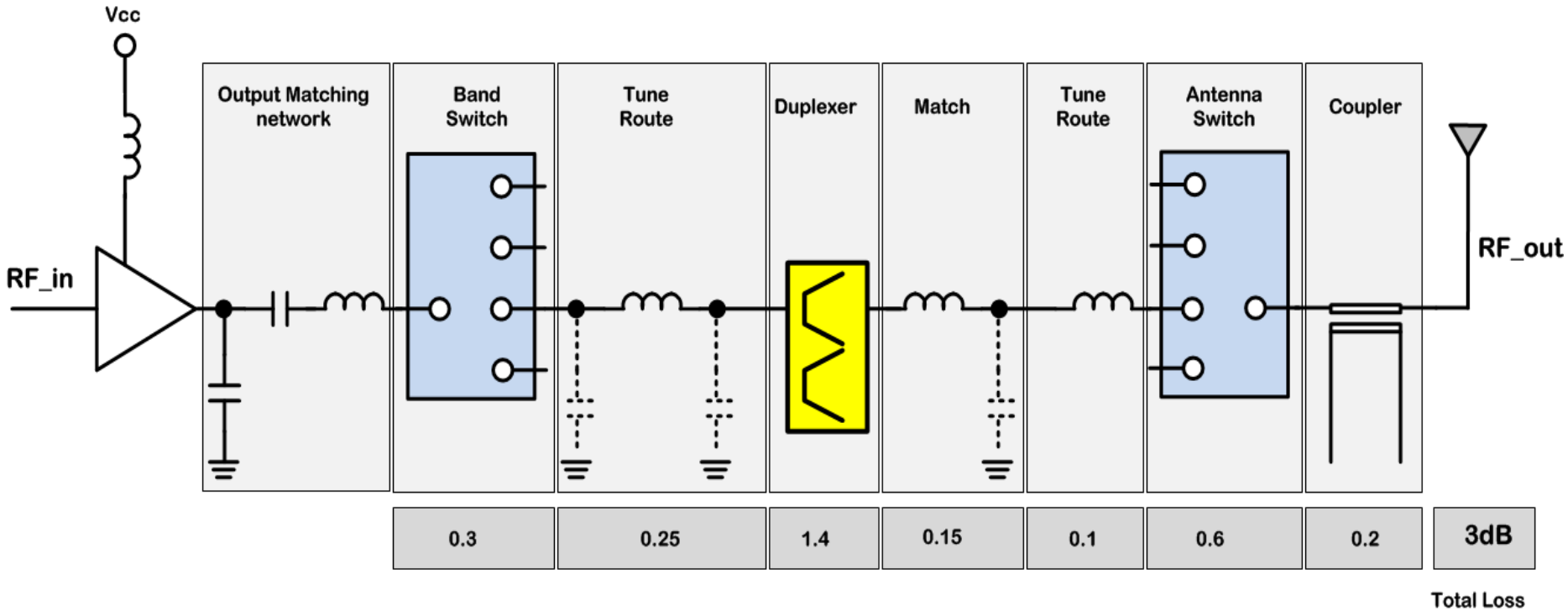
- **Most used structure with/without AC coupling (Cac)**
- **Dedicated ET with error amplifier on ET die**
- **Distributed ET with error amplifier on PA die ---- High BW, low cost**

Peak to Average Power Ratio



- **ET does benefit the higher PAPR modulation**

Power Budget



- **23 dBm at the antenna requires at least 26dBm at PA out**
- **Using a diplexer for CA will add 1.4dB more to the loss**
- **Class 2 for Band 41 requires 26dBm at the antenna**

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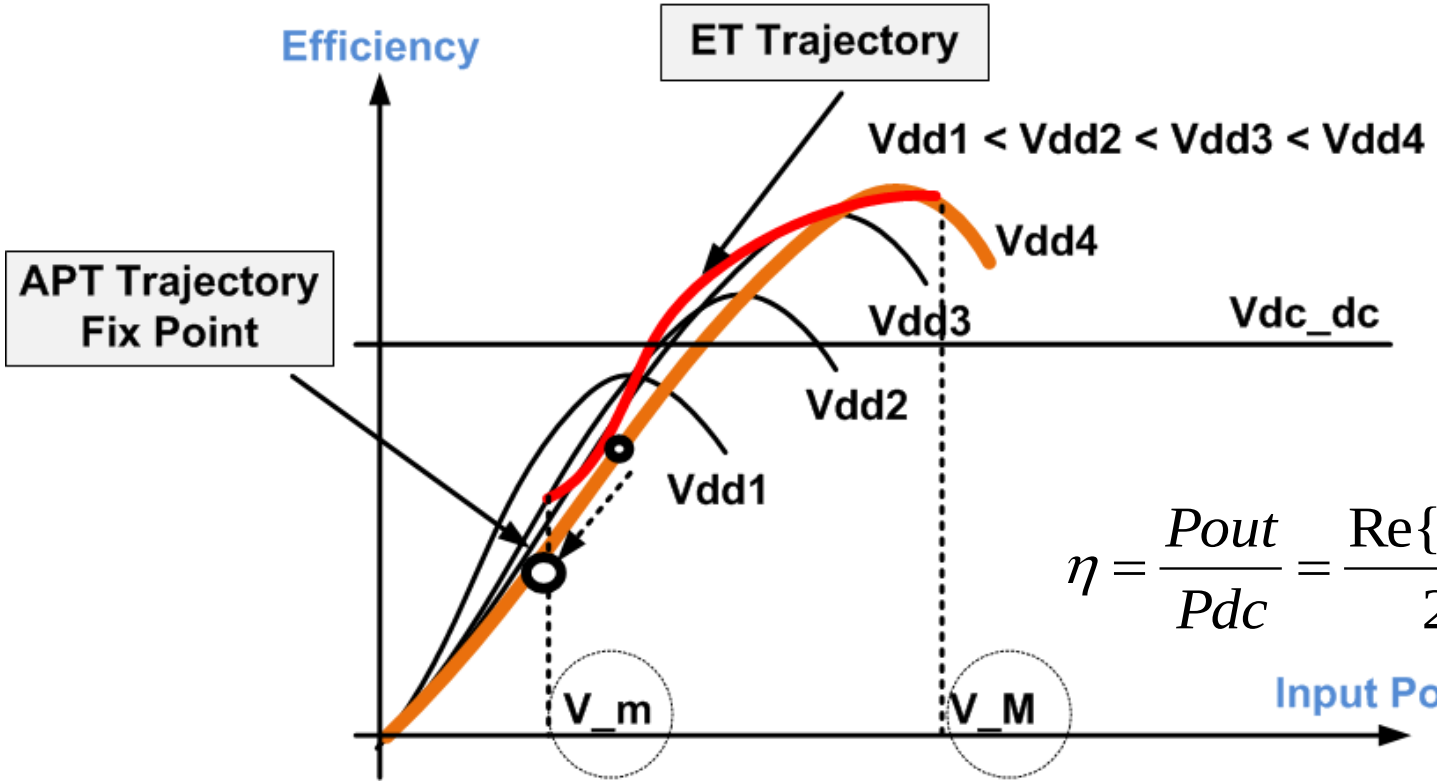
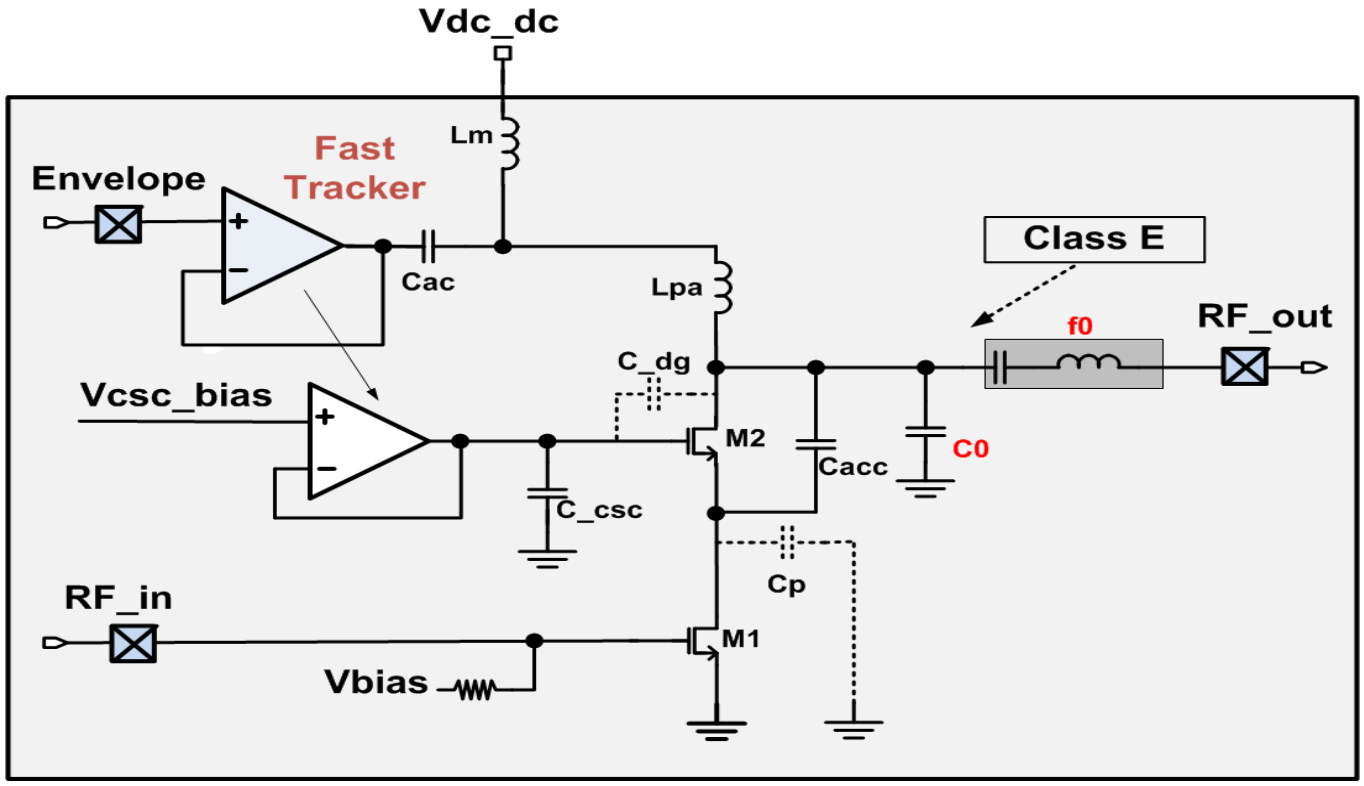
PA Operation Trajectory



$$\eta = \frac{Pout}{Pdc} = \frac{\mathrm{Re}\{Vload * Iload^*\}}{2 * \mathbf{Vdd} * Idd}$$

- **For ET operation we get the best efficiency for each VDD**
- **APT operates the PA in back-off mode therefore requires high Psat**

Three Port Power Amplifier

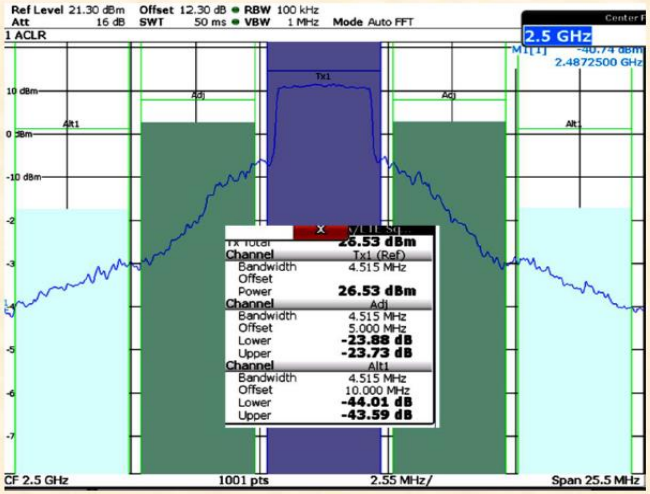


- **Envelope port is the other port to be considered/added**
- **Cacc used for "cascode acceleration"**

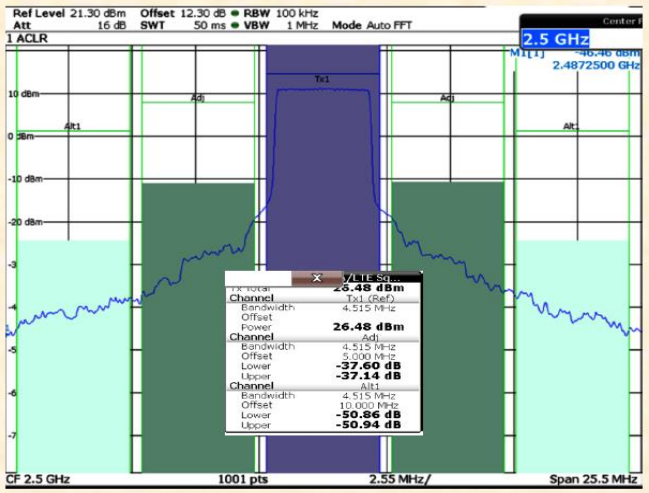
Three Port Power Amplifier

3. Fully integrated broadband CMOS Class-E power amplifier

LTE test data: 16 QAM, 26.5 dBm, 2.5 GHz, V_{dd} = 2.7 V



ET disabled



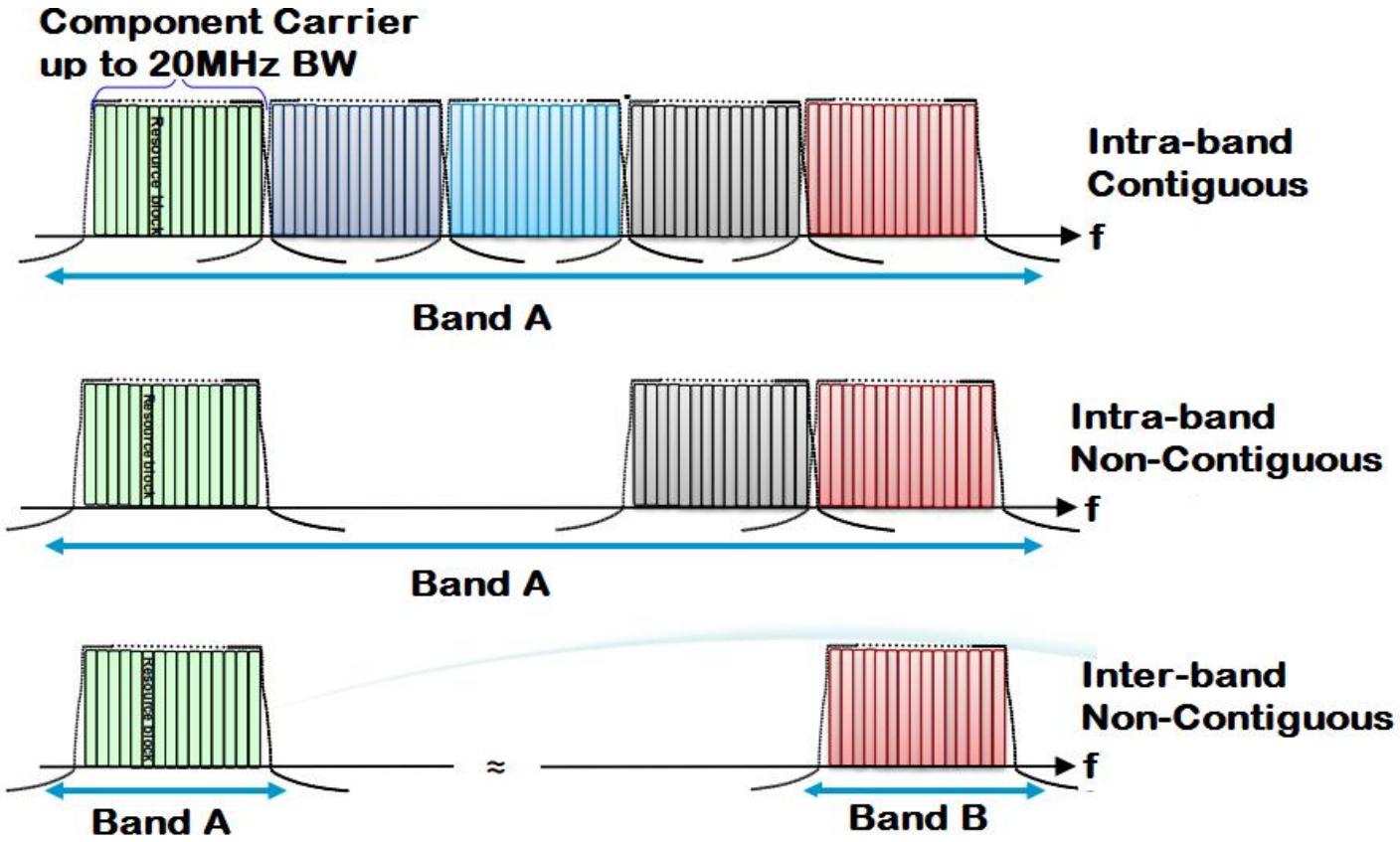
ET enabled

35% overall efficiency
41.5% PA efficiency
ACLR1: 13-dB improvement
ACLR2: 7-dB improvement

- **Three port PA with 35% overall efficiency for B7, 5MHz FDDLTE**

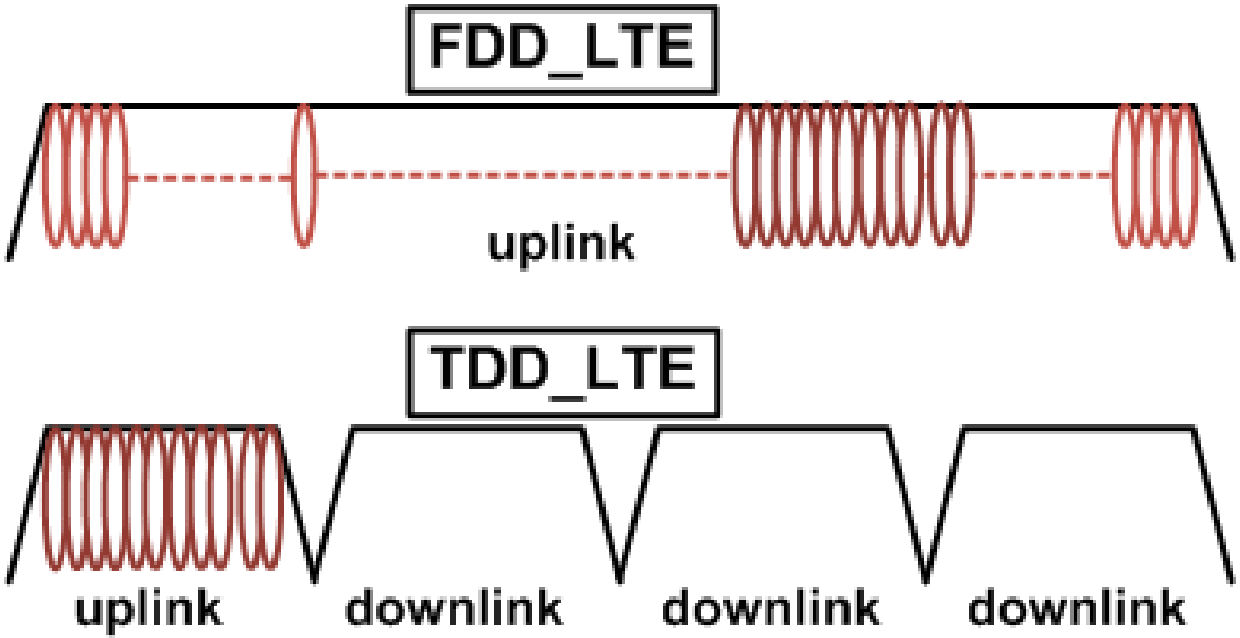
[Grebennikov, Balteanu] –MWC Barcelona 2014

Three Port Power Amplifier



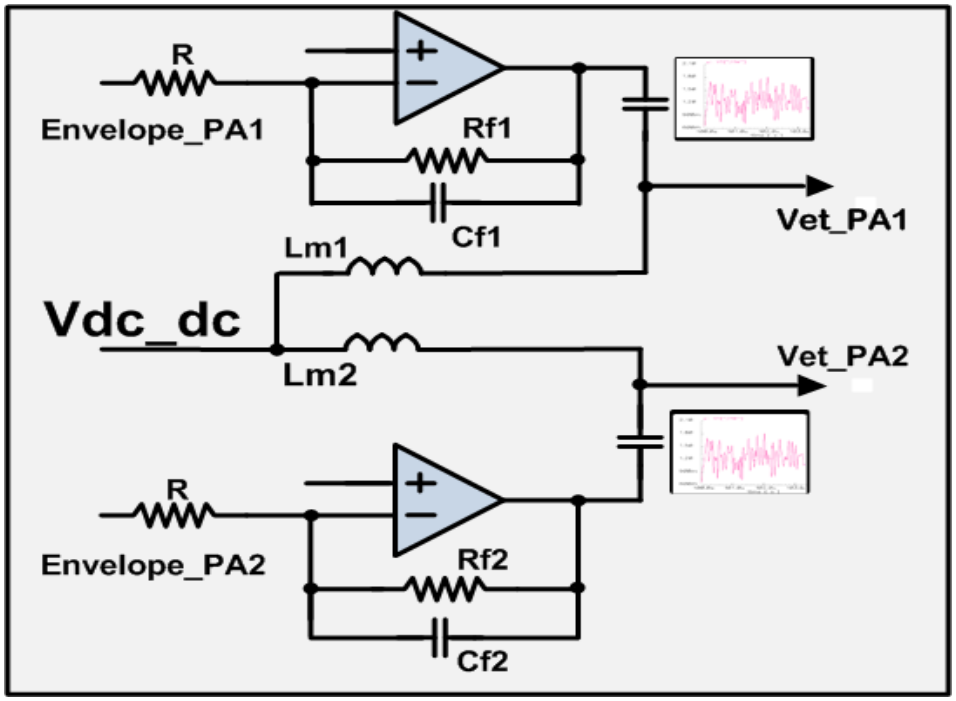
- **Uplink Carrier Aggregation increase PAPR with few dB**

FDD and TDD LTE



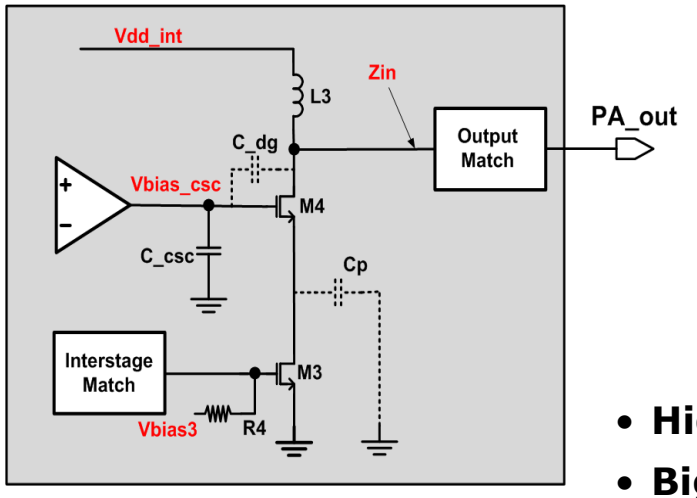
- **TDD bandwidth requirements higher compared with FDD**
- **40MHz 200RBs for TDD is equivalent with 10MHz 50RBs for ¼ uplink/downlink**
- **TDD ET timing has a significant issue compared with FDD ET**

CA Non-Contiguous Bands Envelope Tracking



- **Average Power is aprox. the same for both bands**
- **Reuse the DC_DC common voltage**

Power Amplifier Losses



$$Plost = Pbias + Pswitching$$

$$Pswitching = \frac{1}{Frf}\int_0^T idd(t) * vdd(t) * dt = \frac{Vdd}{T}\int_0^T idd(t) * dt$$

$$Pswitching = Cp * Vdd^2 * Frf$$

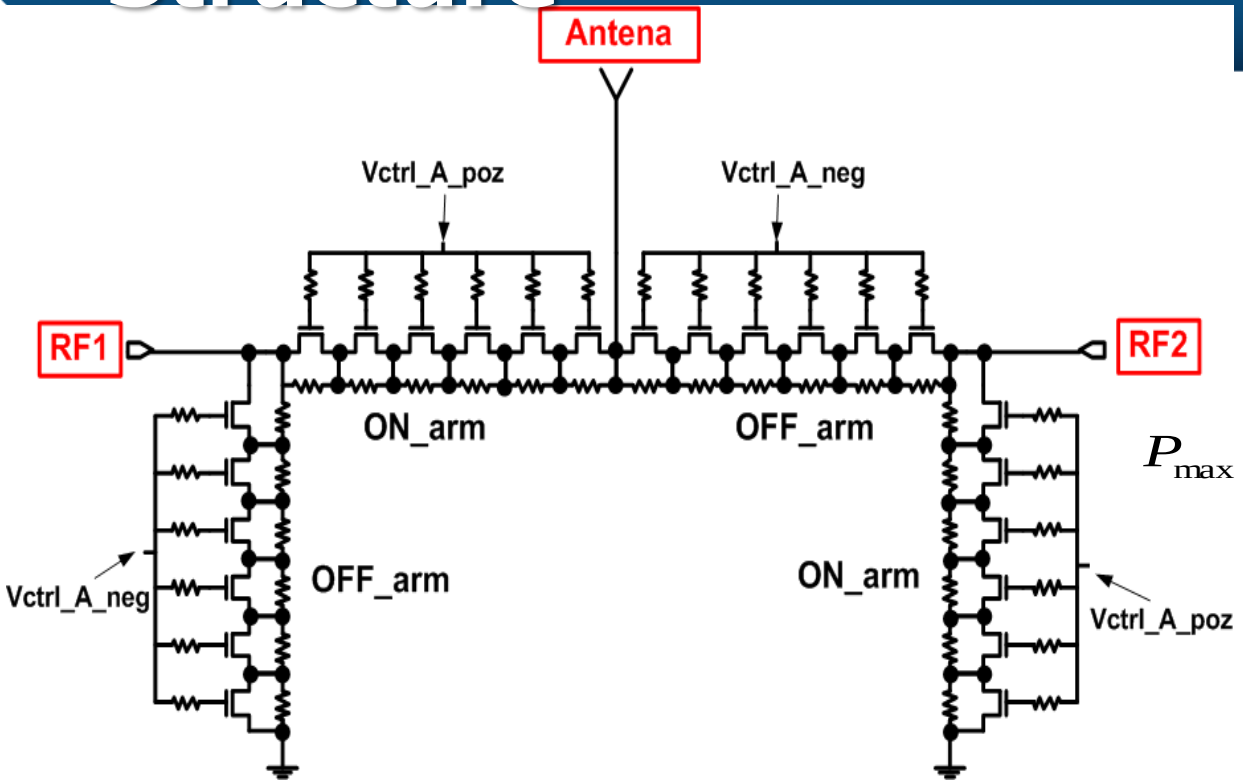
- **Higher load line (Rload) -----> Higher switching loss**
- **Bigger CP & Bigger transistors -----> Higher switching loss**

$$Ploss\_match \cong$$

- **PAE reduction is 1% for every 0.1dB IL in Output Match at 40% PAE**
- **0.8dB IL reduces the PAE by 8%**

Higher Load line good for low matching losses but not good for switching loss

SOI Switch Structure



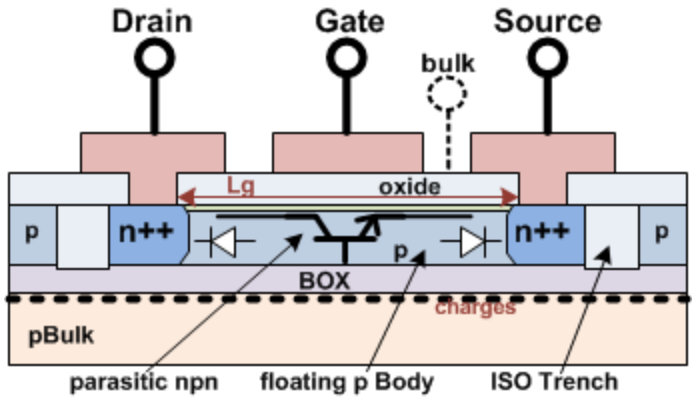
$$R_g >> \frac{1}{2\pi(C_{gs}+C_{gd})}$$

$$\left|V_{DS\_peak}\right| = 2(V_{Th} - V_{NEG})$$

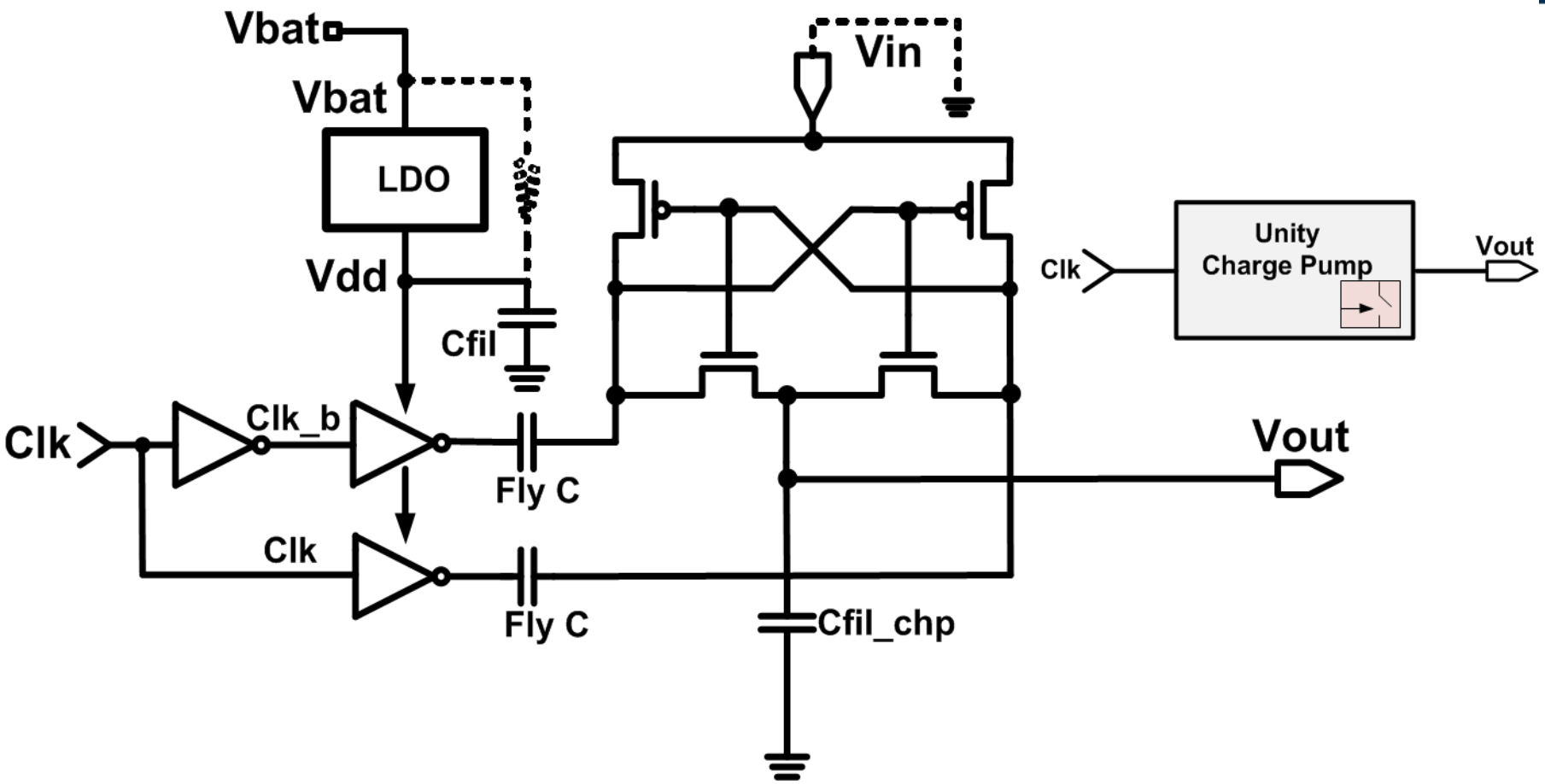
$$P_{\max} = \frac{V_{Tx\max}^2}{2 * Z_0} = \frac{2(nV_{DS\_peak})^2}{Z_0}$$

$$R_{on} \propto \frac{n}{W_g(V_{POS} - V_{Th})}$$

$$FM = R_{on}C_{off}$$

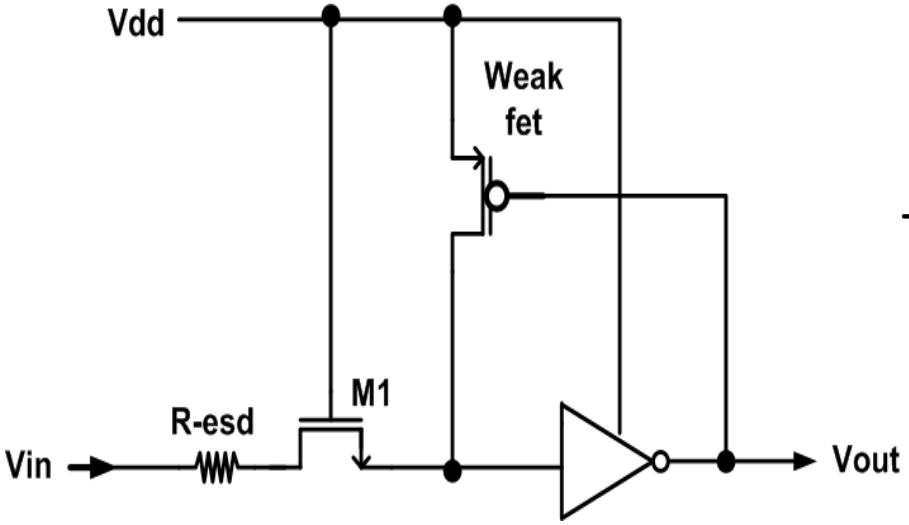


SOI Switch Control Circuitry - NVG

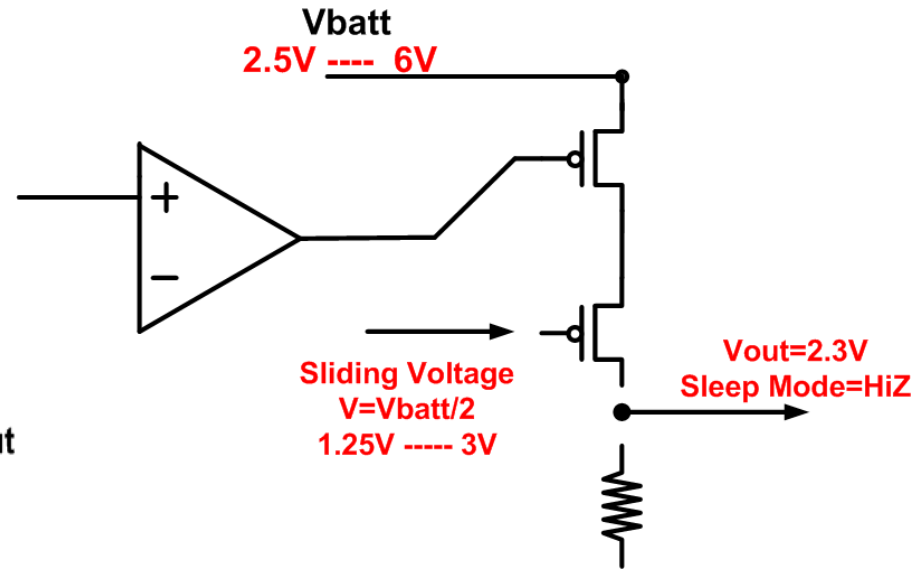


- **Generates negative voltage for Switch OFF operation**

SOI Switch Control Circuitry

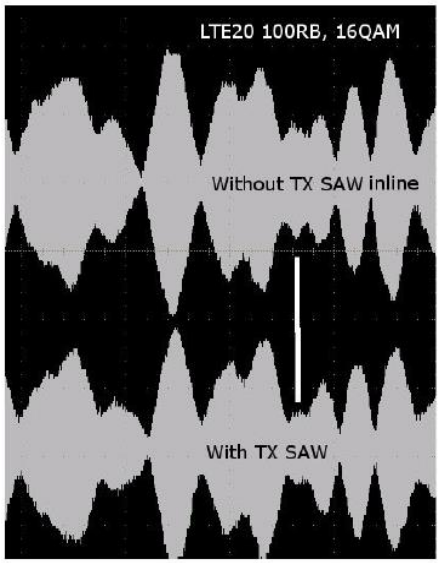


$$Vin \geq 2Vds\_\max$$

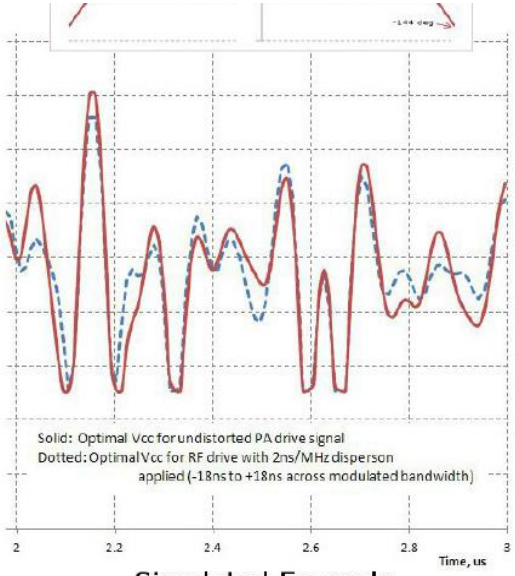


- **SOI Switches usually are battery connected**
- **GPIO Switch operation**

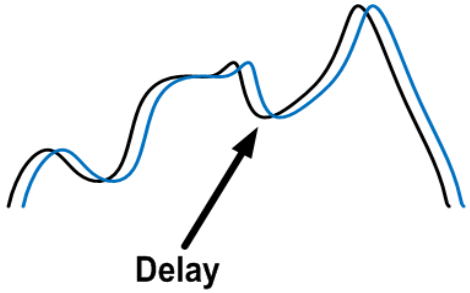
Envelope Tracking Delay Alignment

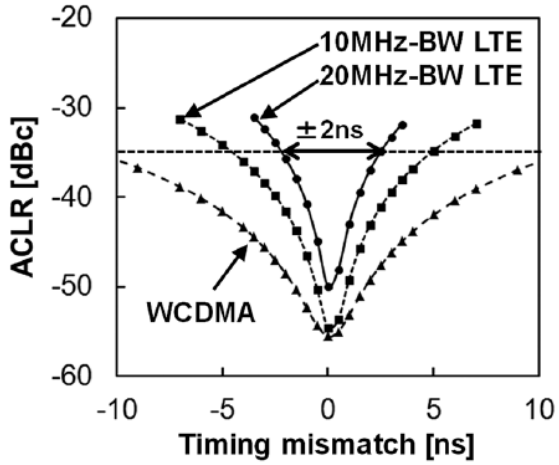


Measured Example



Simulated Example





- **ET Analog Interface require a global delay alignment**
- **Group Delay and PCB board low pass filter makes alignment difficult for high BW such as LTE 20MHz and higher BW**
- **Need to rethink the interface for higher data rate BW**

Conclusions and Discussions

- **Conclusions**
- **Discussions**
- **THANKS！ 谢谢！**