Co-Design of RF Chips and Modules for RF Solution

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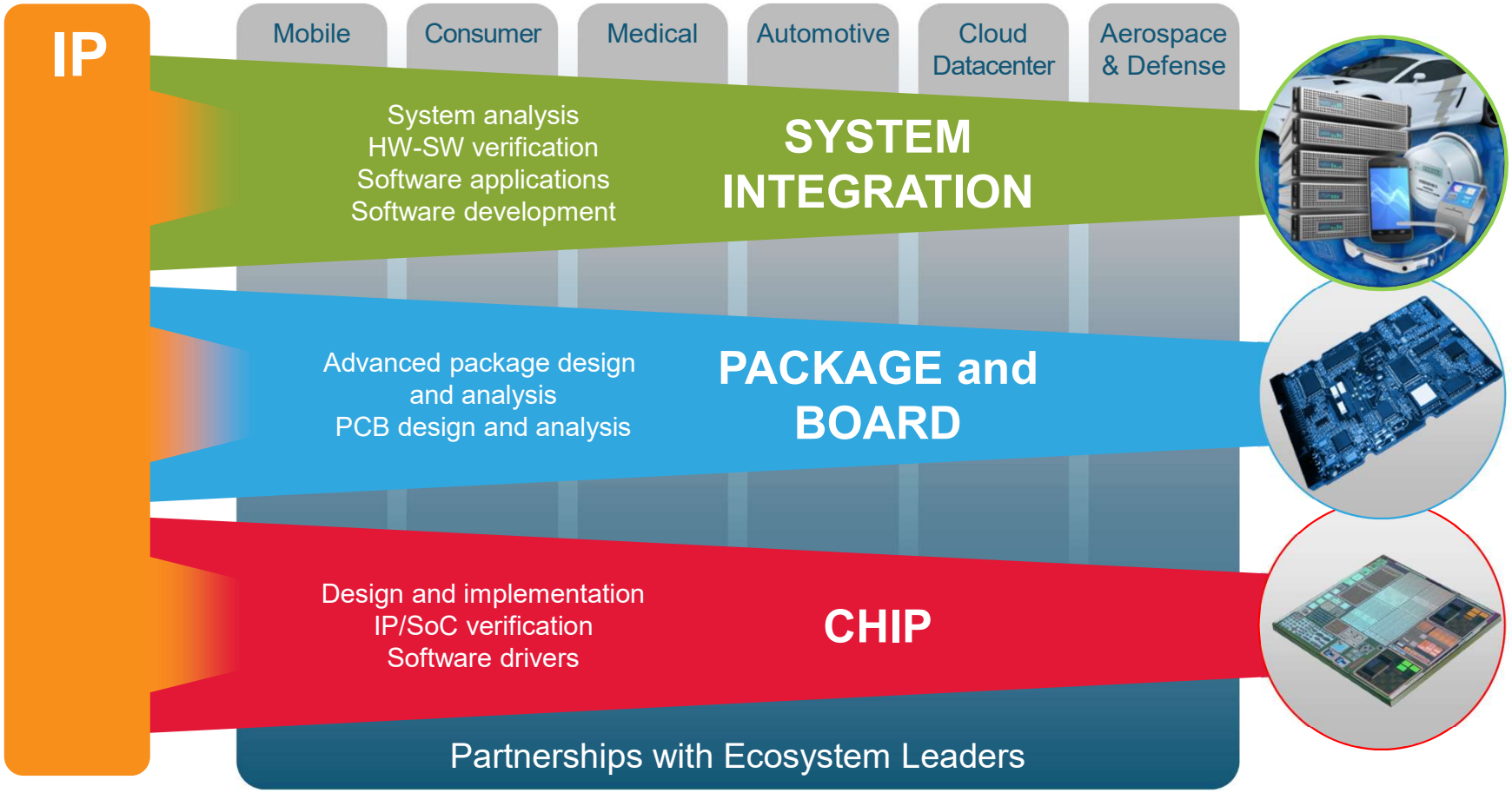
Outline

- Introduction
- New System-Level Solution for RF Design
- Example

System Design Enablement (SDE).



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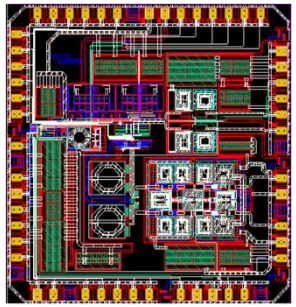
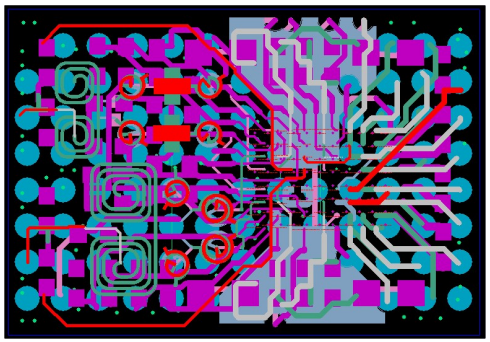
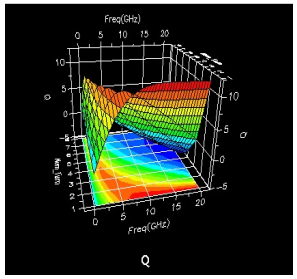
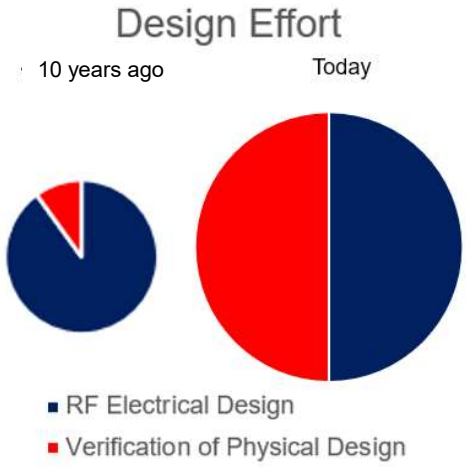
How is RF Design Evolving?







- 10 years ago
  - RF designs smaller in size and complexity
  - Majority of design effort in electrical design
  - Because of the physical design simplicity, minimal verification needed a small portion of design time
- Today
  - Overall RF design effort larger
  - Verification has dramatically increased as part of the flow and in some flows is a larger effort than the RF design itself



- RF design complexity is rapidly outpacing traditional, disjointed design flows
- Market is rapidly expanding: 5G (24-40GHz), automotive (77-81 GHz)
- Module content is increasing: 5-6 technologies (CMOS, SOI, GaAs, GaN, SMD, laminate, package). With BAW, SAW, and FBAR filters, up to 20 ICs in an RF module
- Reduced packaging size does not allow for traditional RF type design flow

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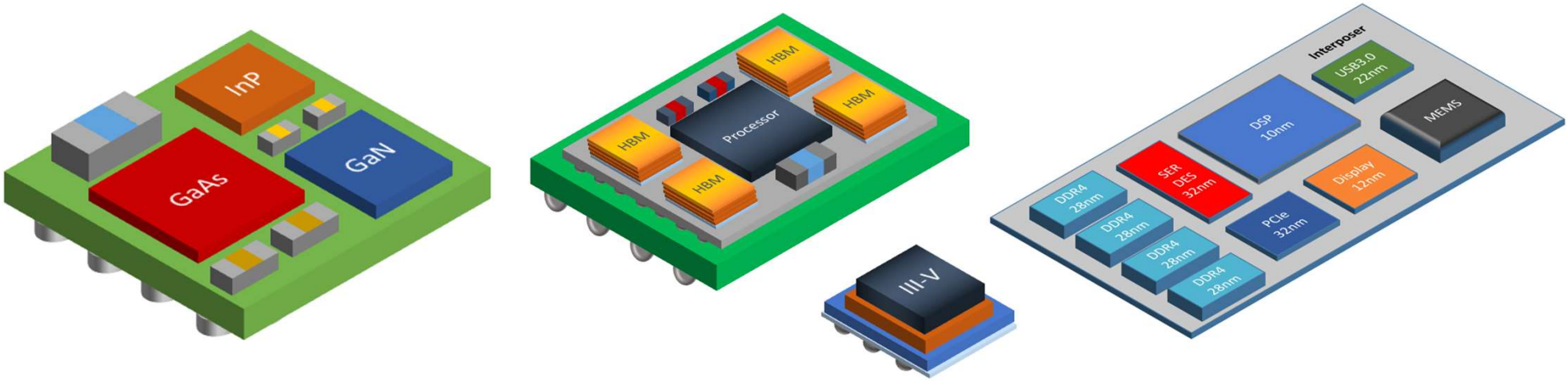
How is Advanced Packaging Evolving?



PCB Style Design Flows | IC Style Design Flows

Multi-Chip Module (MCM)

System in a Package (SiP) RF Module

Heterogeneous Integration

1970 — 2005 — Now — Future

Aerospace & Defense

Integration of III-V devices with focus on reliability. Goal: Reduce the size/weight of the PCB by integrating bare, un-package dies into a single design

Smart Phones

Provide self-contained analog/RF systems/subsystems in a single package. Goal: Simplify the PCB-level requirements by integrating multiple bare die in a in a reduced form-factor required to fit into handheld commercial devices.

2.5D & 3D IC

Three-dimensional stacking for memory and CMOS image sensors. Processor with 3D memory stacks, integrated on a silicon interposer

Disaggregated SoC

Alternative to Moore's Law and dimensional scaling of a single device. Leverage design re-use paradigm that drove SoC with blocks built from varying nodes, integrating them on a single device.

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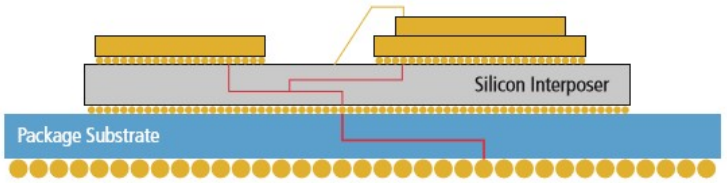
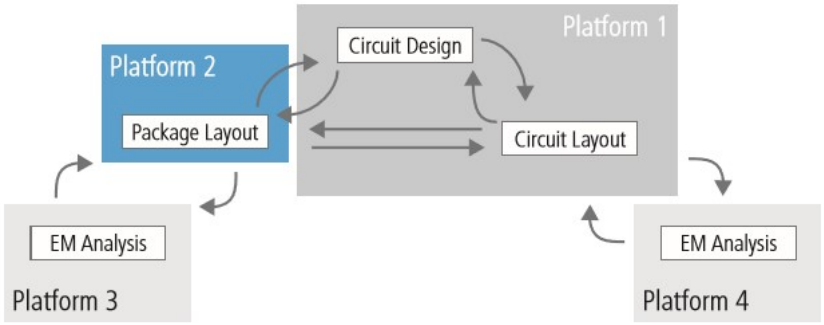
Existing Design Flow





- Different design teams still use disparate EDA tools for various design aspects of electronic products
- Fragmented design flows are unable to meet new challenges:
  - Increased system complexity
  - Increased circuit complexity
  - More stringent bandwidth requirements
  - Reduced operating power requirements
  - Shrinking device sizes
  - Greater process complexity
  - Evolving packaging and manufacturing requirements
  - Product size restrictions
  - Mounting costs
- Different portions of these extremely complex designs interact with one another and need more than the usual time for verification

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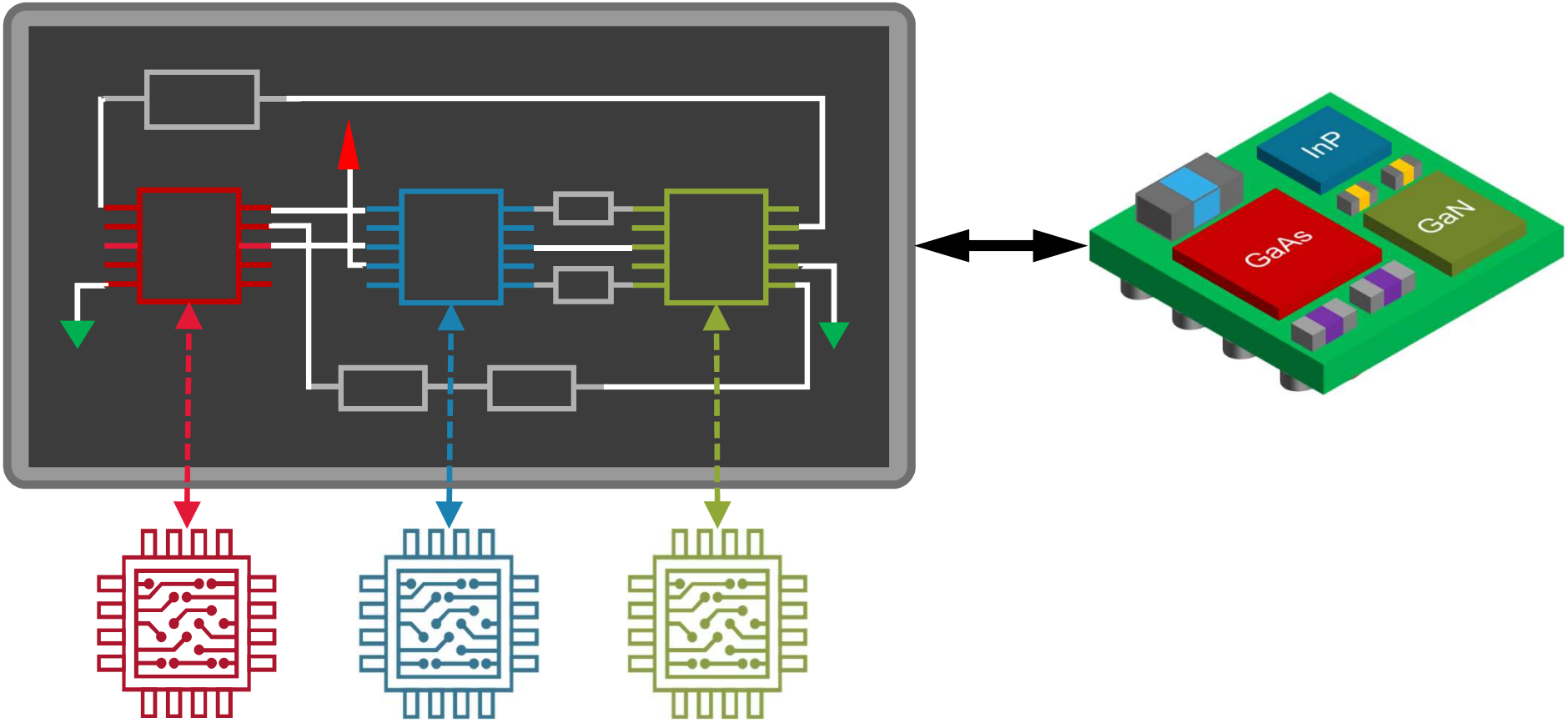
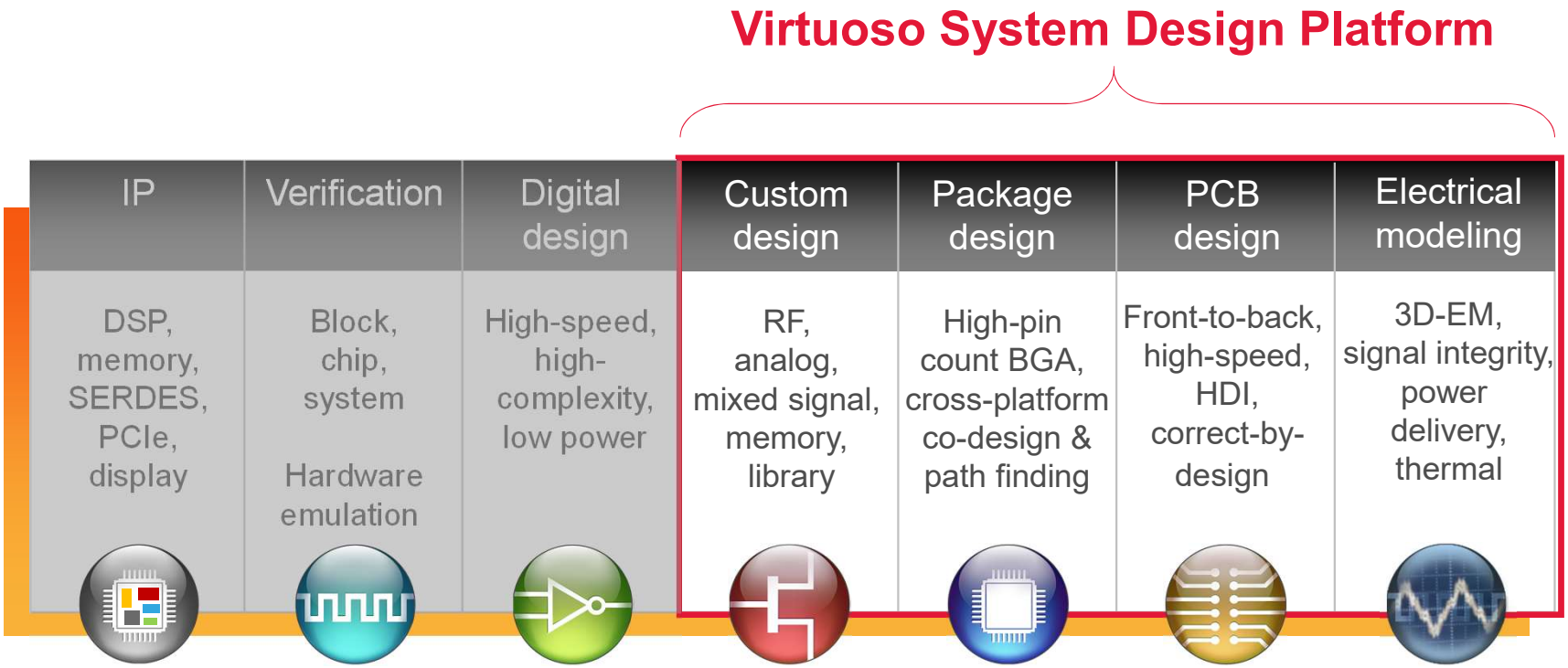
SDE…Bridging Analog/RF IC Platform to Advanced Packaging Solutions to Support Multi-Chip(PDK) Designs



Cadence Solutions



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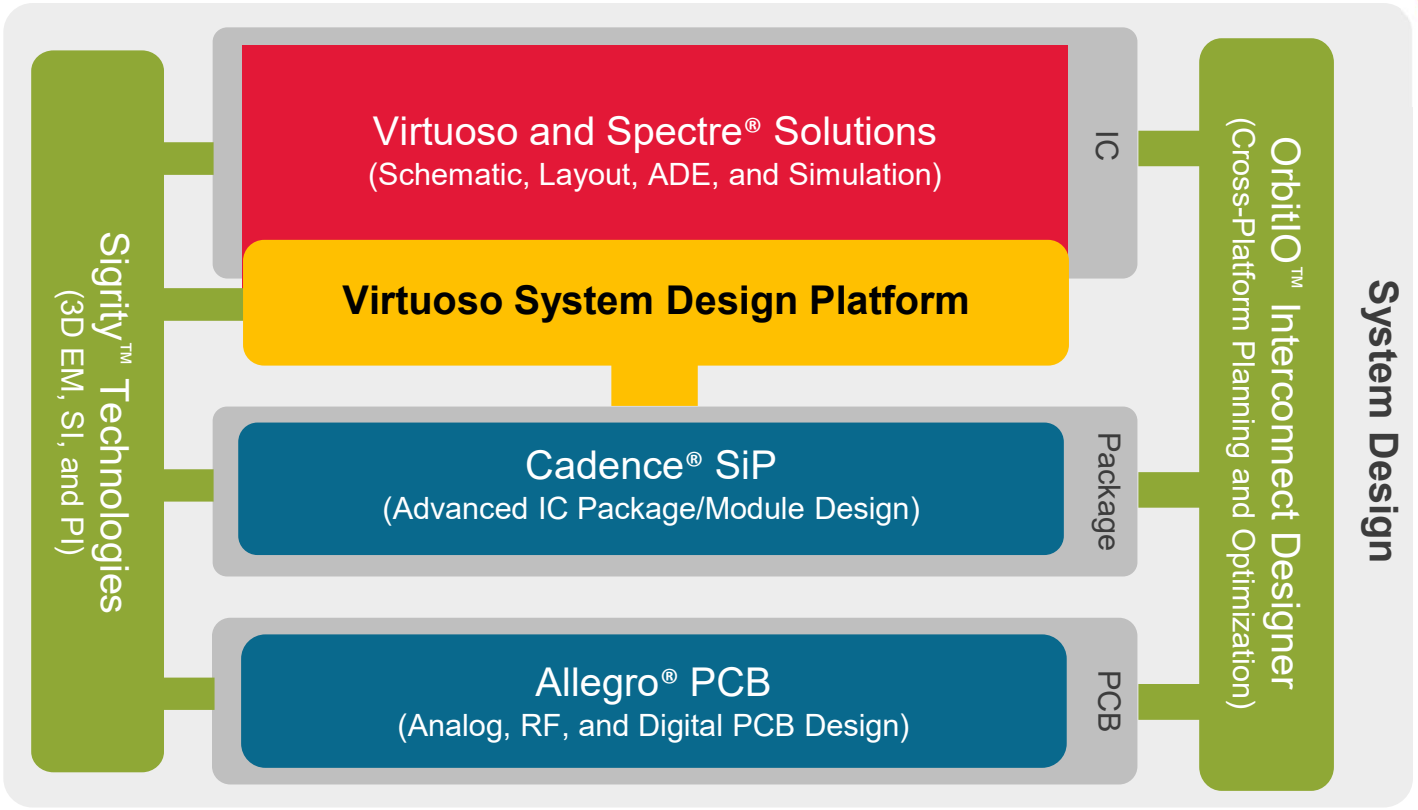
Virtuoso System Design Platform

Extending IC Design Into System Design



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Primary Flows

Implementation
(Top-down)

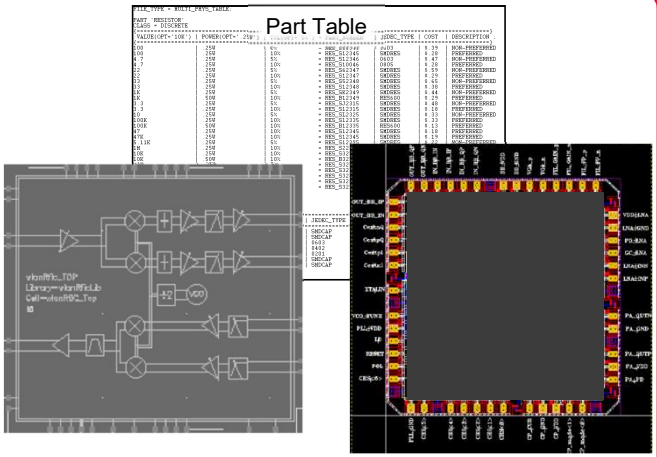
- ✓ Capture and manage system/package level devices and connectivity from schematic editor to package technologies
- ✓ Automatic library generation for package-level devices
- ✓ Die exchange flow with LVL
- ✓ Support for LVS, BOM, and project archiving

Analysis
(Bottom-up)

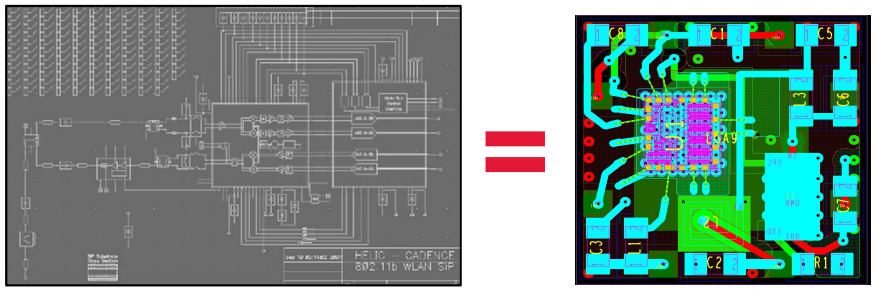
- ✓ Import system-level connectivity and layout parasitic data into Schematic Editor for “system aware” IC design
- ✓ Intelligent n-port S-parameter and RLGC models to streamline testbench-ready schematic creation

Implementation Flow

- Seamless die exchange between IC and package
  - Create die footprint (Allegro format) and schematic symbol (Virtuoso SE format) from IC layout in Virtuoso LS based on new “chips” view
  - Supports exchange of top metal (RDL) routing
  - Includes co-design flow with layout vs. layout checking
- Single “golden” schematic for implementation and analysis
  - Native netlist data for Allegro used for bi-directional flow between Virtuoso and Allegro technologies
  - Additional package/board-level properties inserted with part table file (PTF) support to support full documentation (BOM, etc.)
  - Package-level layout vs schematic (LVS) checking
- Cross-platform layout constraint synchronization
  - Synchronization of Virtuoso SE and Allegro constraint managers



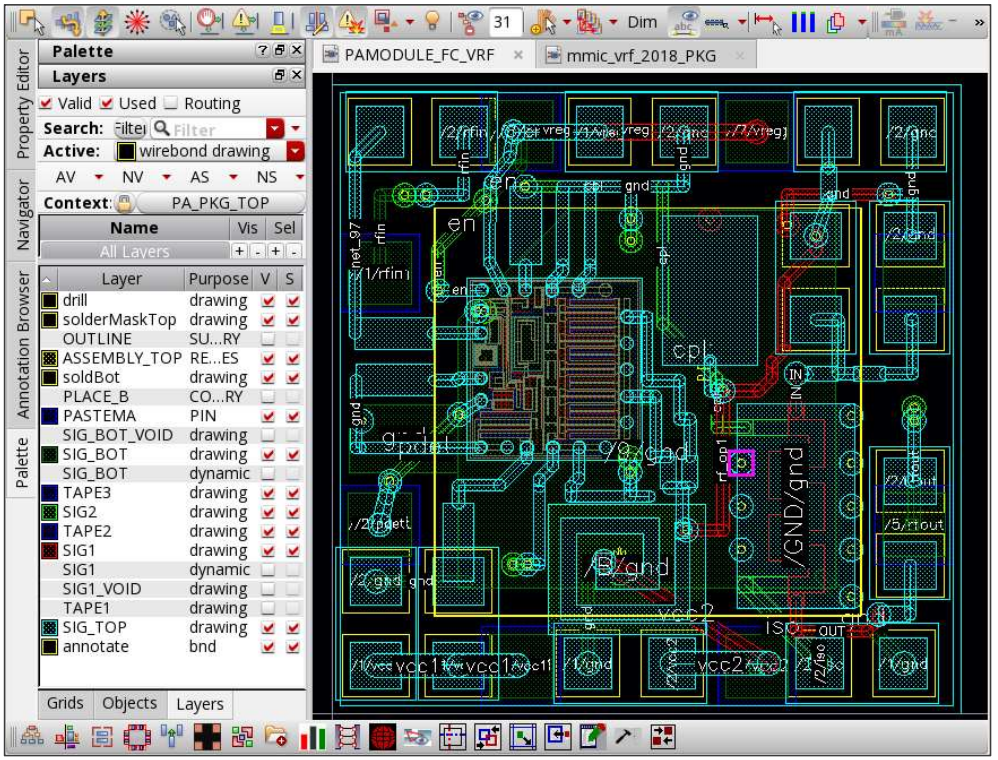
“Chips” Cell View



Automated Logical to Physical Verification

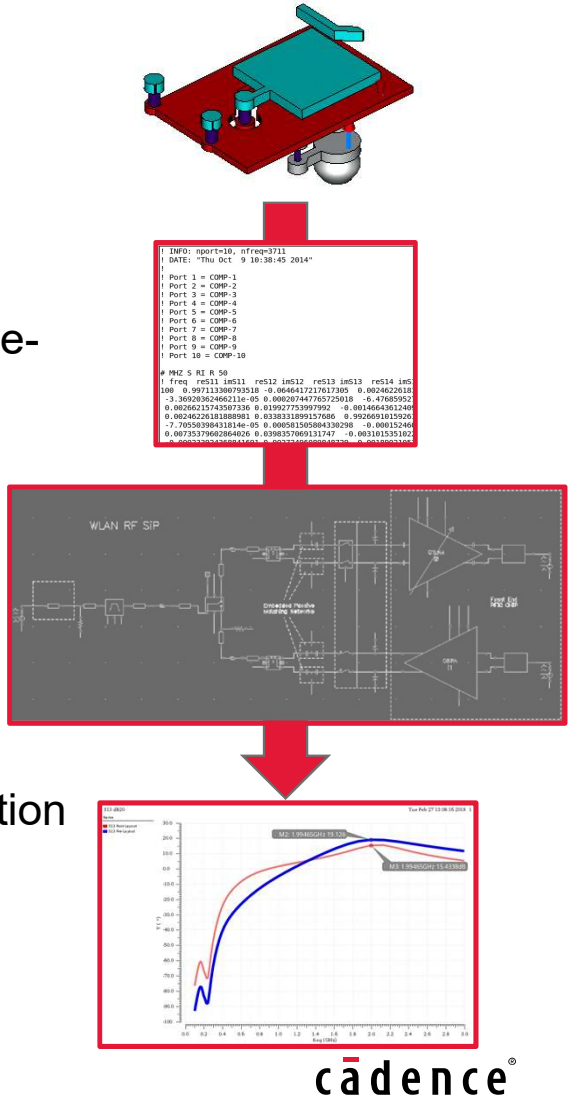
Implementation Flow

- Virtuoso Multi-Tech (VMT) framework
  - Includes all VSDP capabilities
  - Includes OA⇔SIP
  - Enablement for future “system-level” flows
    - 2.5D & 3D IC, Photonics, etc.
- Additional multi-die capabilities available
  - Package/module-level layout capabilities provided in Virtuoso Layout Suite EXL
    - All angle component placement
    - Copper pour with auto-voiding
    - Wire-bonding
  - “Edit in concert” chip and package co-design capability
    - Simultaneous editing of IC layout(s) and package layout



Analysis Flow

- Tight integration between PCB/package layout databases and Sigrity™ PowerSI® 3D EM extraction engine
  - Supports partial/full nets, groupings and device-level modeling
  - Generates “smart” n-port with direct pin mapping and eliminates double-counting of discrete devices
  - S-parameters and RLGC
- Automatically create extracted views that include the layout parasitics from package and PCB
  - Automatic schematic generation/update (golden source schematic) with layout parasitics from package/board
- System-level, layout parasitic aware testbench creation
  - GUI-based method and streamlined binding, simplifies testbench creation
- Multi-technology netlist extraction into Virtuoso ADE
  - Eliminates issues with potential model collisions and netlisting procedures (namespace conflicts) across different PDKs



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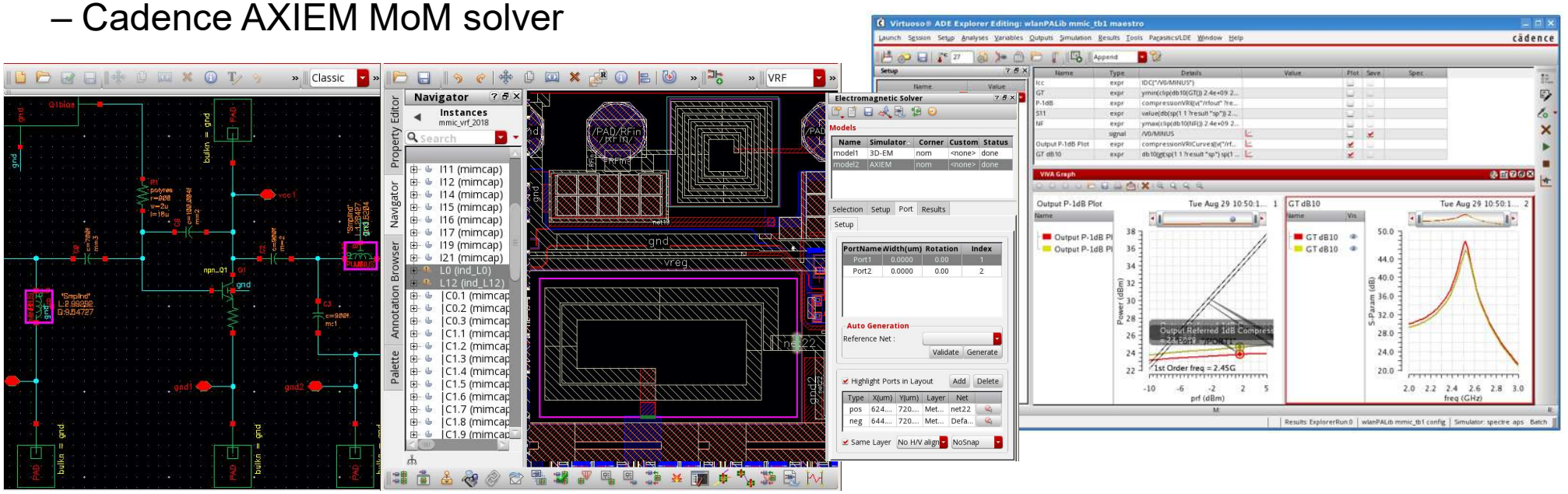
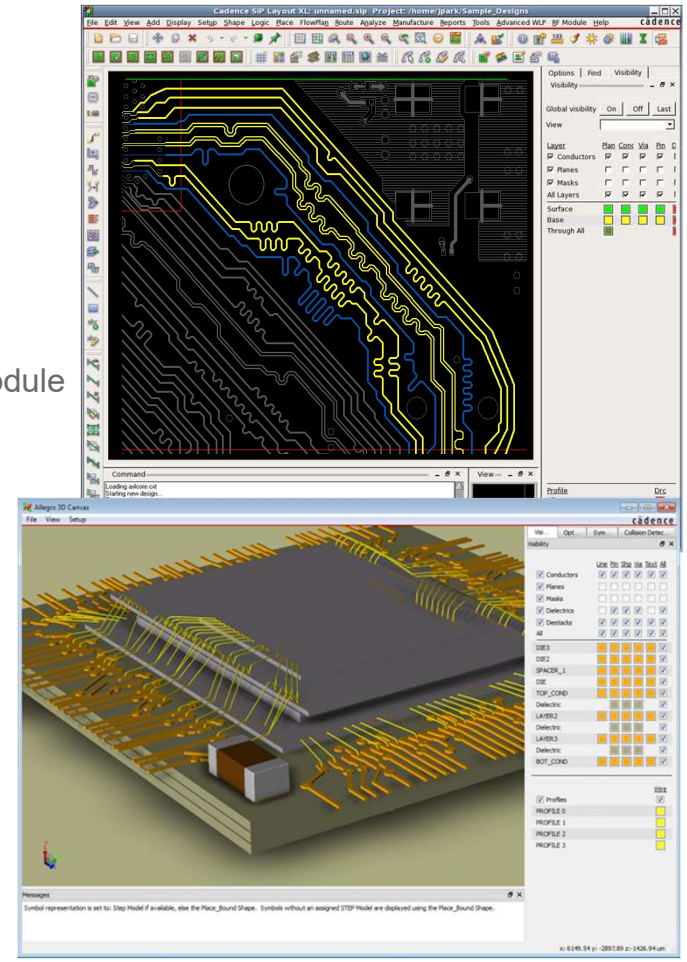
Analysis Flow

- Integrated field-solvers with Virtuoso Layout Suite for on-chip and off-chip device-level modeling
  - Includes automatic annotation to Virtuoso Schematic Editor
  - Quasi-static, Full-wave FEM and hybrid solvers
  - Cadence AXIEM MoM solver



Package Layout

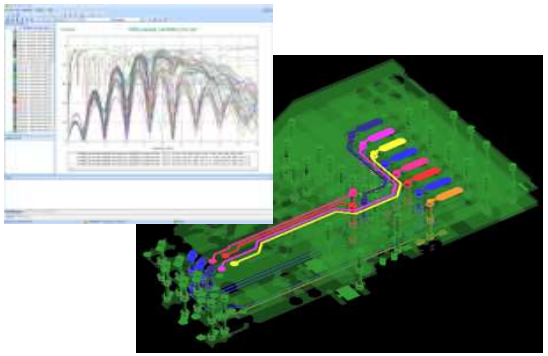
- Architected as a package/module design solution
  - Correct-by-construction with real-time DRC
  - Incredibly flexible connectivity use-model
    - Schematic and/or table and/or spreadsheet
    - Connectivity on-the-fly
  - Technology file-driven package substrate style stack-up
    - Unlimited substrate material types
      - Laminates, Ceramics, Glass, Flex, etc
    - True die model, die-stack editor, embedded devices, cavities, all package/module substrate materials supported
  - Industry leading wire-bonding
    - True 3D profiles, 3D overlap checking, multi-die/multi-tier, platting tails/bars, etch-back
  - Advanced package-specific push/shove and automatic routing styles
    - Radial, all angle, flip-chip
  - Package-specific checking and reporting
    - BGA ball-maps, bond wire diagrams
  - PCB & IC manufacturing outputs
    - IPC-2581, Gerber, GDSII, etc.



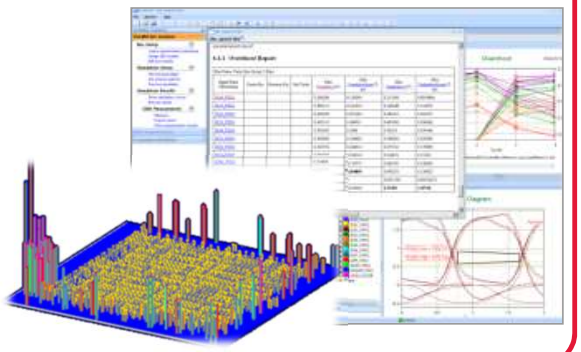
Integrated 3D EM Modeling

- Technologies for 3D EM, signal integrity and power delivery modeling
  - ✓ Extraction with hybrid solver, quasi-static, and full-wave 3D-EM engines
  - ✓ Able to address the broadest range of single or multi-die packages
  - ✓ Power-aware signal integrity analysis
  - ✓ Advanced multi-gigabit channel analysis
  - ✓ Industry-leading IBIS-AMI modeling support

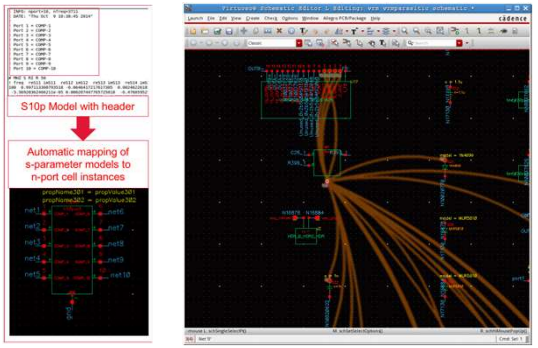
EM Extraction



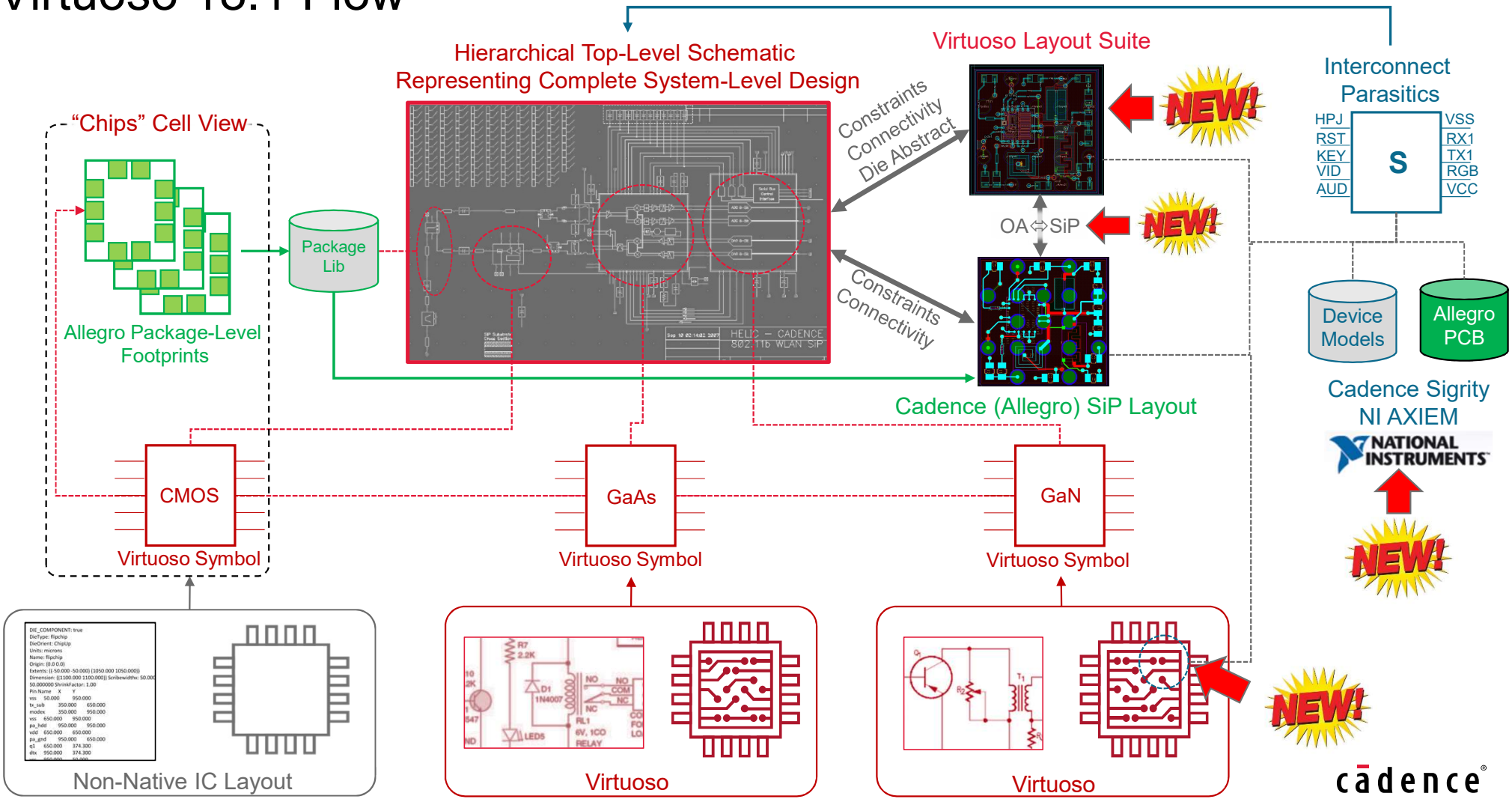
SI & PI Simulation



Schematic Interface



Virtuoso 18.1 Flow



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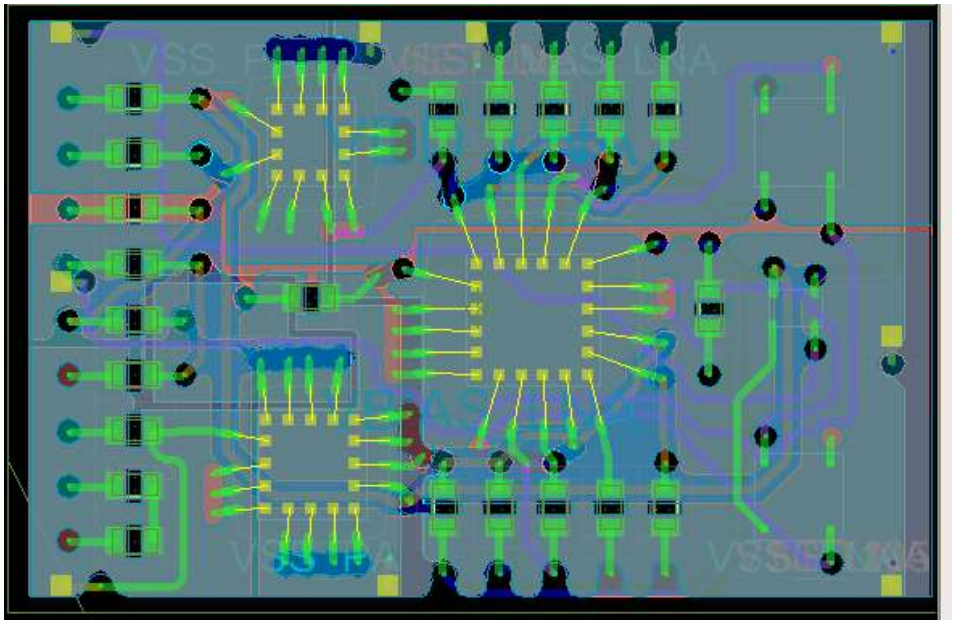
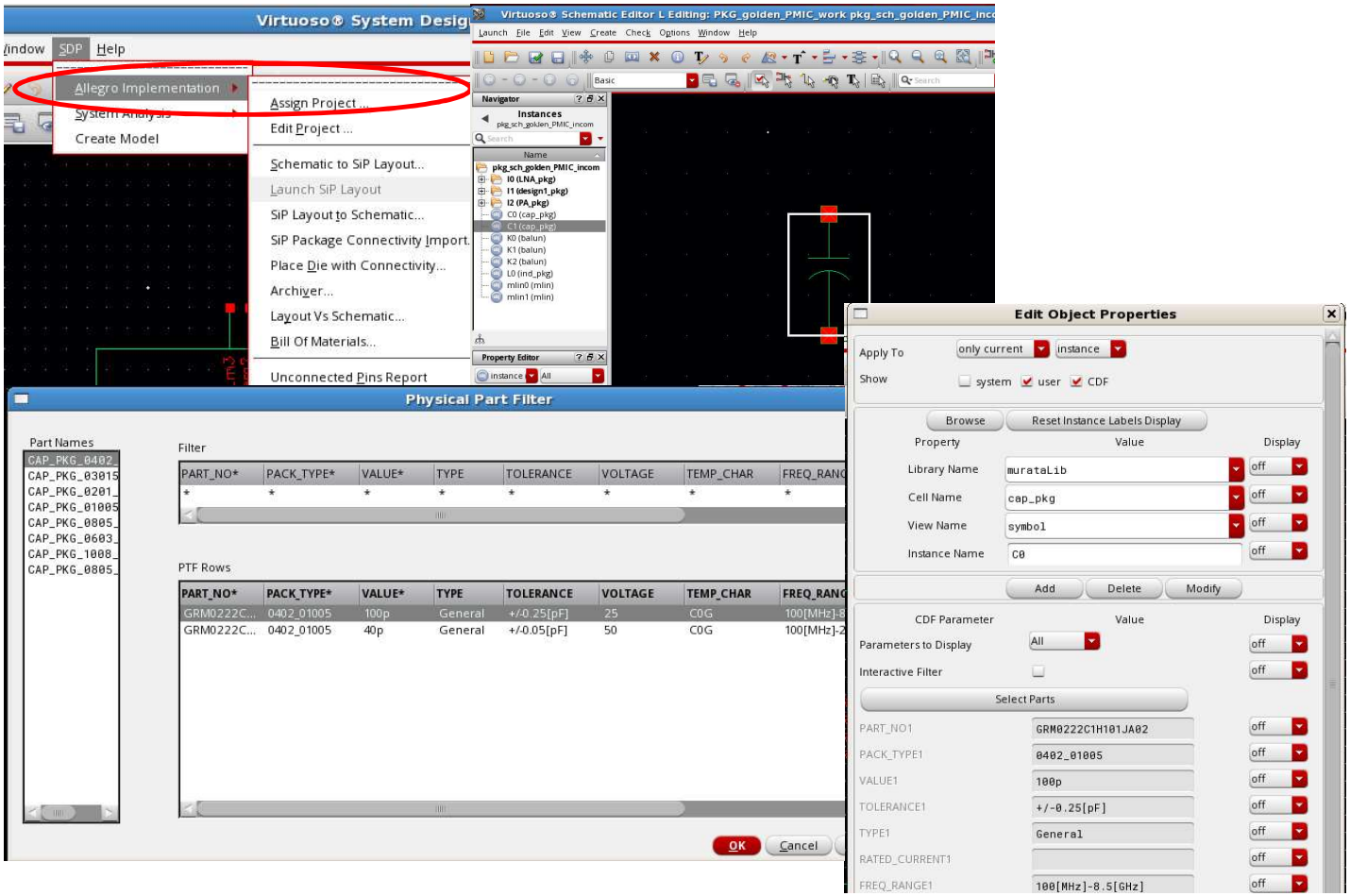
System Description

- RF front-end module @ 2.4GHz consisting of
  - 45nm CMOS LNA (Low-noise amplifier)
  - 90nm CMOS PMIC (Power management integrated circuit)
  - 1um GaAs HBT MMIC power amplifier
  - Off chip SPDT switches, baluns and passives
- 8-layer laminate SIP



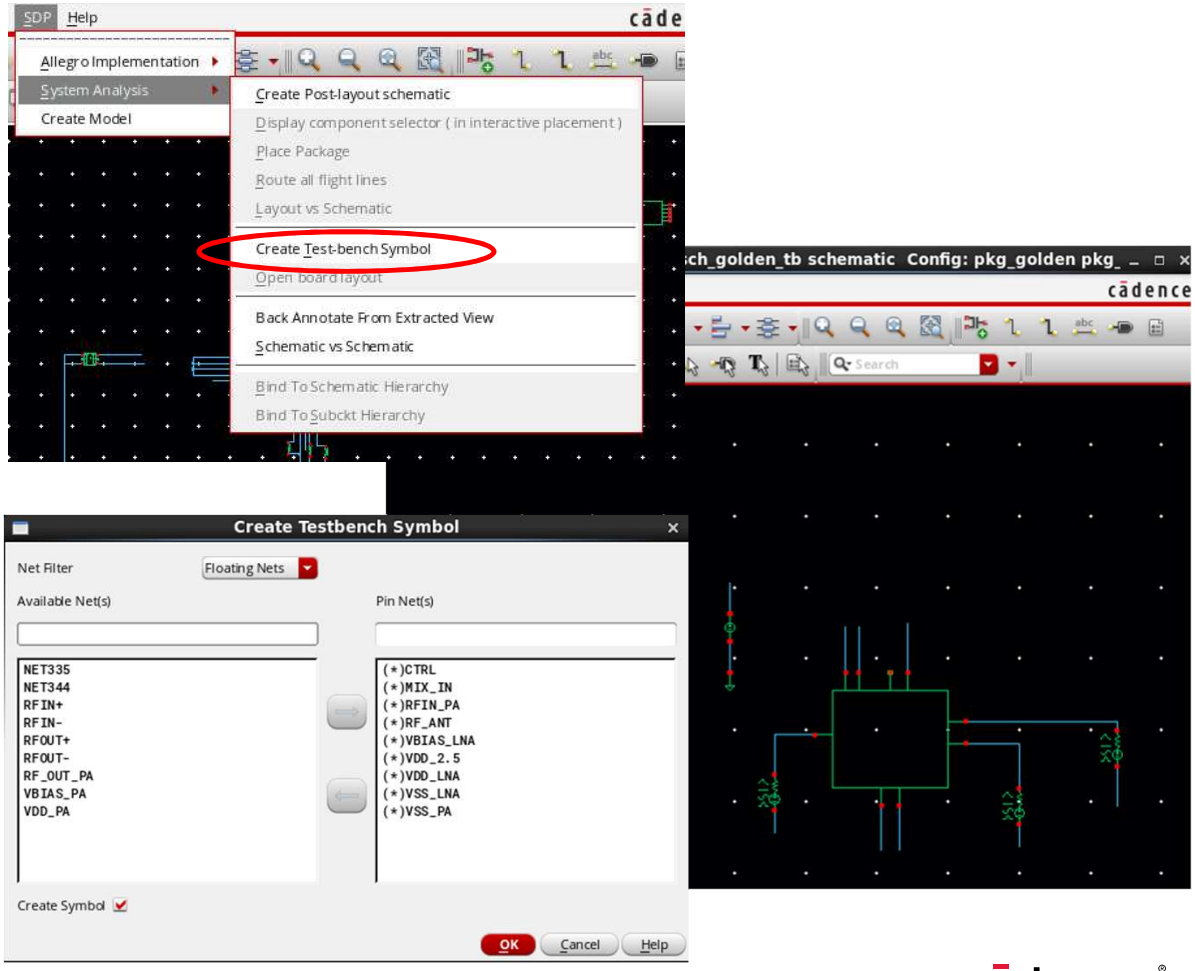
Create Hierarchical System-Level Schematic

- Assign a project to have access to board libraries
  - Shared footprints and models with Cadence SiP Layout
- SiP-level components
  - Can import from Allegro library
  - Simulation models included for easy simulation setup
  - Part Table files enable seamless property mapping



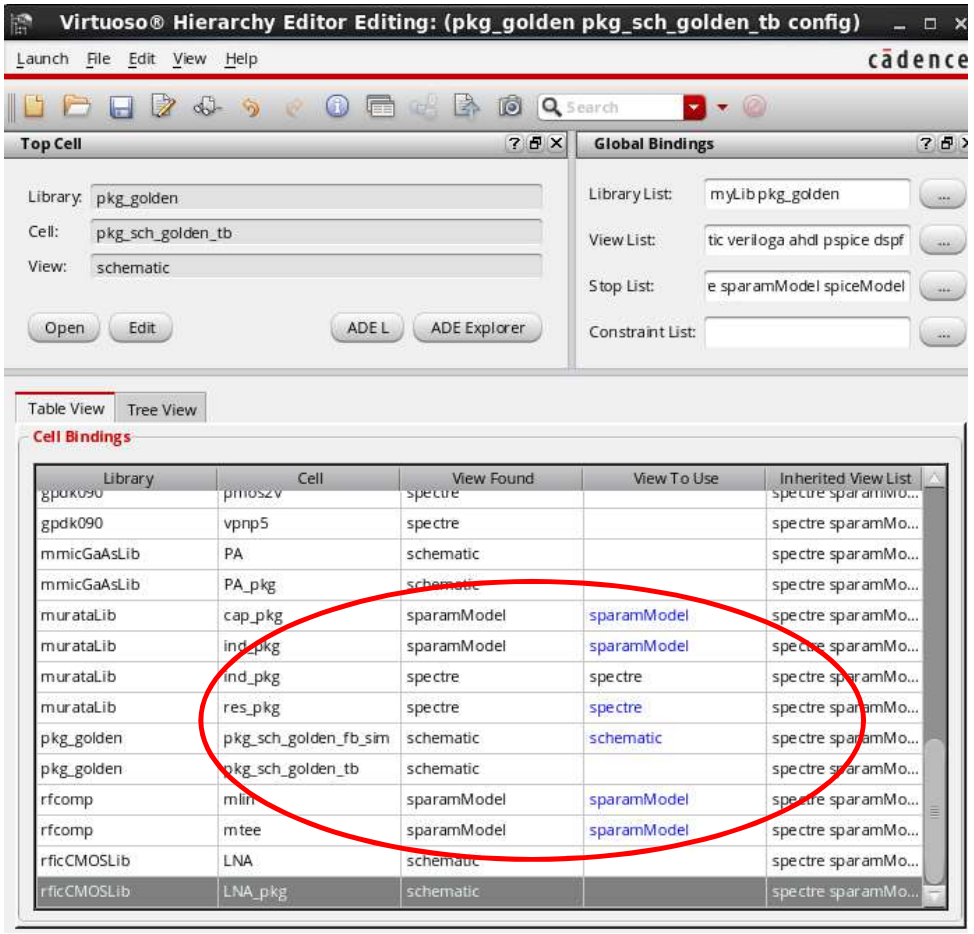
Testbench Symbol Auto-Creation

- Auto-generated schematic may have huge number of nets and ports
- Need efficient method to create smaller symbol for simulation purposes
- Create Testbench Symbol allows user control of pins for simulation symbol



Creation of Configuration Views Using the Hierarchy Editor

- Use familiar Hierarchy Editor to control simulation views
- Package components have multiple simulation views
  - Spectre® for ideal primitives
  - sparamModel for imported s-parameter models
  - Schematic for SiP design schematics



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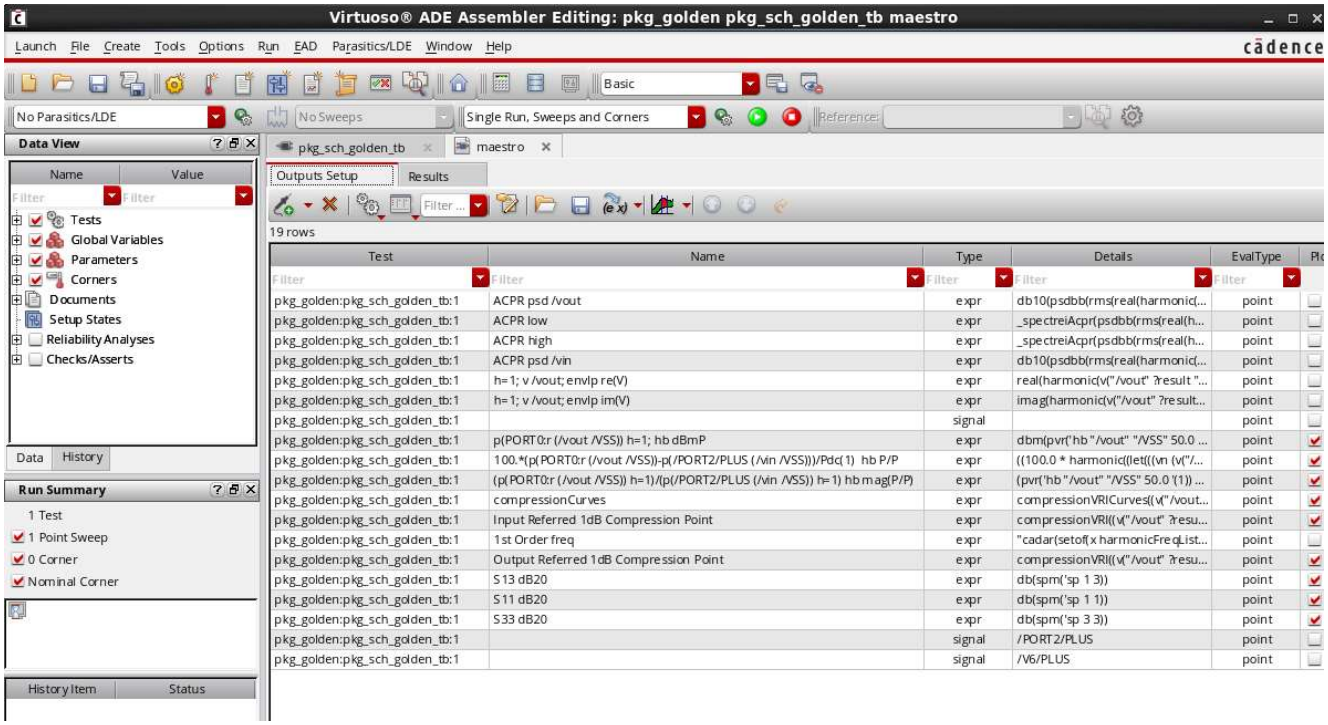
Virtuoso ADE Explorer/Assembler Simulations

- Rely on standard simulation tools to run system simulations
- No new netlisters or tools needed
- Standard measurements and signal post-processing work
  - Available MATLAB interface functionality for system-level measurements



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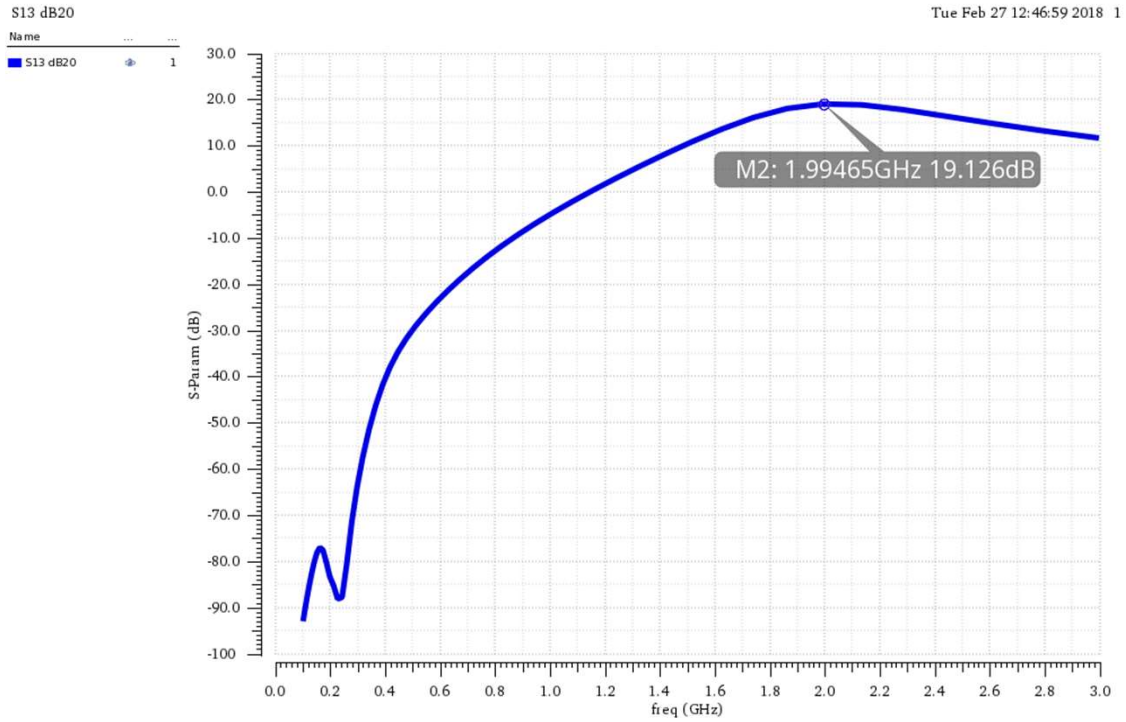
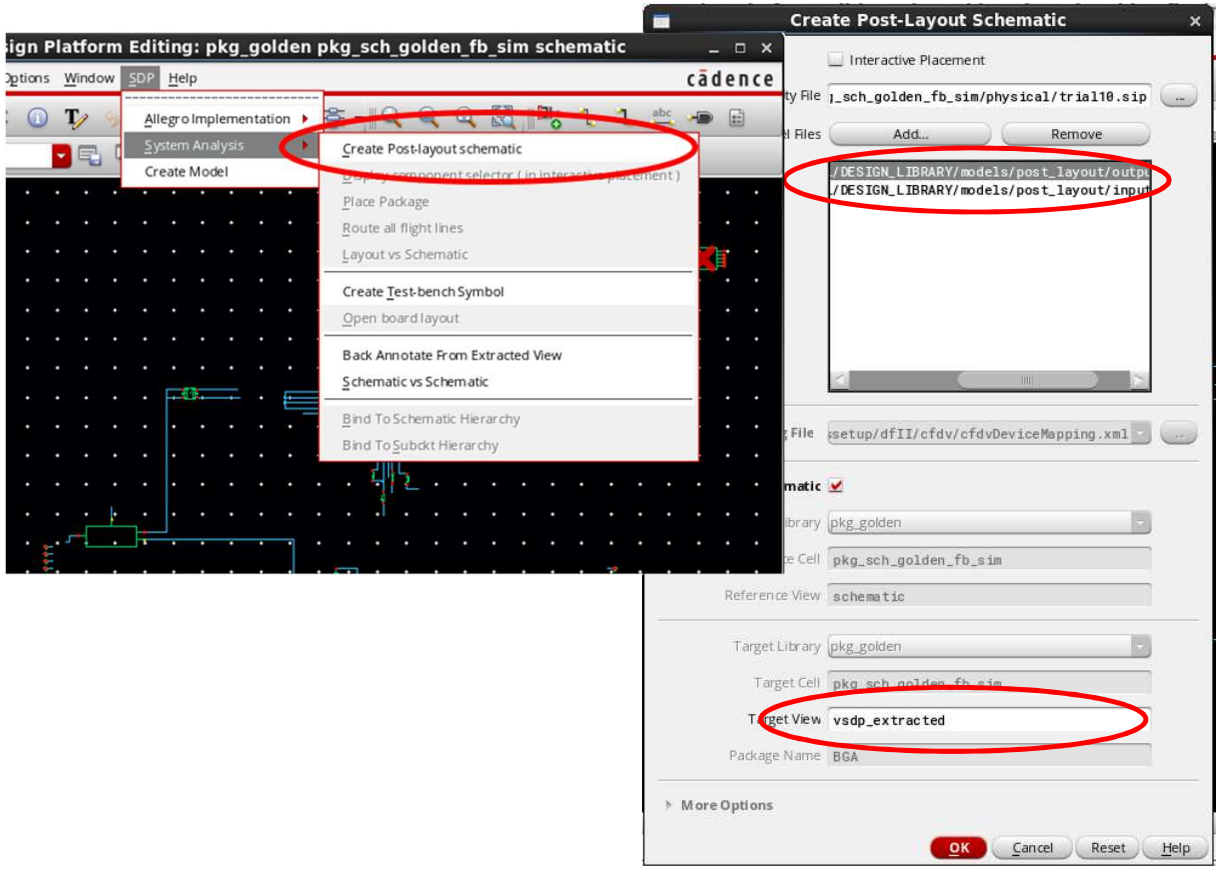
Pre-Layout Simulation Performance of the PA



Small signal gain ~= 19dB

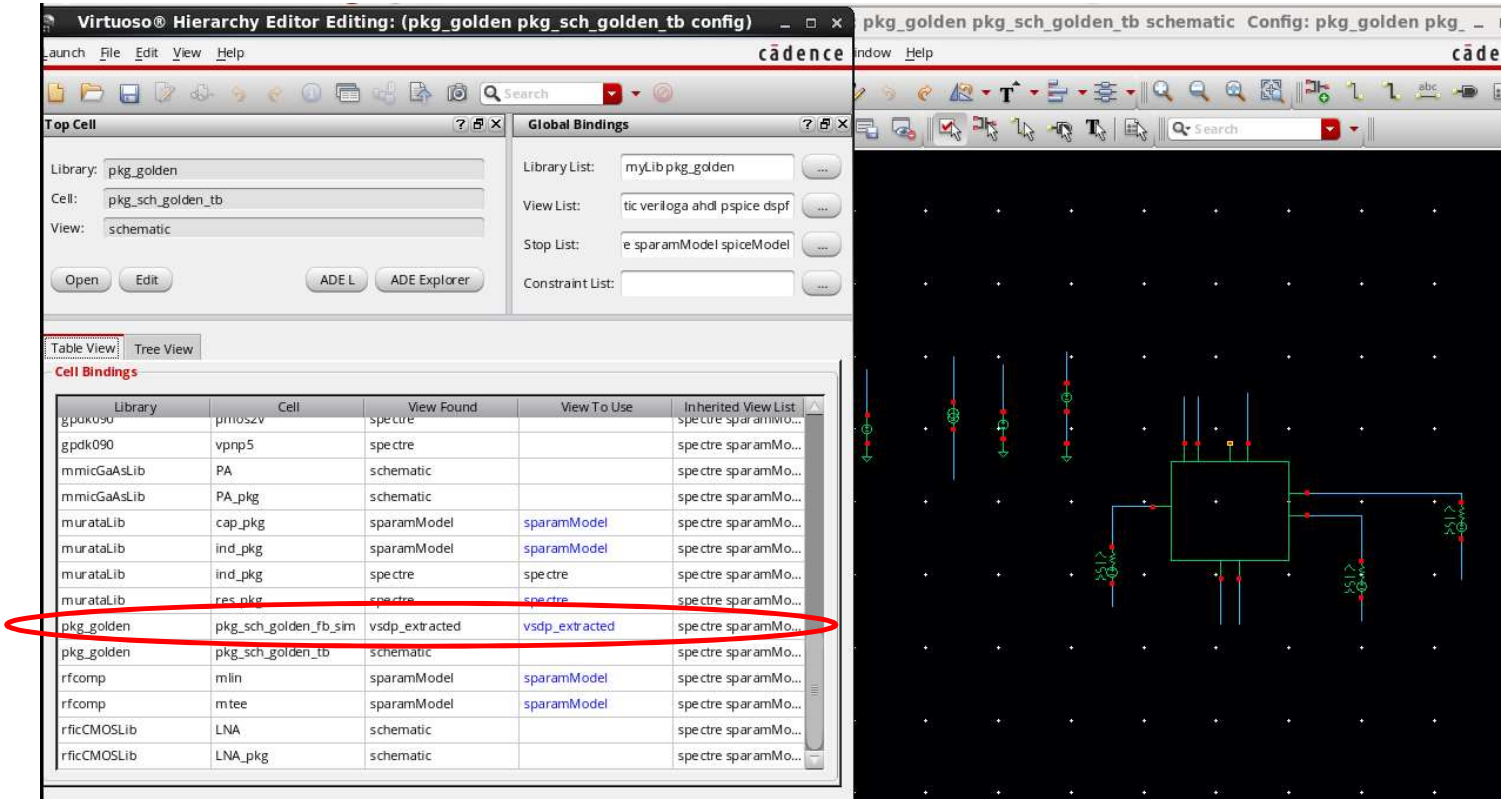
Virtuoso System Design Platform – Extracted View Creation Assistant

- Assistant used to guide creation of extracted view
- Parasitics extracted directly from package/module layout
  - Board-level extraction also supported
  - Direct 3D-EM modeling based on Sigrity technology
  - Third-party models supported
- Provide a list of s-parameter files and the SiP file
- Provide target lib/cell/view
- New schematic automatically generated with system-level layout parasitics



Enabling the Extracted View in the Testbench Configuration

- Extracted view simulation uses same config view
- Hierarchy Editor used to select new extracted view
- No change to testbench needed
- Flow familiar to users of Quantus™ extracted views



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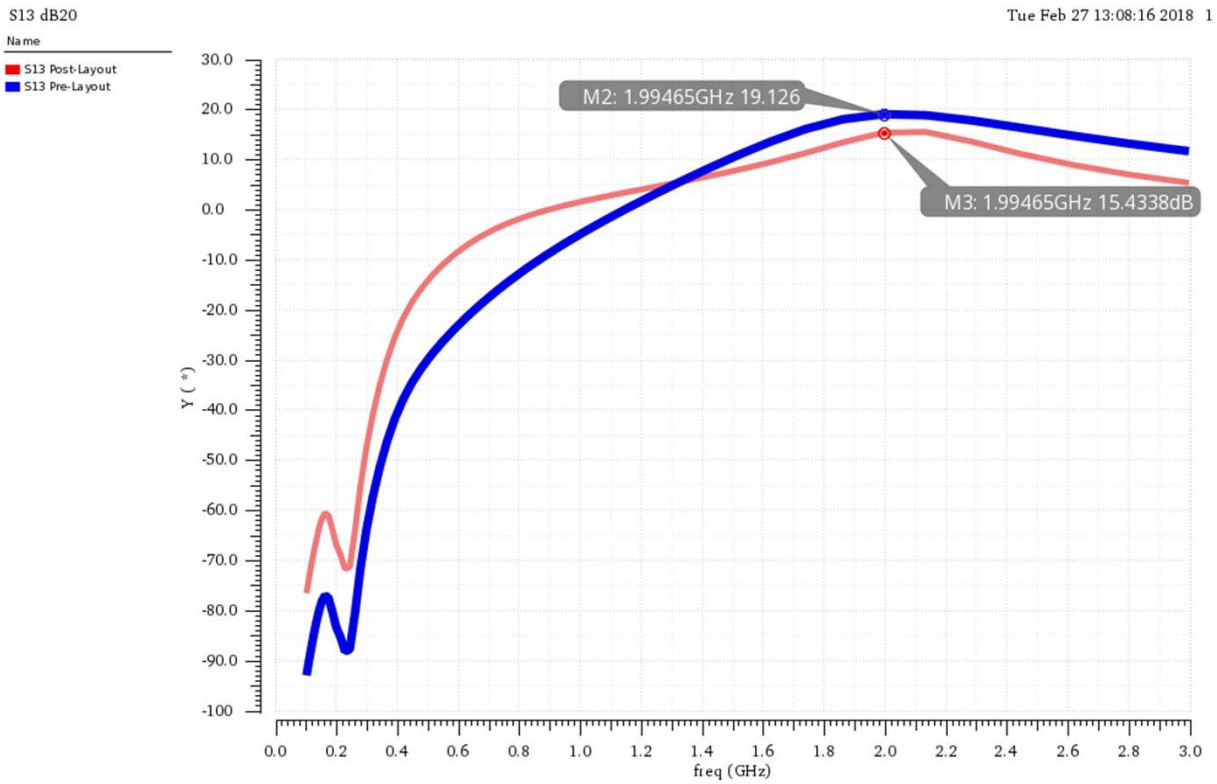
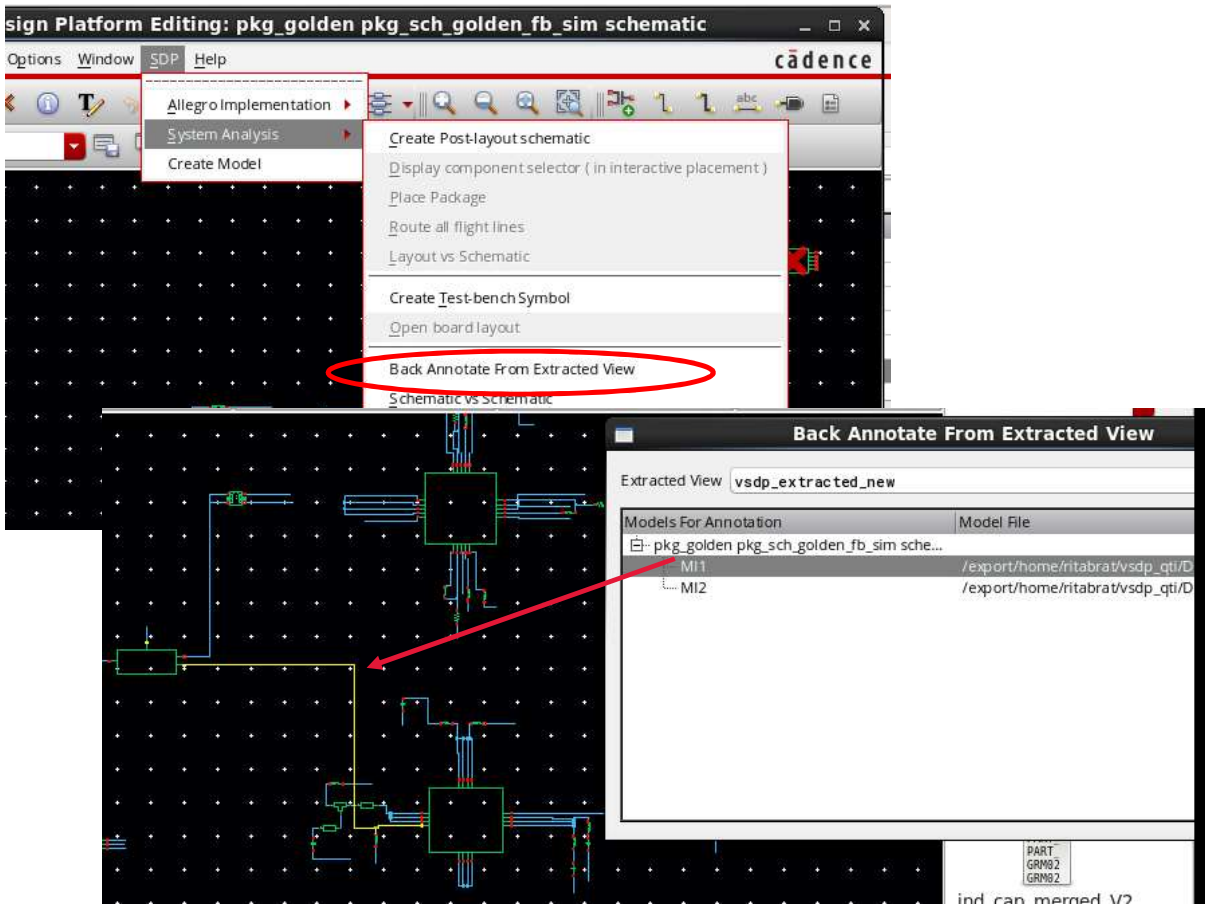
Virtuoso ADE Simulation with Package Layout Parasitics



~3.5dB loss due to package-level layout parasitics
Significant reduction in effective filter order

Visual Display of S-Parameter Models on the Golden Schematic

- Functionality aids in debugging simulation data
- Provides visual identifiers on schematic of which nets in extracted view have parasitics
- Provides listing of all s-parameter files used in the extracted view



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