Synchronizing high-speed data converters and digitizers, the benefit of daisy chaining

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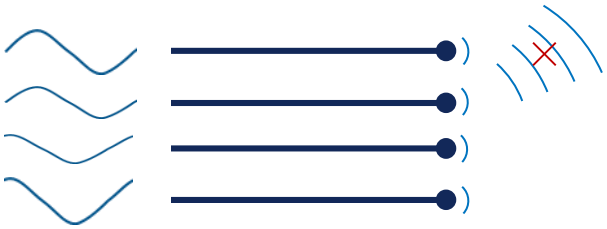
Summary

1. Application
2. Synchronization Definition, Challenges & Current Solution
3. Daisy Chaining Synchronization Solution
    1. Data Converters
    2. Digitizers
4. Benefit & Limitations

Beamforming

Single Elements Transmit/Receive

+ One element illumates a large swath
+ Increased interference between units (noise)



Multiple Elements Transmit/Receive

+ Same signal with dynamically controlled phase/gain generated by each element
+ Interference between elements outputs/inputs enables beamforming
+ Facilitate interference cancellation between units (noise)
+ Synchronization between elements mandatory

Application

Telecom systems

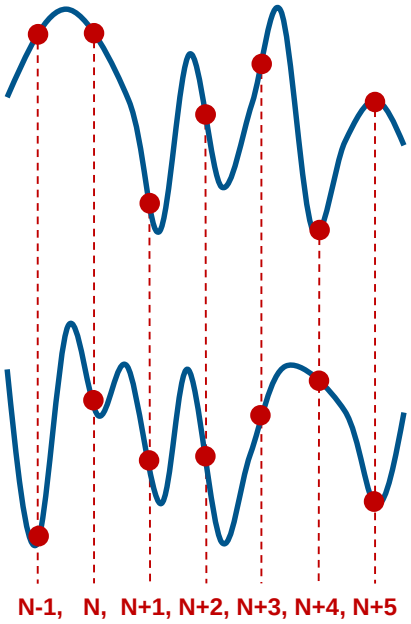
+ 4G, LTE, 5G Network
+ Massive MIMO
+ Satellite based Telecom (constellation and their ground station
+ Telecom Test Equipment

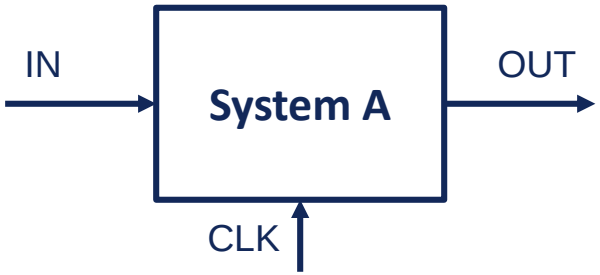
Radar systems

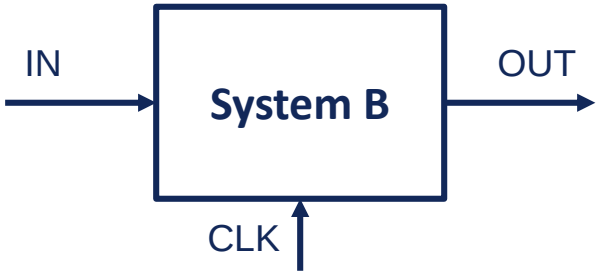
Wideband Radar +

Synchronization Definition

- The clock signal is the time reference and time aligned at the input of all systems
- Two systems are synchronous when they sample data on the same clock edge and the data are aligned at the output of all systems





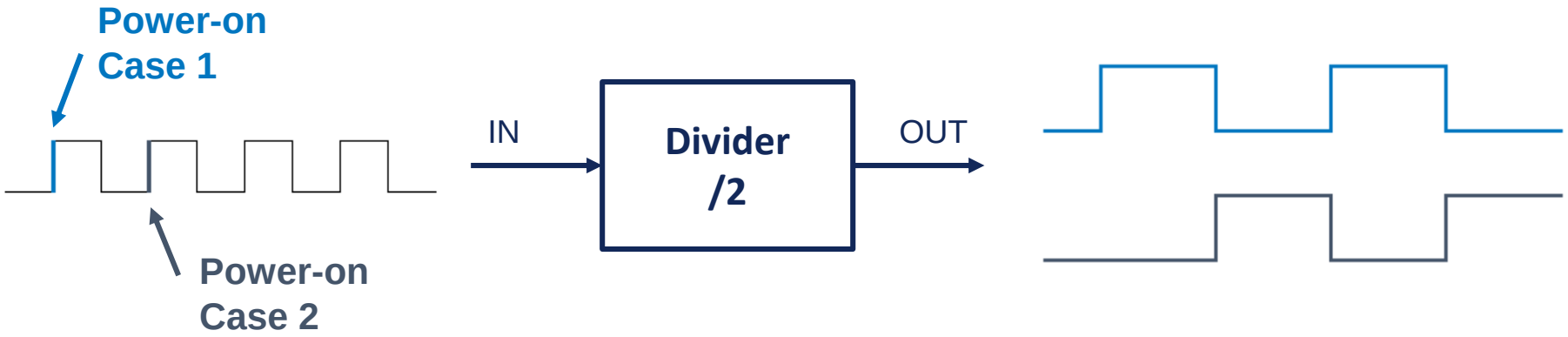


Not Synchronized

Synchronized

Synchronization is not automatic

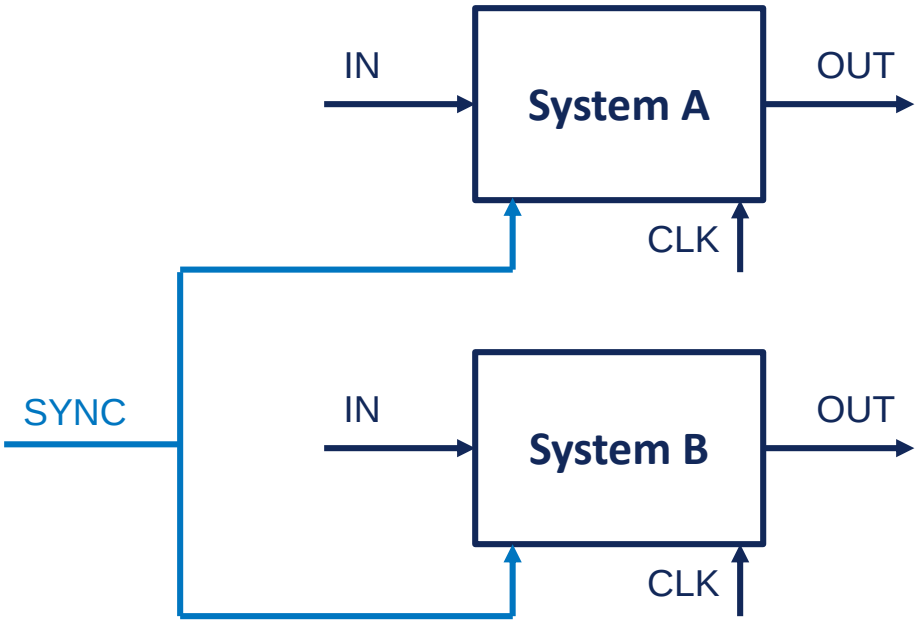
- Data converters and digitizers are complex system involving advanced time and clocking circuits implementing dividers, DLLS, PLLs, …
- At power-on these time and clocking circuits start in an undeterministic state, a start is needed to bring them into a deterministic state



- Two possible cases depending on the power-on leading to an undeterministic start. When looking at the output of two dividers in two identical system, there are no guarantee that they will start similarly

Traditional Solution 1

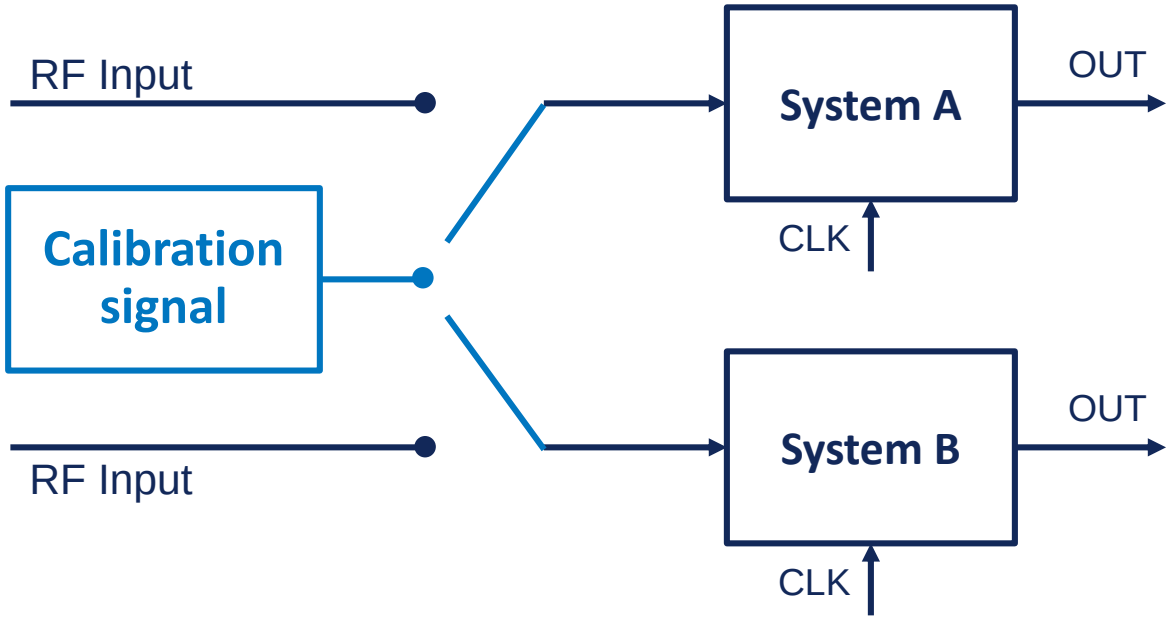
- A synchronization (or start) signal, generally a pulse or a low frequency clock, is propagated to the different systems that needs to be synchronized
- Timing on this signal are very constrained as they need to arrive at the same time (within one clock cycle) on all systems to synchronize



- Complex timing constraints
- All calibration process to redo at every power-up or loss of synchronization
- Difficult to implement on large scale or through backplane

Traditional Solution 2

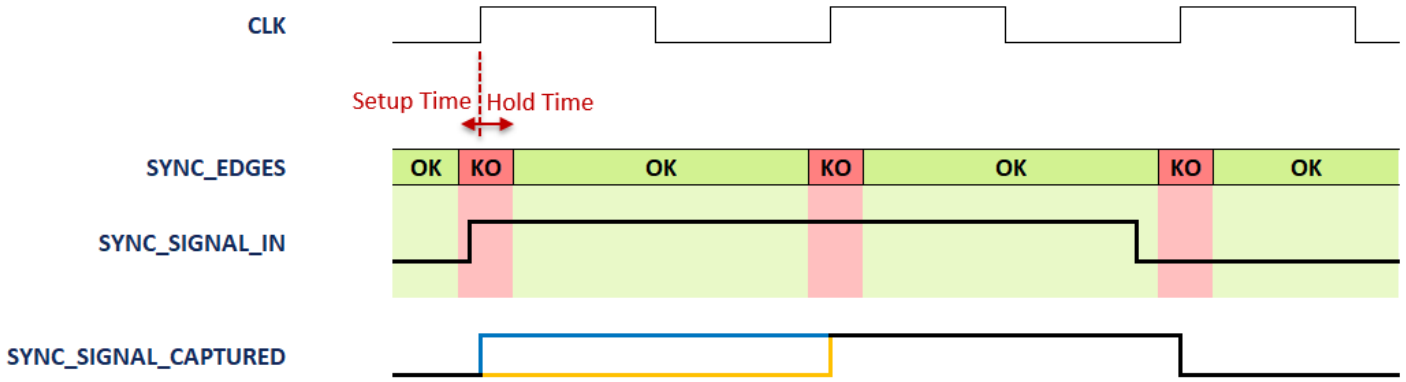
- Specific calibration data are propagated through all the systems with similar timings
- By comparing the timing of these known data, the systems can be calibrated to achieve synchronize



- High SWAP-C impact
- Complex timing constraints
- Switch degrade RF performance
- All calibration process to redo at every power-up or loss of synchronization
- Difficult to implement on large scale or on backplane implementation

Meta-stability challenge

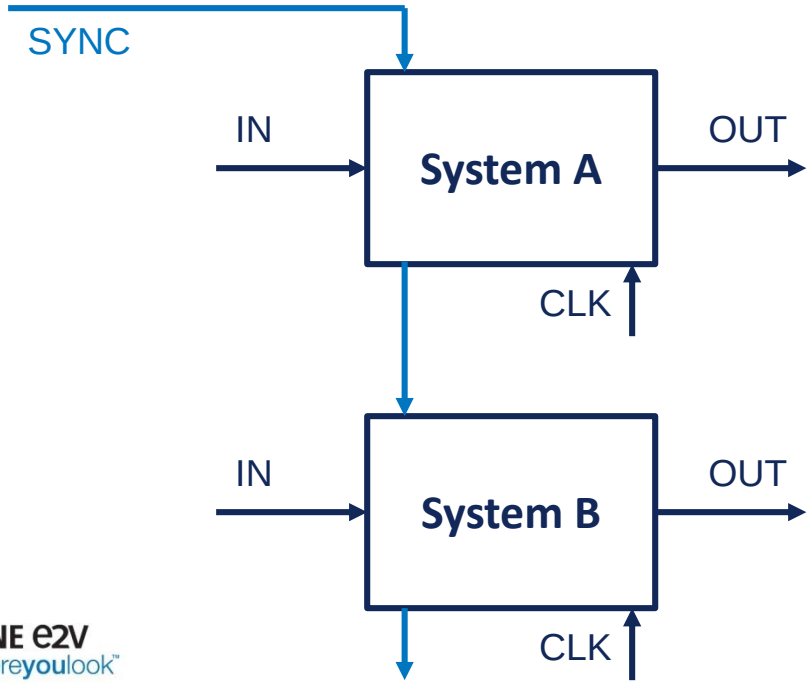
- Meta-stability occurs when a digital signal changes state close to the clock edge that captures it
- When meta-stability occurs, the output can update to the new state randomly at the right clock cycle or the following one leading to undeterministic timing



- At low speed, the clock period is large with regards to the meta-stability zone. However when the clock frequency increases, meta-stability zone is a non-negligible time and needs to be cared for

Chaining Synchronization

- A synchronization signal is propagated from system to system through a daisy chain implementation
- Meta-stability detection and/or avoidance solution are implemented in the data converter and digitizer



- No or few timing constraints on the synchronization signal
- Synchronization training to be done once per layout (no production calibration needed)
- Support large scale and backplane implementation

Chaining Synchronization

- Example with Teledyne e2v latest high-speed ADC, the EV12AQ600
- ADC 12-bits, 6.4GSps single, 3.2GSps dual, 1.6GSps quad-channel

Characteristics

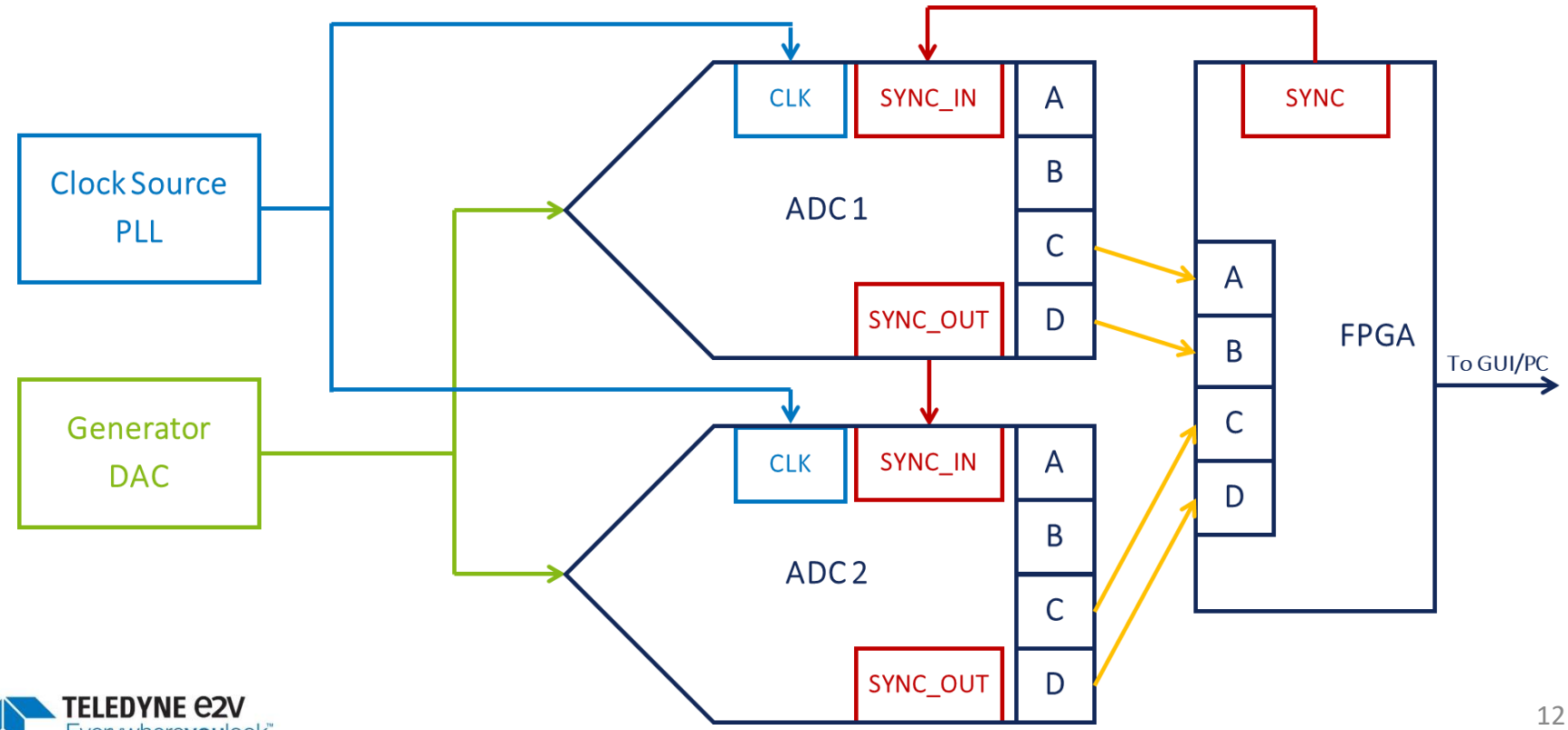
- **Capability for single, dual, quad-channel operation:**
  Dynamically configurable in 1, 2 or 4 channel
  Unique analog input cross-point switch
- **Bandwidth:** Analog input bandwidth above 6.5GHz
- **Step response:** 115ps
- **Consumption:** 1.6W/channel (6.4W total)
- **Input:** 1 Vpp differential into 100Ω
- **Output:** 8 ESIstream serial interface at 12.8Gbps
- **Package:** CBGA323 (16x16mm, Pitch 0.8mm)

Applications

- Ultra Wideband Satellite Digital Receiver
- Broadband Telecommunication System
- High Speed Data Acquisition
- Automatic Test Equipment
- High Speed Test Instrumentation
- Wideband SAR system
- Radar system (weather, traffic surveillance, …)

Chaining Synchronization

- Example with Teledyne e2v latest high-speed ADC, the EV12AQ600
- 8 channels at 1.6Gsps synchronized



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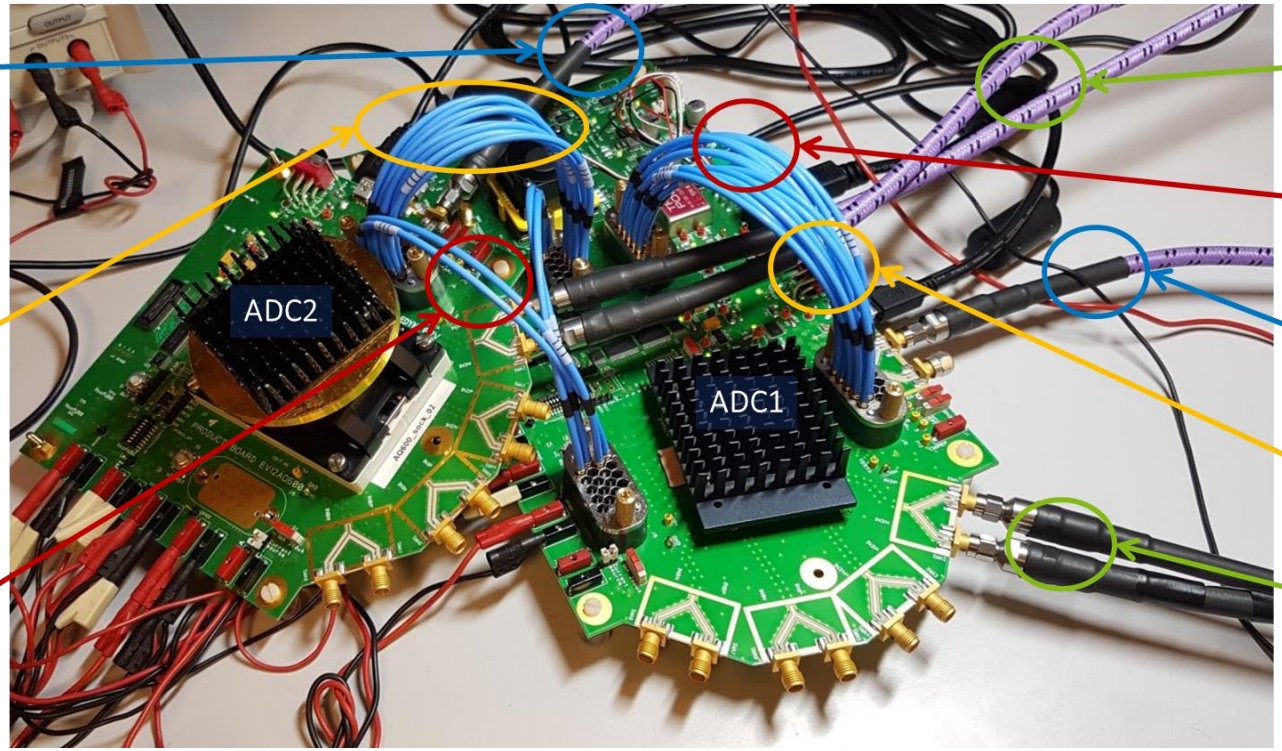
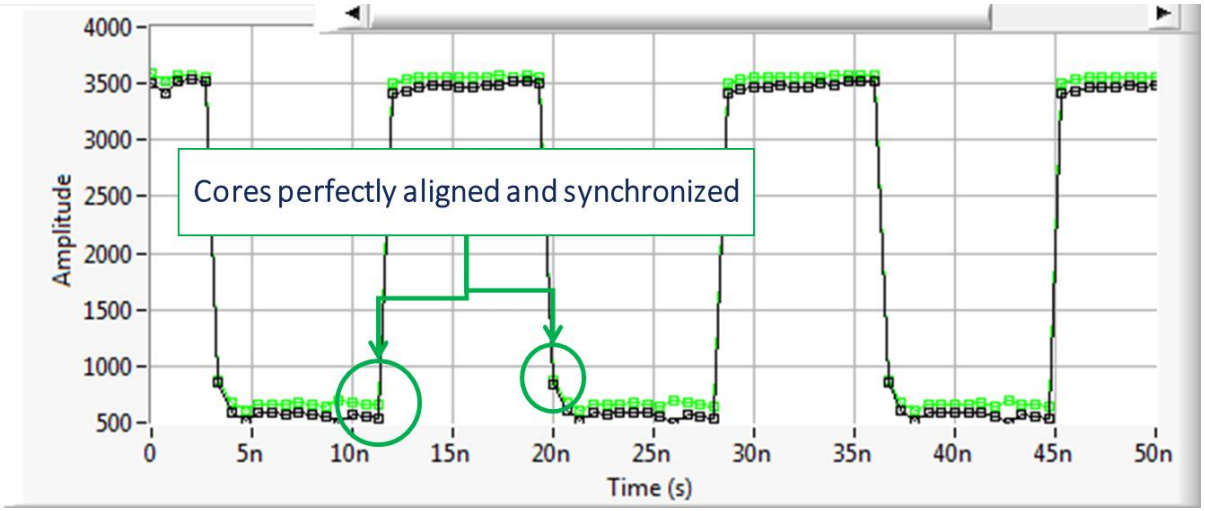


Chaining Synchronization

- Example with Teledyne e2v latest high-speed ADC, the EV12AQ600
- 8 channels at 1.6Gsps synchronized



Data from GUI:

- Green signal: data from ADC1 core C
- Black signal: data from ADC2 core C
- Analog input square wave

- After the training, the two ADC are synchronized and it is repeatable over power cycle and synchronization cycle
- Stability of the synchronization validated up to +125°C

Chaining Synchronization

- Example with Teledyne SP devices latest digitizer, the ADQ8
- Digitizer 10-bits, 1GSps, 8-channel

Characteristics

- **10-bit vertical resolution**
- **8 channels with 1 GSPS / channel**
- **DC - 250 MHz**
- **DRAM: 1 Gbyte**
- **PXIe Gen 2x8; 2 slots**
- **Open FPGA architecture**
- **Superior timing engine**
  - 52ns re-arm time
  - 25ps Trigger time-resolution

Applications

- Ultrasound applications
- Non-destructive testing
- Wireless communication
- Time-of-flight
- Particle physics
- Semiconductor test
- ATE
- Quantum technology

Chaining Synchronization

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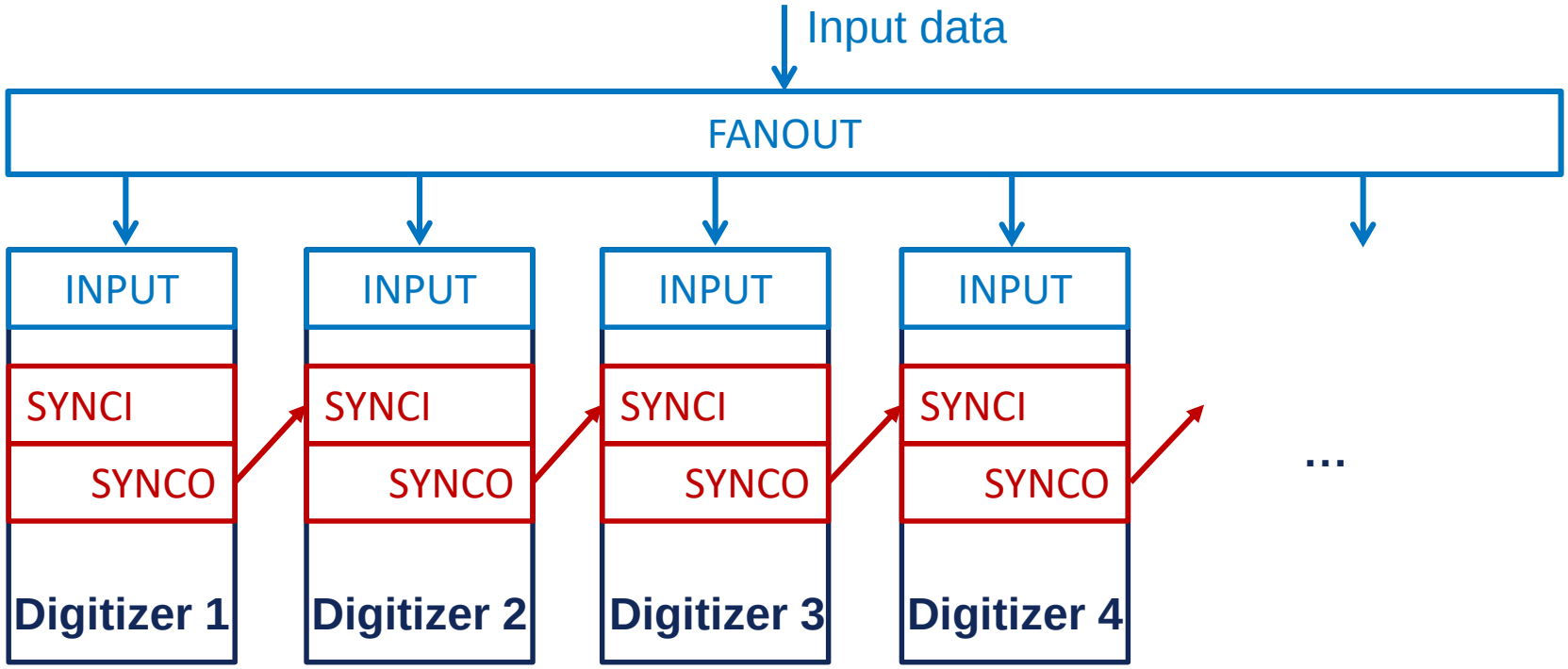
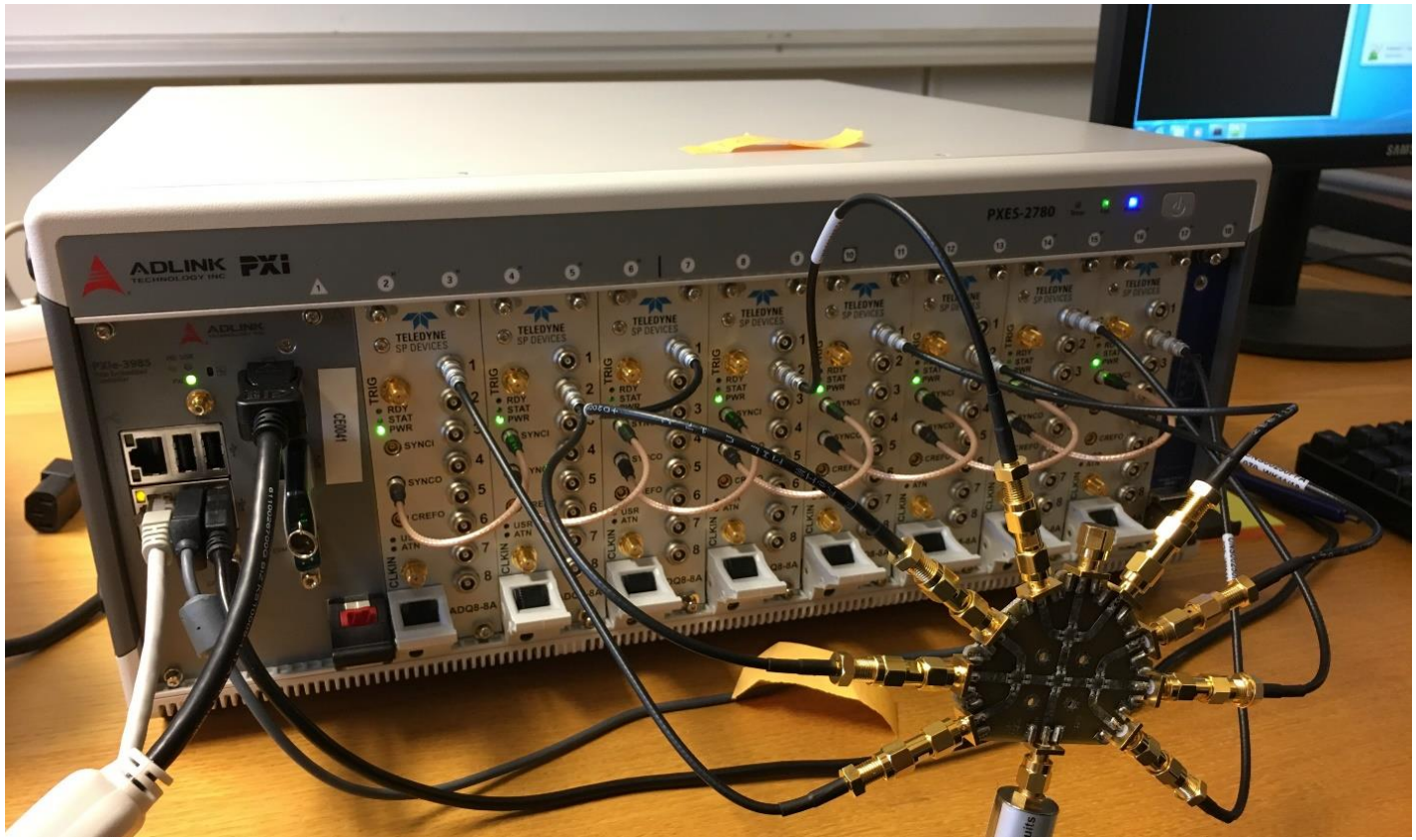


Chaining Synchronization

- Example with Teledyne SP devices latest digitizer, the ADQ8
- 64 channels at 1Gsps synchronized



Benefit & Limitation

- One training per design thanks to meta-stability detection and/or avoidance solution
- Support large scale system including backplane connection
- SWAP-C savings and less complexity compared to traditional solutions
- Constrained timings on the clock signals. As the clock is the time reference of the system, this is always the case for deterministic application. Specific solutions exist to align clocks
- Constrained timings on the input signals. Specific solutions exist to align the input signal

Thank you

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