100nm and 60nm GaN/Si MMICs: The optimum complement to Si MMICs for mmW and TeraHertz applications

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Outline

- Opening comments
- mmW and TeraHertz applications
- Competing Si & III/V RFIC technologies
- Why GaN/Si
- 100nm and 60nm GaN/Si processes
- GaN/Si and CMOS Hetero-integration
- Conclusion

Opening comments

- The Si RF community has been dreaming of replacing III/V solutions for the last 30 years but the telecommunication system roadmap is ruling the roost

- The III/V community has overlooked the importance of roadmapping for the last 30 years

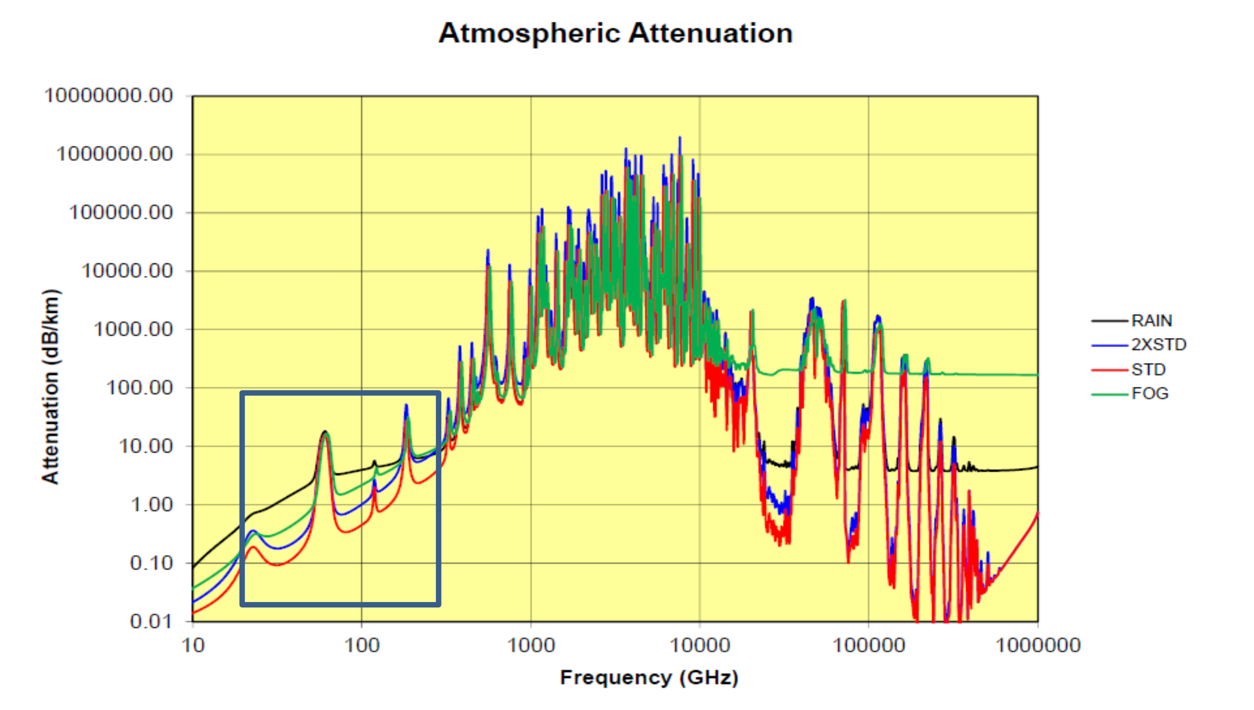
- 100 nm& 60nm GaN/Si is low cost without limits on wafer size and is a full replacement of GaAs solutions and ready for heterogeneous integration

Opening comments

- OMMIC founded in 2000, by Philips Semiconductors

- Over 40 years of experience in III-V semiconductors
- Unique GaN Process best suited for upcoming 5G
- Only foundry in Europe offering complete service:
    - Epitaxial Growth
    - Process Development
    - MMIC design, fabrication, test and qualification

Frequency Spectrum for mmW and Terahertz applications



3.5 to 90 GHz telecommunication bands

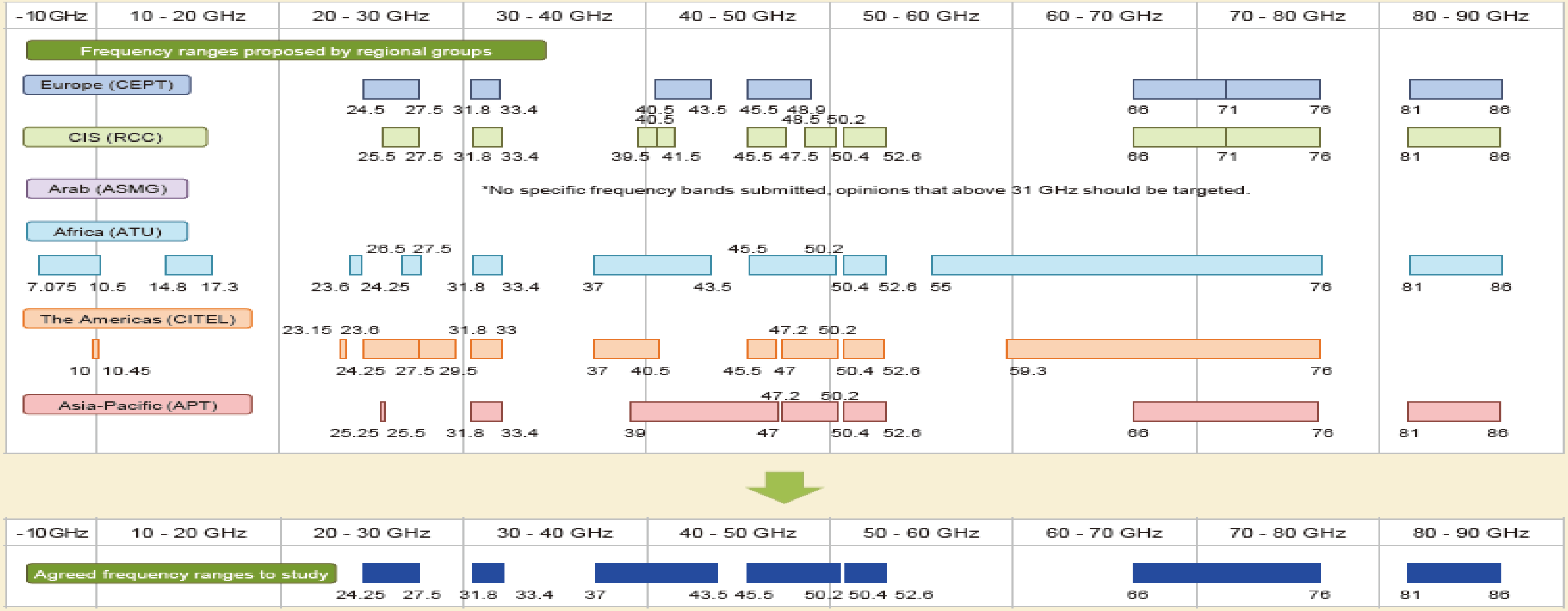
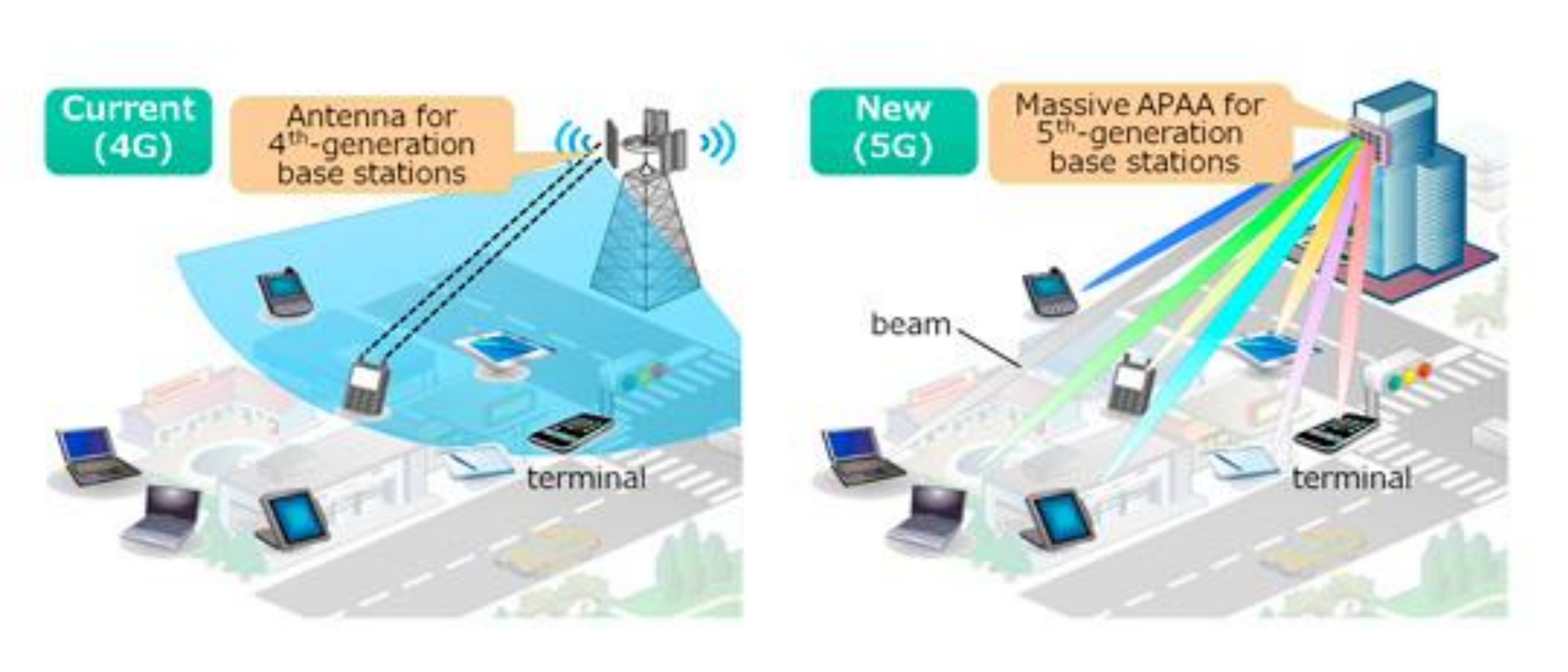


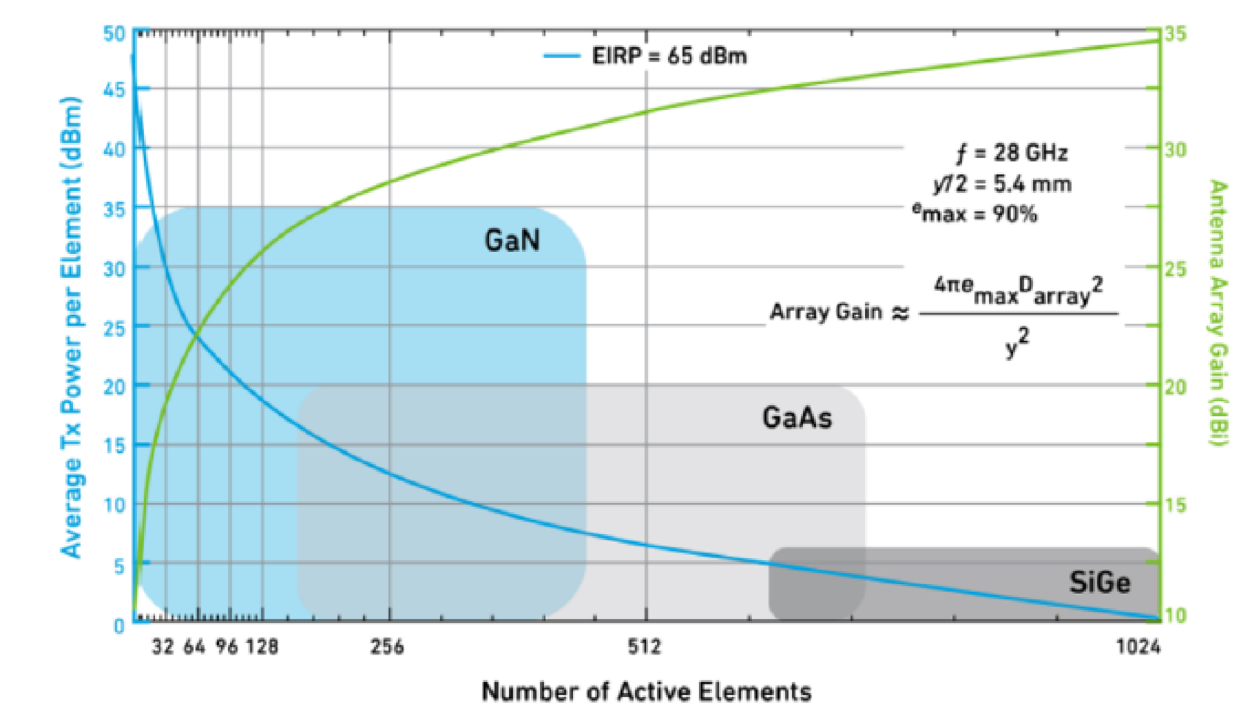
Figure 2 Frequency ranges to study for IMT identification in WRC-19

mmW and TeraHertz applications

Massive MIMO 5 G base station



65 dBm EIRP, GaN /Si(C) is the winner



Competing RF IC processes

SI CMOS FD SOI
SiCMOS FinFET

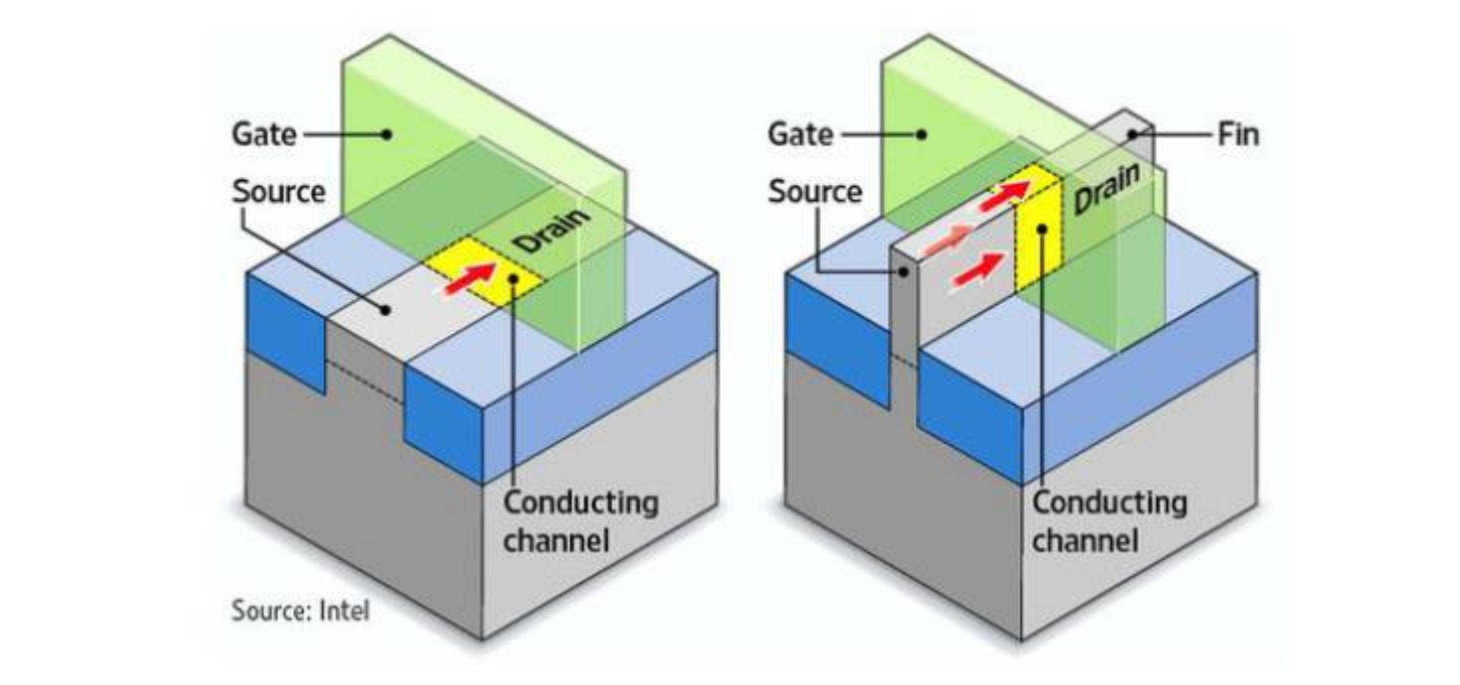
BiCMOS (SIGe HBT+ CMOS)

GaAs PHEMT
GaAs MHEMT or InP PHEMT

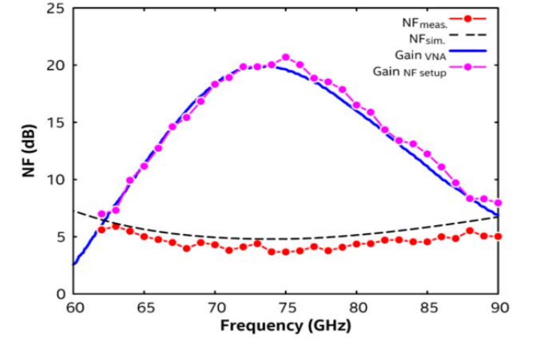
GaN /SIC or GaN/Si HEMT

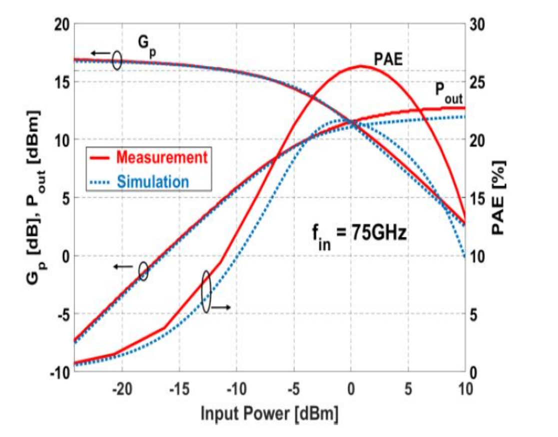
InP HBT

Planar FD SOI CMOS versus FinFET



14nm FinFET : 480GHz fmax





- RF FinFET by Intel: Trigate introduced in 2011,
- 22nm FFL: 14nm FinFET with 22nm relaxed metal back end
- FD SOI is short channel effect limited while FinFET is less
- Ft : 280GHz, fmax: 480GHz,gm/I=30
- NF min at 70GHz: 2dB
- Selfheating of gate is the issue: limits the Imax
- 75GHz LNA: 2 stage, stacked, 20dB, 3.7dB NF, 71-78GHz
- 75GHz PA: 18dB gain, 26%PAE, 12.8dBm

45 nm FDSOI : 250GHz fmax

Frequency (GHz)	Pout (dbm)	PAE(%)	comments
24	26	34	16dB gain
28	23	42	-30dBc ACPR
33-44	18	43	Class F
75	12		

Frequency (GHz)	NF(dB)	
30	1.3	13dB gain
90	4.5	12dB gain

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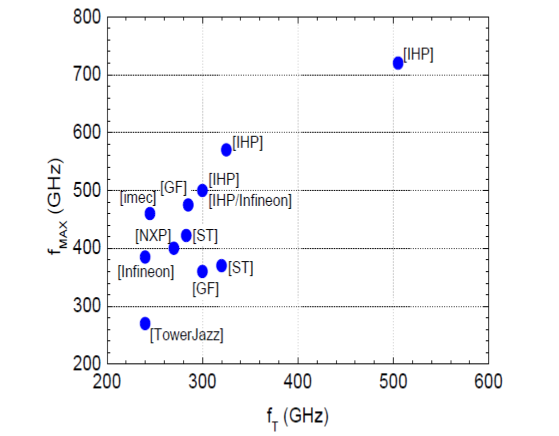
SiGe BiCMOS



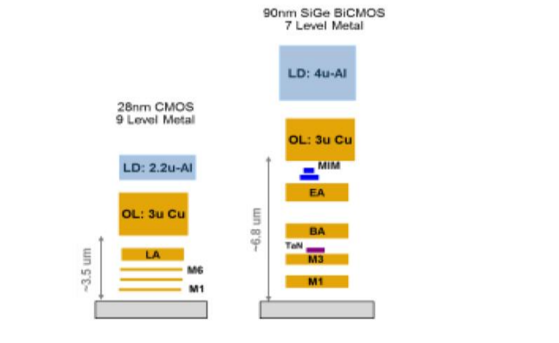


Figure 6: Metal stack comparison of that observed in 28nm CMOS and a 90nm SiGe BiCMOS. Thin metal and ILD's in advanced CMOS brings the top-level thick metal for RF wiring closer to substrate and causes more loss.

BiCMOS trying to resist advanced CMOS

- Why BiCMOs still exist ?? (50 masklevels, trade off Bipolar, CMOS , not the best of CMOS due to thermal budget) 130nm Bipolar and 55nm CMOS node , trying to scale to 28nm???

- SiGe HBT PA for 5G:28GHz, 18dB gain, 20dBm, 40%
  SiGe HBT PA28-42GHz : 17dBm, 27%PAE, 130nm BiCMOS

SiGe BiCMOS vs FDSOI

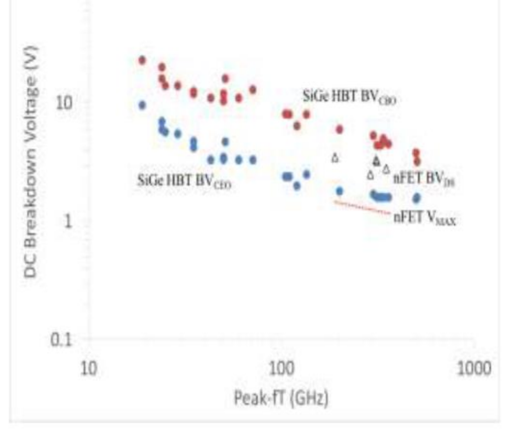
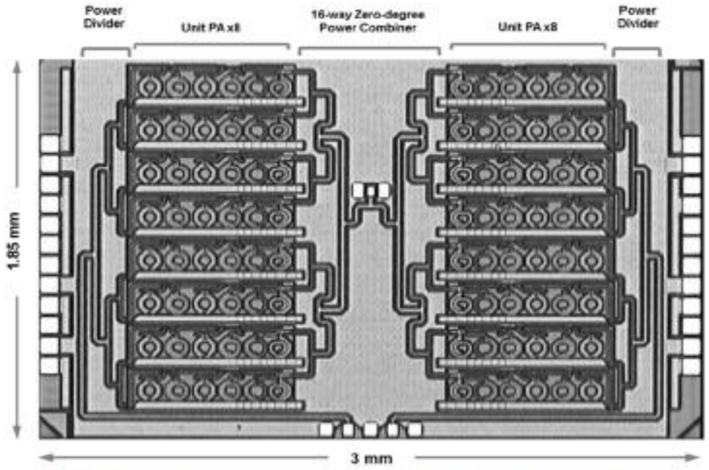


Figure 9: SiGe HBT BV_{CEO} and BV_{CBO} breakdown voltages compared against BV_{dss} and V_{max} of scaled nFET technologies competing in mmWave.

- Global Foundries : SiGe BiCMOS vs FD SOI
- SIGe BICMOS for RF : 130nm /90nm(1.8/1.6V)
  - Fmax:265/370GHz, NF min (30GHz) : 1.6/1.1dB
- FD SOI : 45 nm better than 28nm(1V).
  - Fmax: 265GHz, NF min: 0.8dB at 6GHz
- But WHAT CAN BE DONE in CMOS will be done in CMOS

Best Ka band Si Power amplifiers



Die micrograph of the CMOS 16-way power-combined PA designed and tested at MIT/CMU (0.7 W at 44 GHz)

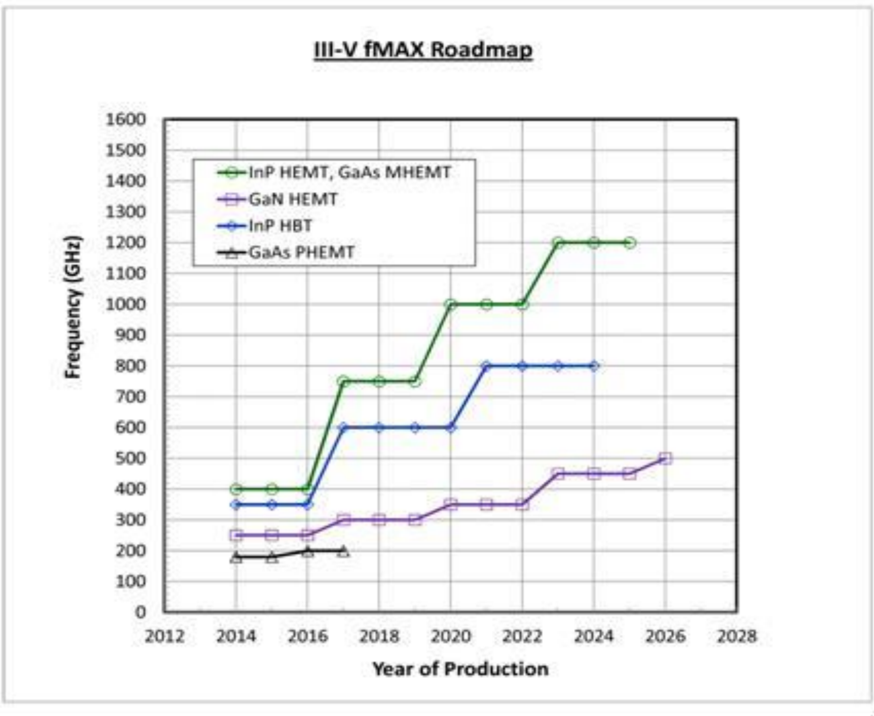
Conclusions on Si processes

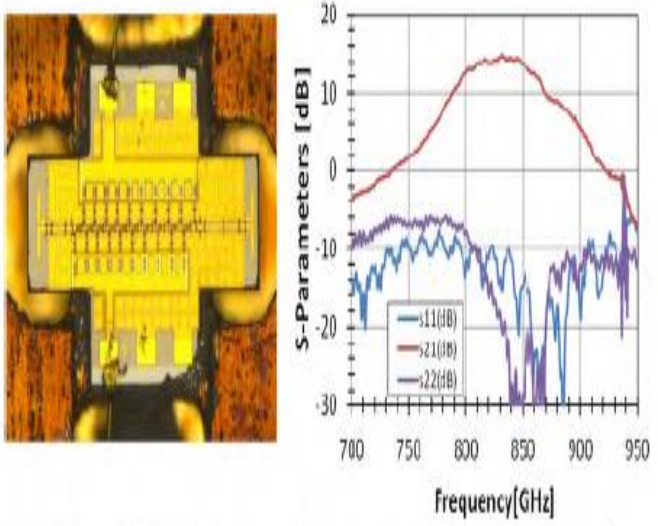
- Si RF processes : essentially targeting digital integration
  - BiCMOS (130/55 nm, 3V)
  - RF CMOS : 14nm FinFET, 45nm FDSOI, 1,5V

    +++ integration

    ---- Limited by breakdown voltage and parasitics related to digital integration, 23dBm at Ka band
- III/V RF processes : specifically developed for RF applications

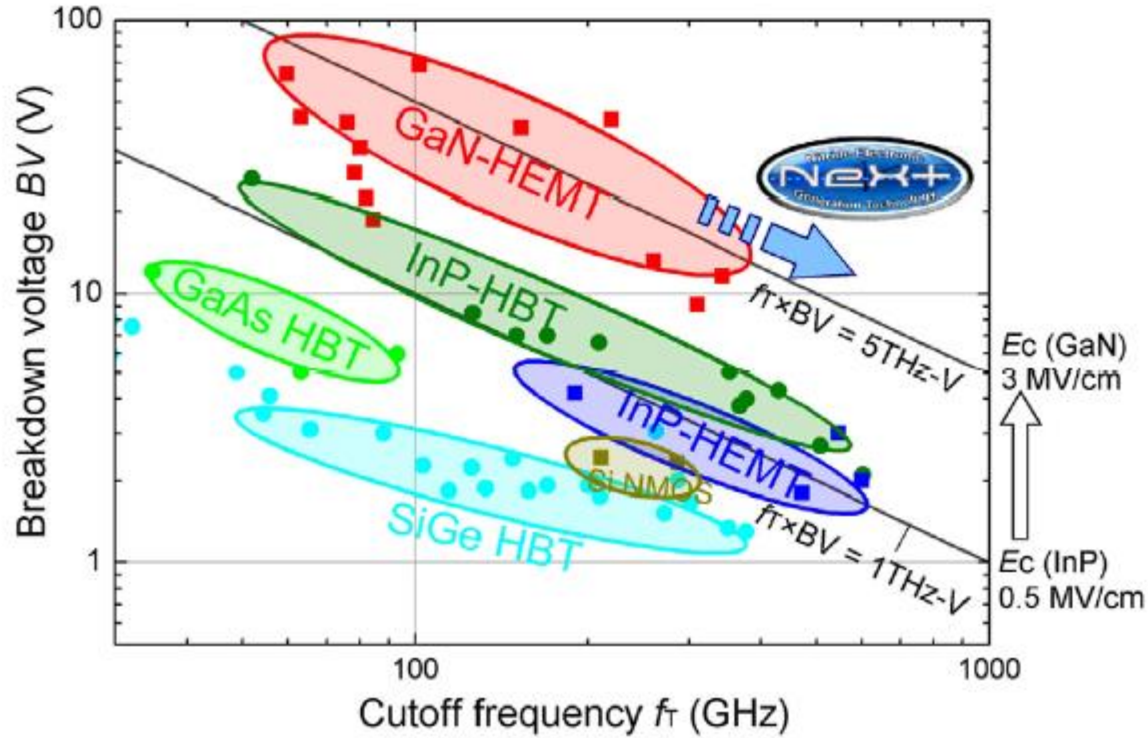
ITRS III/V production roadmaps



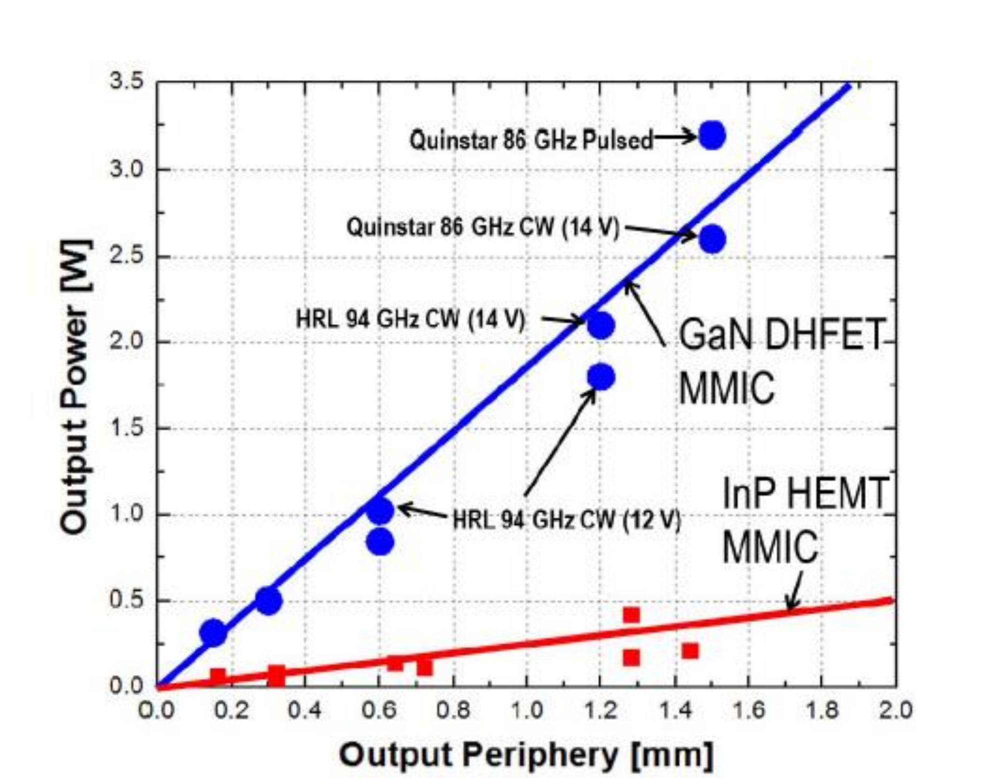


THz Monolithic ICs: Packaged 10-Stage LNA shows peak gain of 14.7 dB at 830 GHz. Source: Northrop Grumman

ITRS III/V production roadmaps



W band III/V PAs



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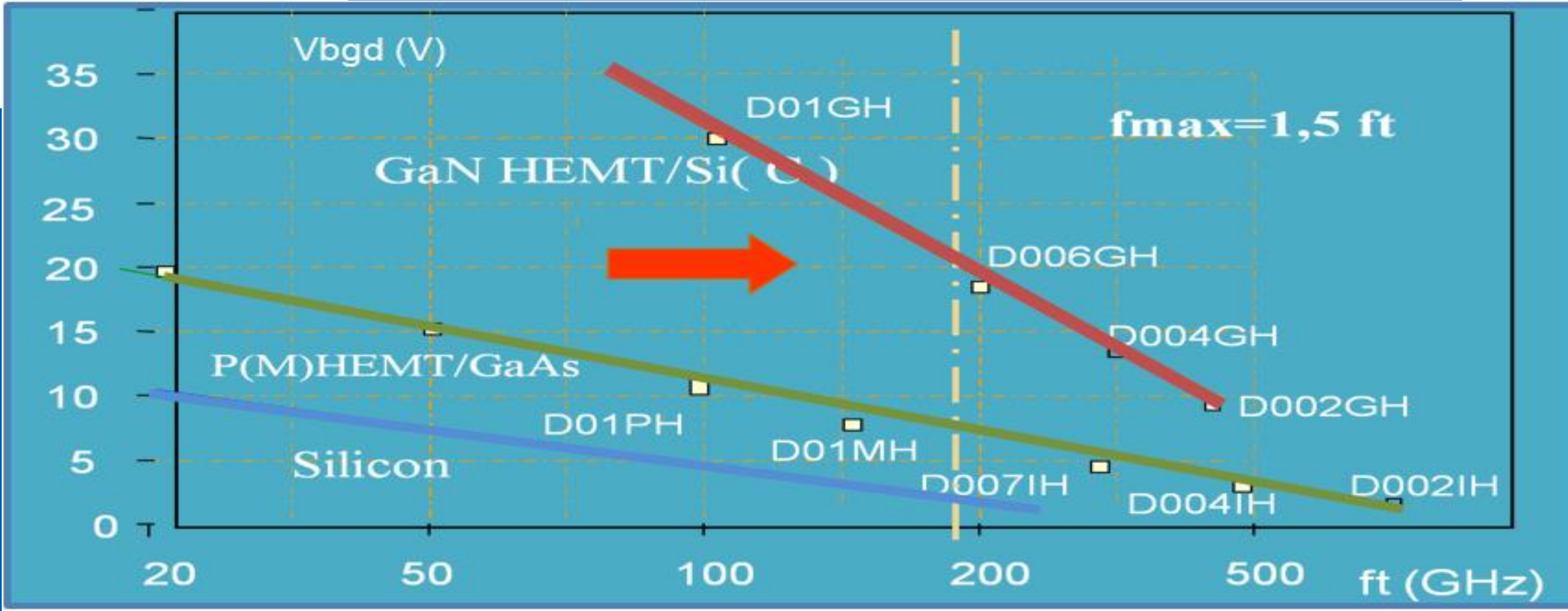
Ka band III/V LNAs

Technology	Frequency Range (GHz)		Noise Figure (dB)		Power Dissipation (mW)
	Min	Max	Min	Max	
GaN HEMT	30	39.3	1	1.6	82
GaN HEMT	30	37	1.9	2.2	5
GaAs pHEMT	26	36	1.5	1.8	NA
InP HEMT	26	40	1.3	1.8	16
InP HEMT	27	30	1.3	1.6	40
GaAs pHEMT	26	32	1	1.6	48
InP HEMT	43.3	45	1.6	2	30
InAs/AlSb HEMT	33	37	1.8	2.2	4.5
GaAs pHEMT	24	43.5	2	3	175

OMMIC III/V roadmap



WHY OMMIC GaN/SI

Replacement of existing microwave and millimetre wave circuits based on GaAs or InP PHEMTS

1) to improve the output power or robustness
2) with the same low noise performance
3) at the right cost
4) enabling heterogeneous integration

OMMIC 100nm & 60nm GaN/SI processes

Full MMIC Process for mm-wave designs
Via holes, air-bridges, metal resistors, MIM capacitors

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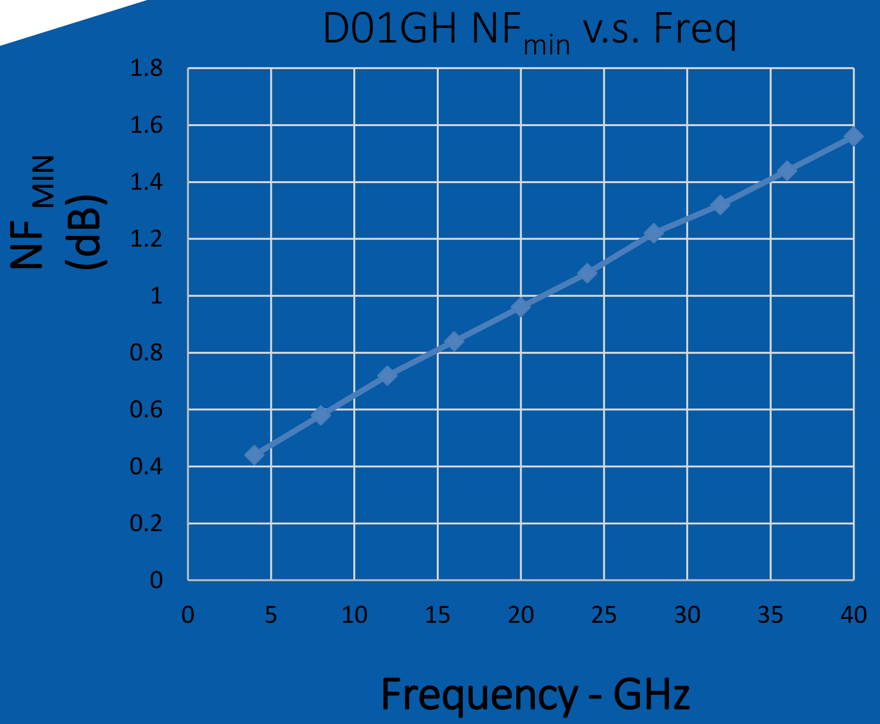
OMMIC 100nm GaN/SI process

Parameter	Value
FrequencyCut-off (H21)	105 GHz
Maximum Stable Gain @30 GHz	14.5 dB
Min Noise Figure /Ass. Gain @40 GHz	1.5 dB / 8 dB
RF Power Density (40GHz)	3.3 W/mm(50%PAE) 5.7 W/mm peak
Transconductance	700 mS/mm
Source Resistance	0.18 Ohms.mm
Low Field resistance(Ron)	0.8 Ohms.mm
Breakdown Voltage	40 V
Quiescent Voltage	12 V
Activation Energy(DC life test)	1.78 eV

D01GH GaN/Si low Noise PROCESS

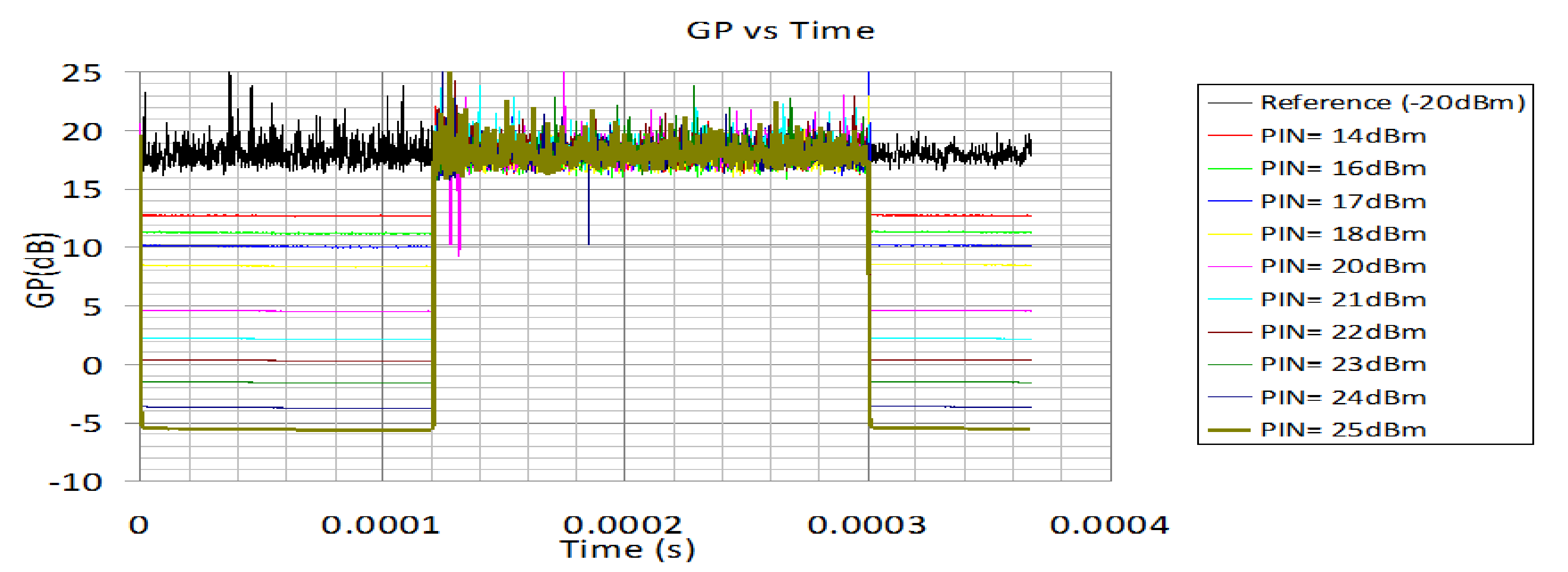


GaAs v.s GaN

5

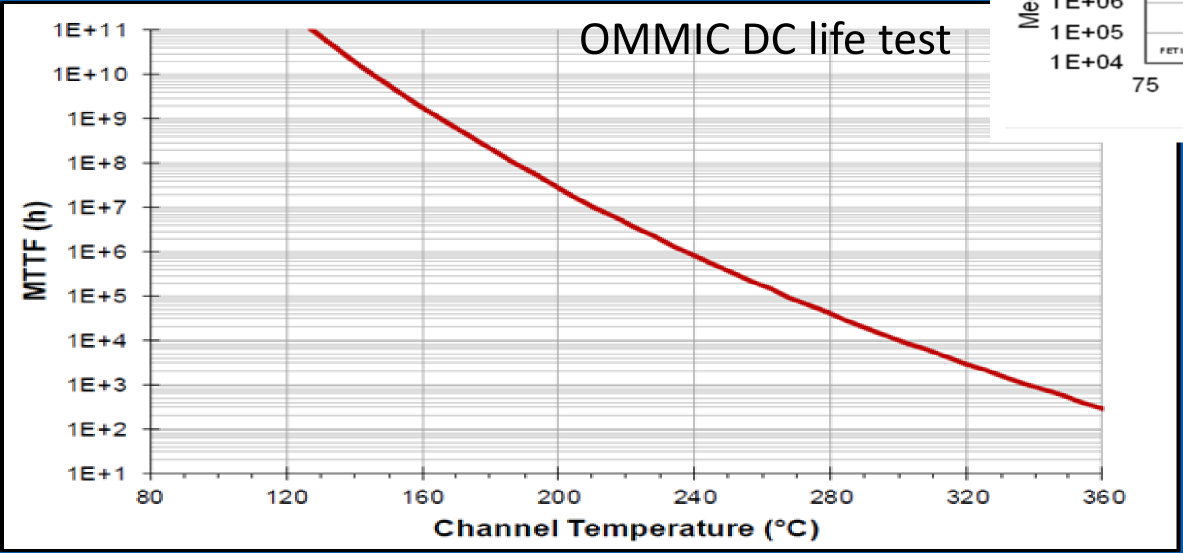
	D01PH GaAs pHEMT 135 nm	D01GH GaN/Si HEMT 100 nm	D01MH GaAs mHEMT 120 nm
V_{ds} (V)	3	5	1
I_{ds} (mA)	15	42	30
R_s (Ohm)	1,0	1,2	0,8
R_g (Ohm)	0,65	0,70	0,7
NF_{min}	1,72 dB	1,54 dB	1,13 dB
Associated Gain	4,5 dB	8 dB	12,4 dB

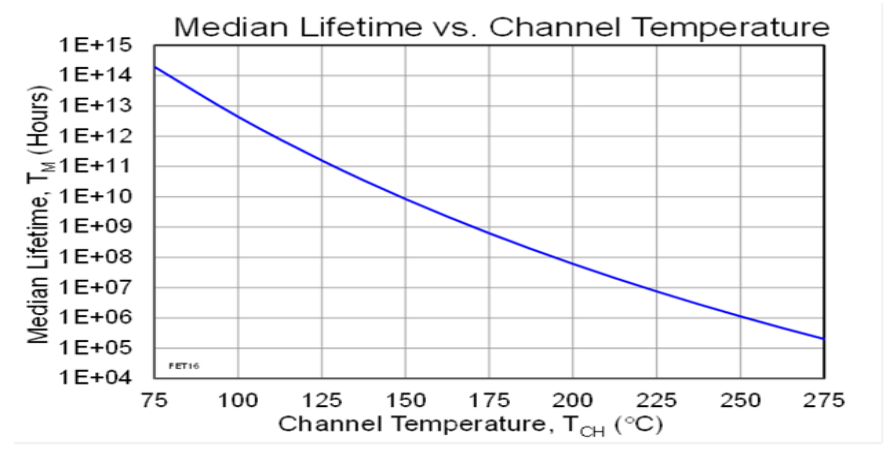
Recovery time after an input power pulse



No measurable Recovery Time after 24dBc agression (+25dBm input power on 2x35um device)

MTTF for 20% failure criterium
Ea= 1.8eV





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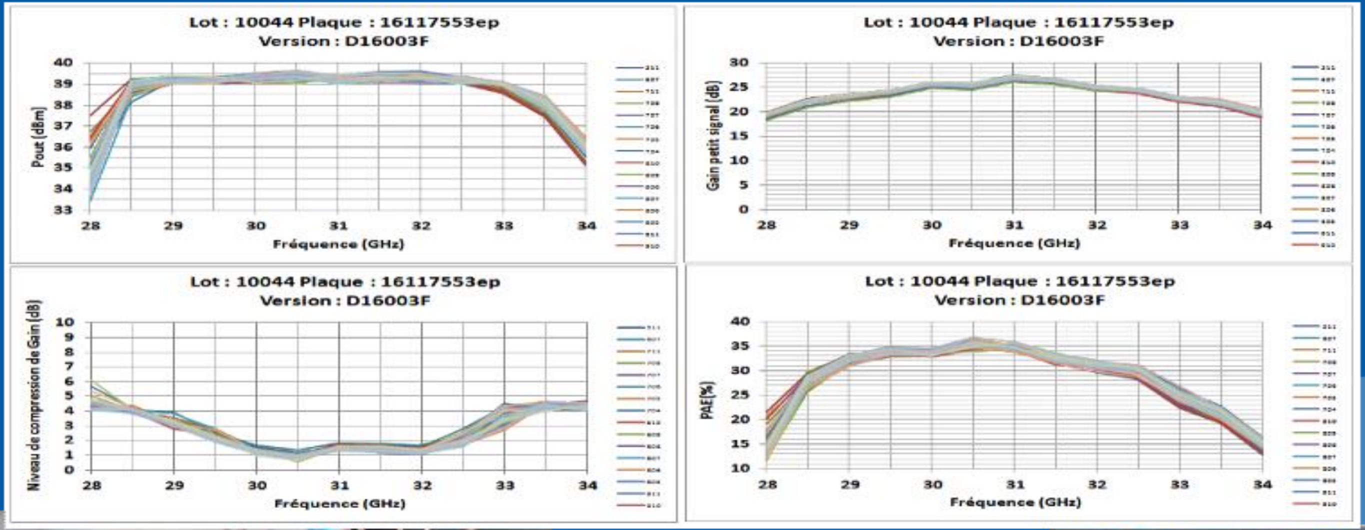
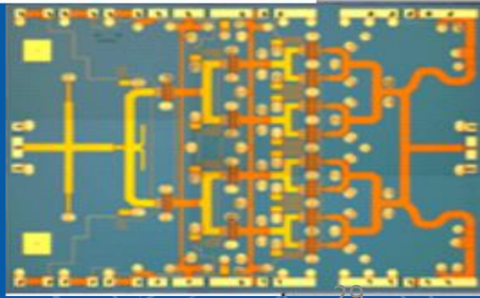
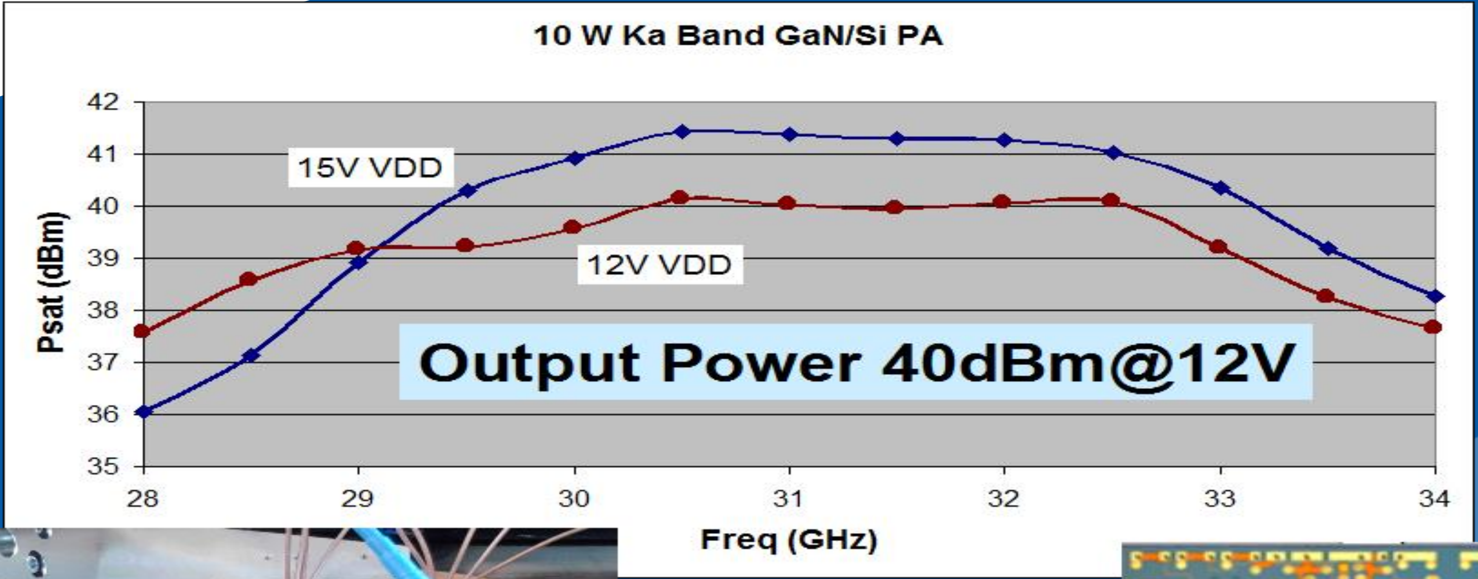
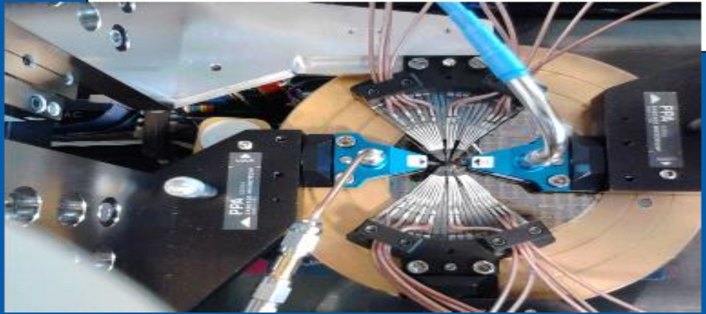
30 GHz 10 W Psat amplifier

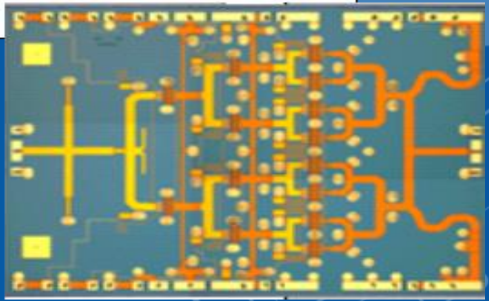




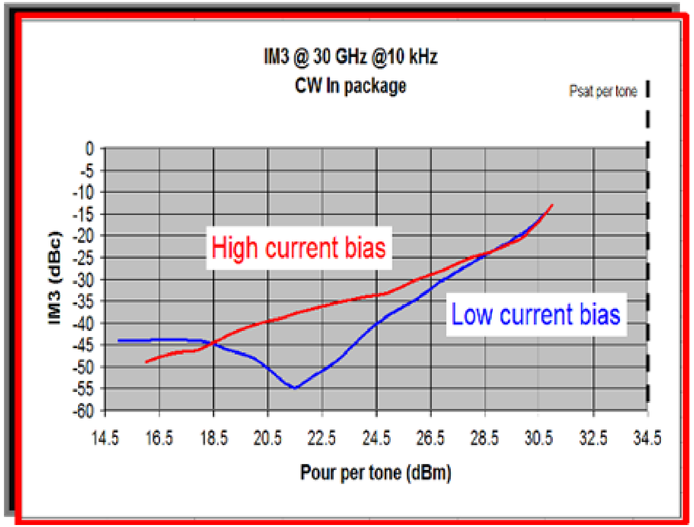
30 GHz 10 W Psat amplifier







6W PA Linearity (IM3, EVM)



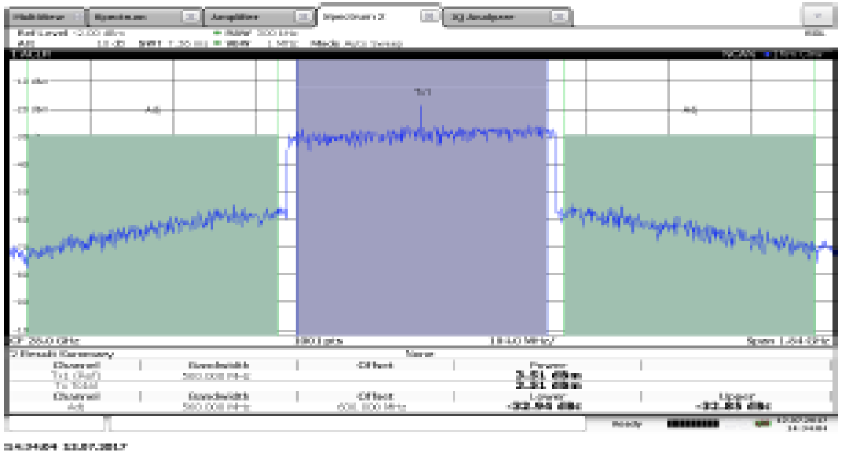
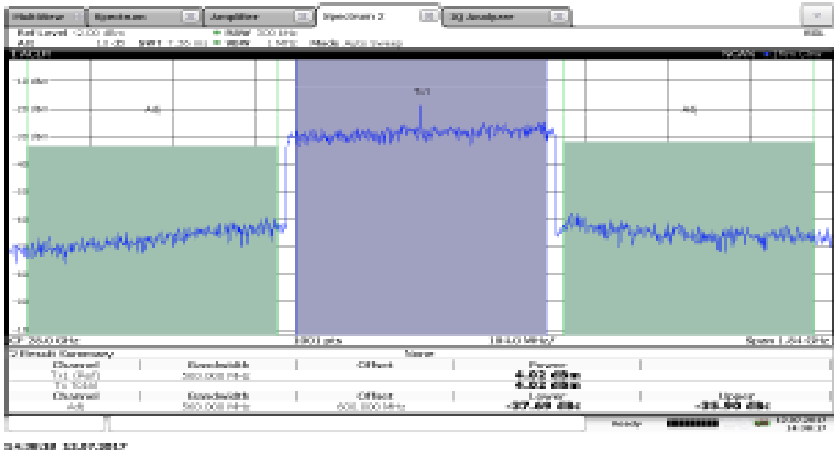
IP3= Pout+IM3/2
EVM(64QAM)= Pout/2* IP3

30GHz 5G Pout requirement is 0.5W

Tested result :
Pout : 27dBm (10dB back –off)
IM3 (10dB back –off) : -40 dBm
PAE:14%
EVM: 1%

ACLR measurements

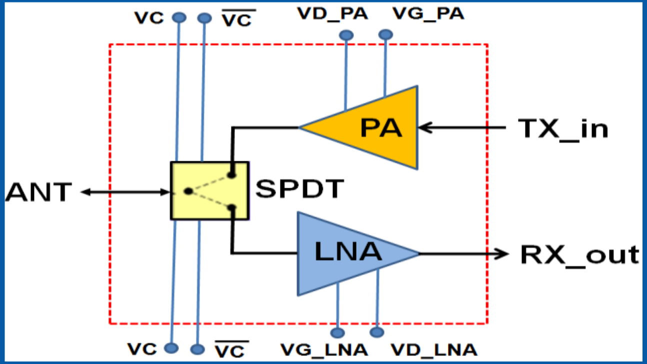
- center frequency=28GHz, Bandwidth=600MHz
- Pout=22.4dBm, PAPR=10.1dB

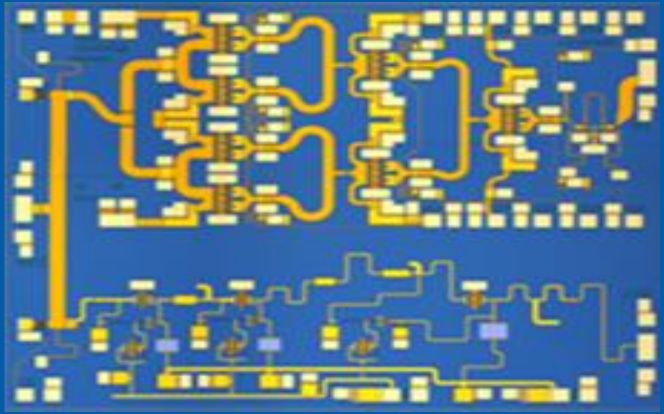
w/o DPD	w/ DPD
	
ACLR-Lower: -32.94 dBc ACLR-Upper: -32.85 dBc	ACLR-Lower: -37.69 dBc ACLR-Upper: -35.90 dBc

30 GHz T/R chip (LNA + PA + Switch)

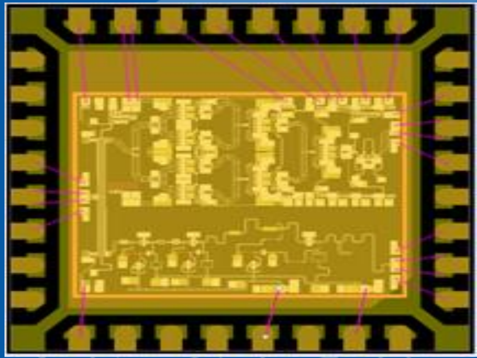
The best

5W PA, 1.2dB loss switch, 1.6dB NF LNA LNA @ 30GHz



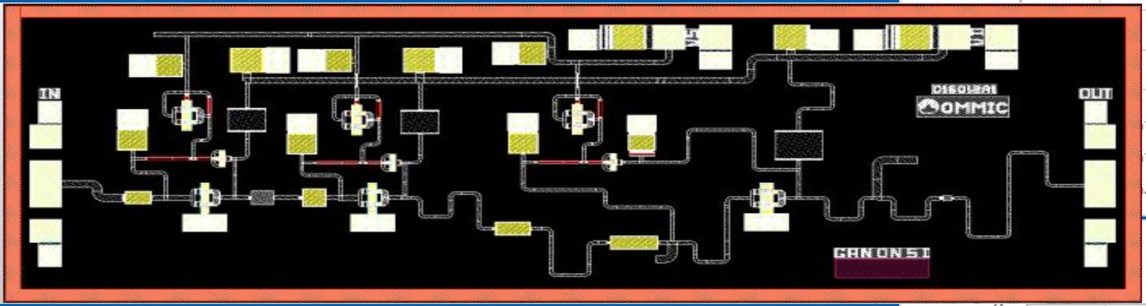


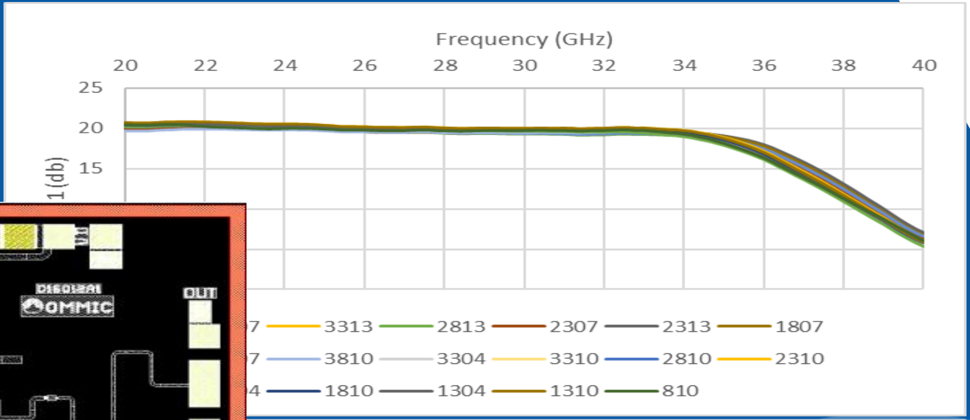
QFN5x5

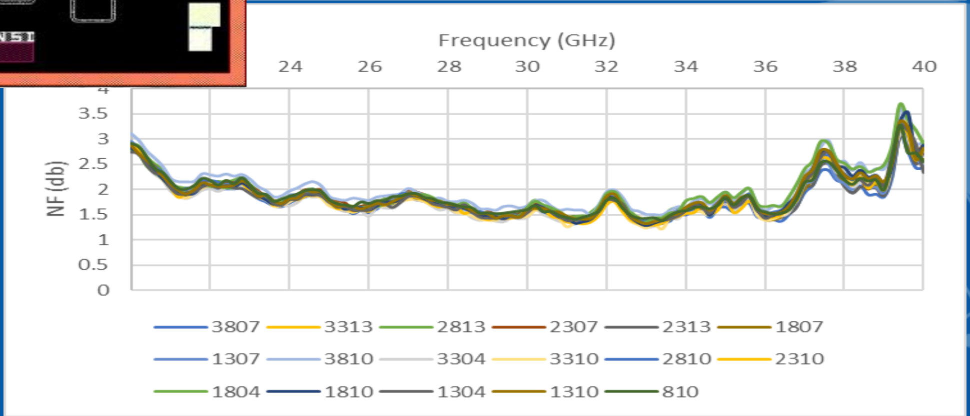


20-34 GHz GaN LNA

20dB Gain, 1.5dB NF @ 30GHz





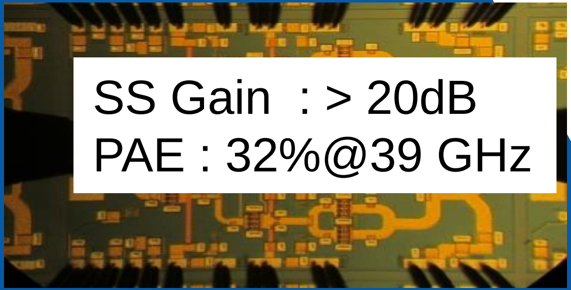


DC regulation
Single VSS, single VDD

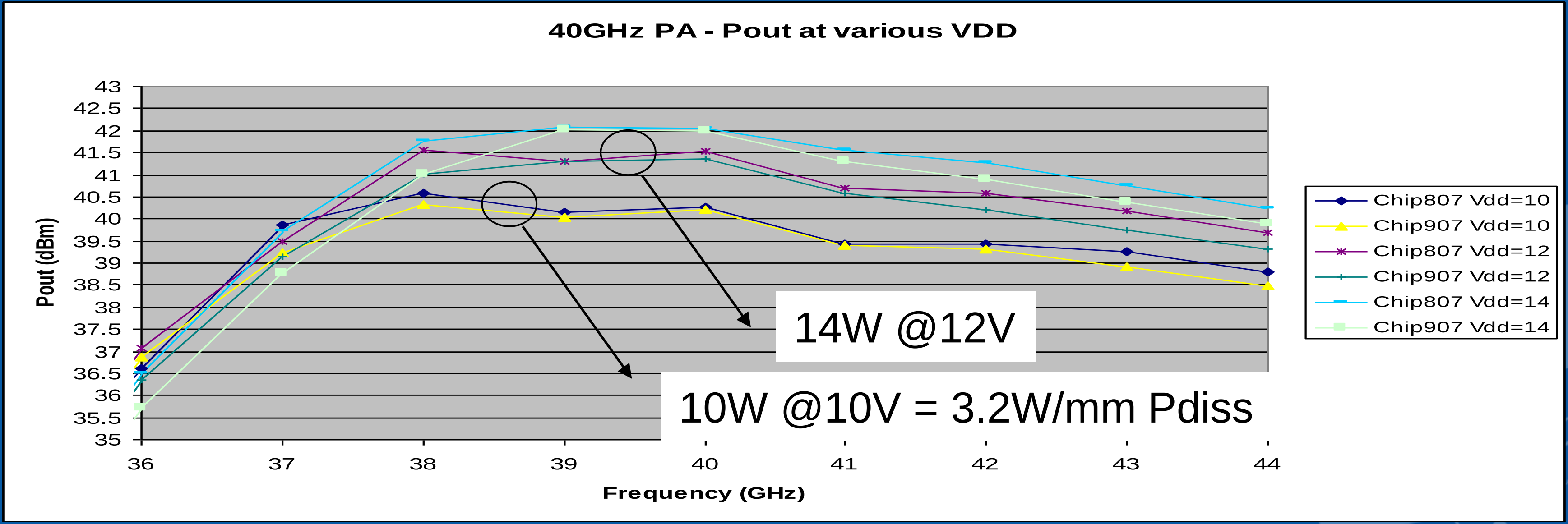
Possible VDD= 3 to 8.5V
DC current : 40 to 130mA
with little impact on performance

41dBm 39 GHz PA

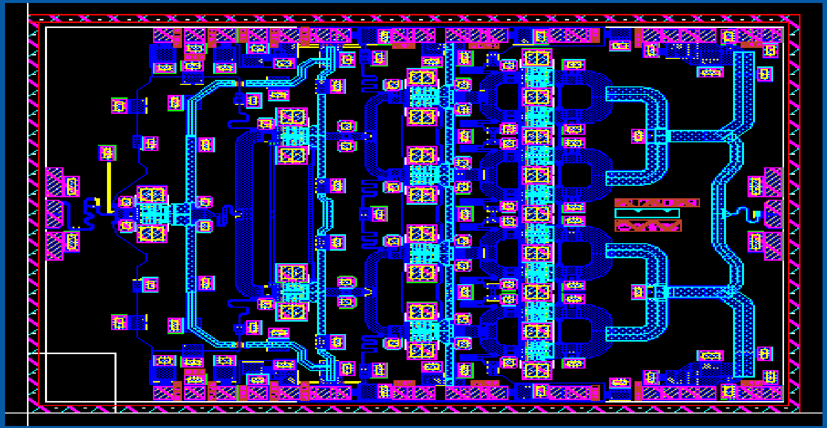
40dBm@10V, 41.5dBm@12V, 42dBm@14V



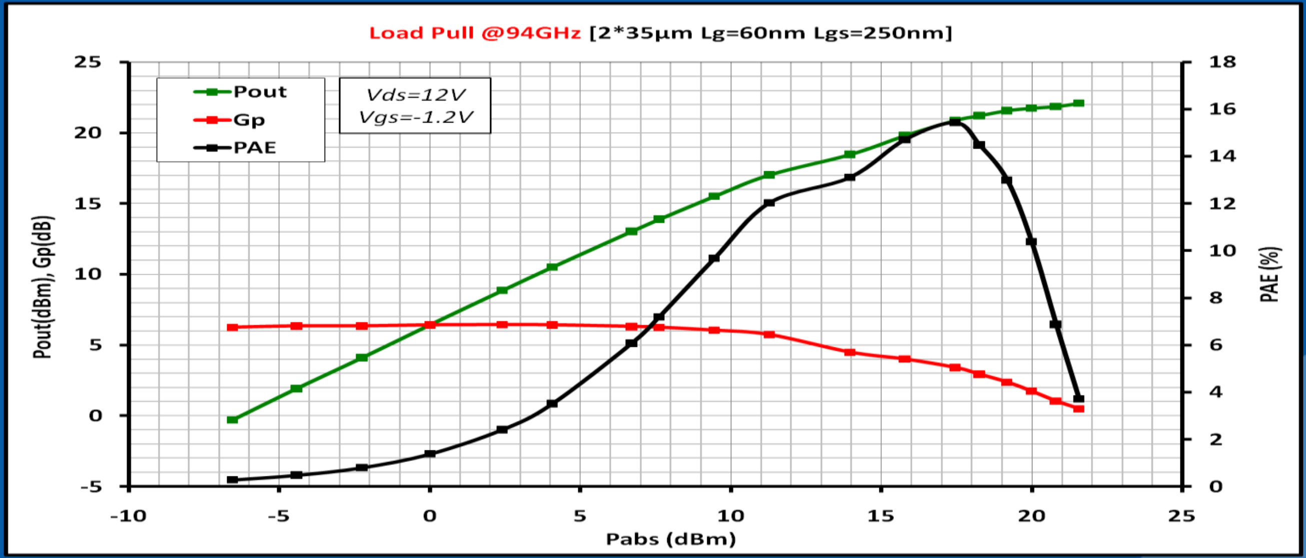
SS Gain : > 20dB
PAE : 32%@39 GHz



Q band PA
44-47GHz
37dBm, 18dB gain ,18%PAE



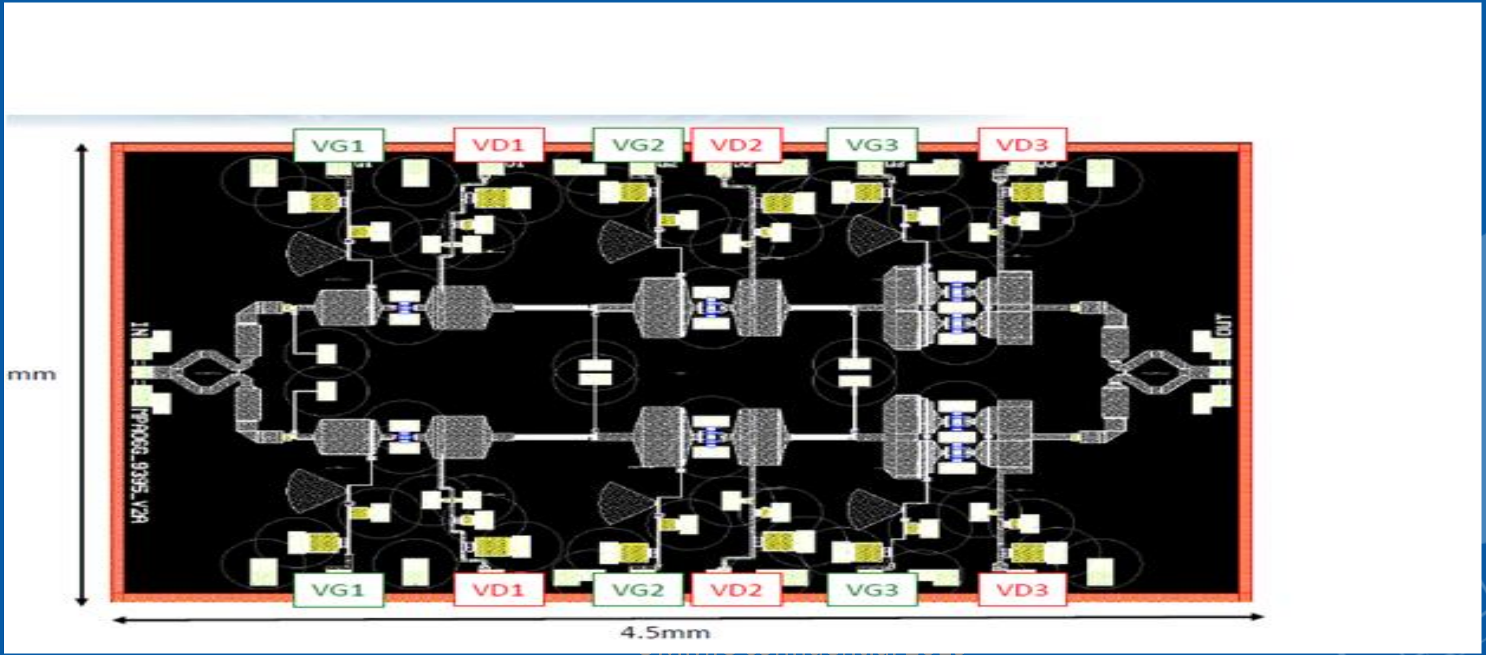
D006GH 60nmGaN/SI
Power characterization @ 94GHz [Vds=12V]



$P_{out\ Max}$ = 2.3 W/mm / PAE of 15% / $G_{p\ lin}$ = 6.45 dB

1.4dB NF @ 40GHz

W band PA
600mW, 12dB gain , 8%PAE @ 94GHz



CONCLUSION

1. OMMIC 100 and 60nm GaN/Si processes are a logical replacement of GaAs MMIC processes and a perfect complement to RF CMOS for advanced 5G systems.

2. To fully meet the cost requirements we opened our 6 inch 100nm GaN/Si line on September 26, 2017
3. The hetero-integration of Si CMOS with GaN/Si is the way to continue the TeraHertz roadmap further and achieve the ultimate level of integration with the best performance of all technologies