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Power Related Considerations in RF, Microwave and High Speed Circuits

Instructor: Steve Sandler

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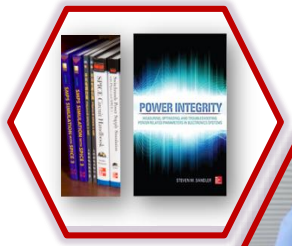
PICOTEST

Better Products Through Better Test

And Just a Bit About Steve

- 40+ Years Experience (1977-present)
- AEi Systems – Founder and CTO (1995-)
- Picotest – Founder and Managing Director (2010-)
- Test Engineer of the Year (2012-2014)
- Experience: Space Shuttle, Space Station, GPS, Large Hadron Collider and many other military and commercial projects
- Primarily focused on RF, Analog, and Distributed Power Systems

I enjoy writing



lab time

lecturing

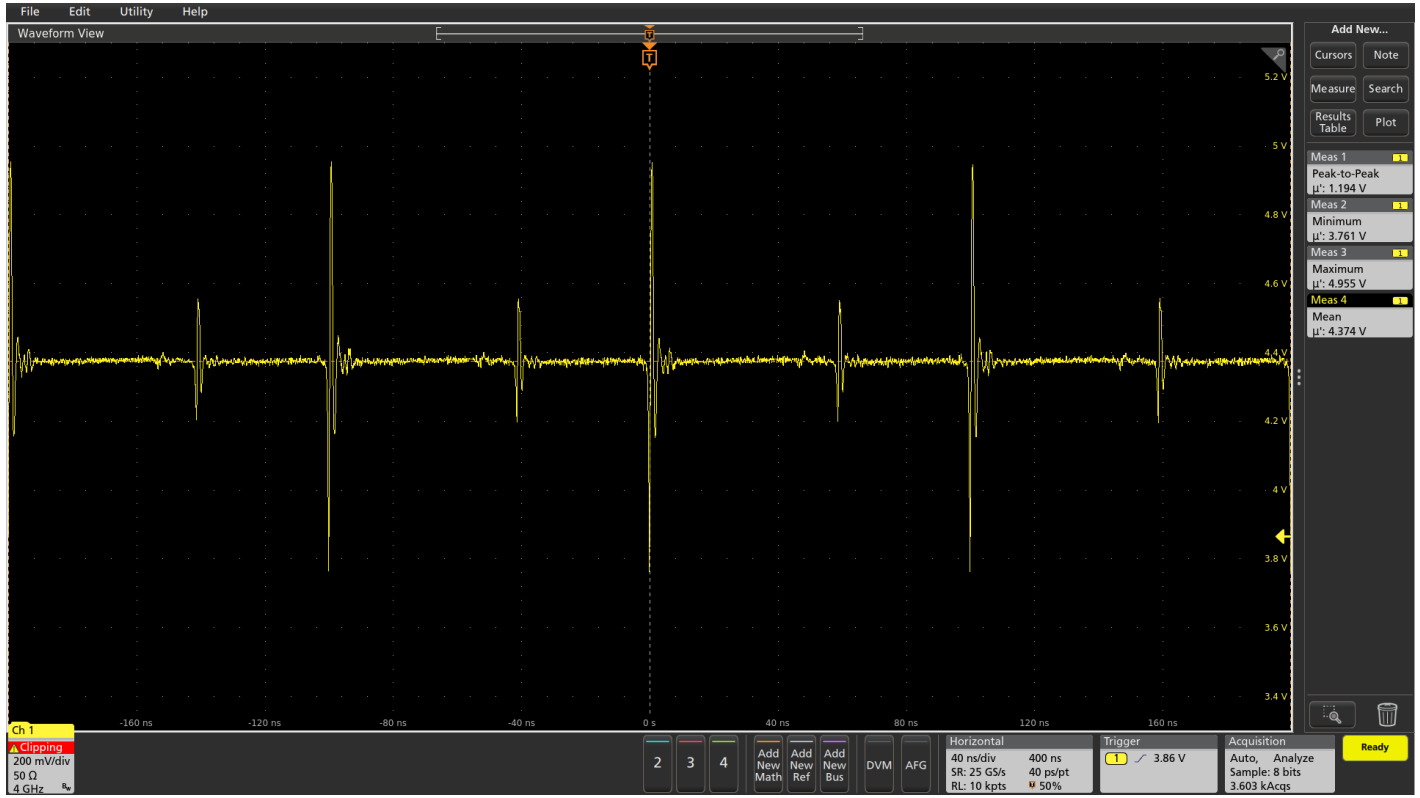
making pizza

Introduction

Most engineers associate power integrity with voltage transients, induced by high speed, high current switching and power plane decoupling.

This is only ONE source of noise and there are many other noise sources.

Today I'll show another of these noise sources and I'll share MY definition of Power Integrity.



What Experts Are Saying

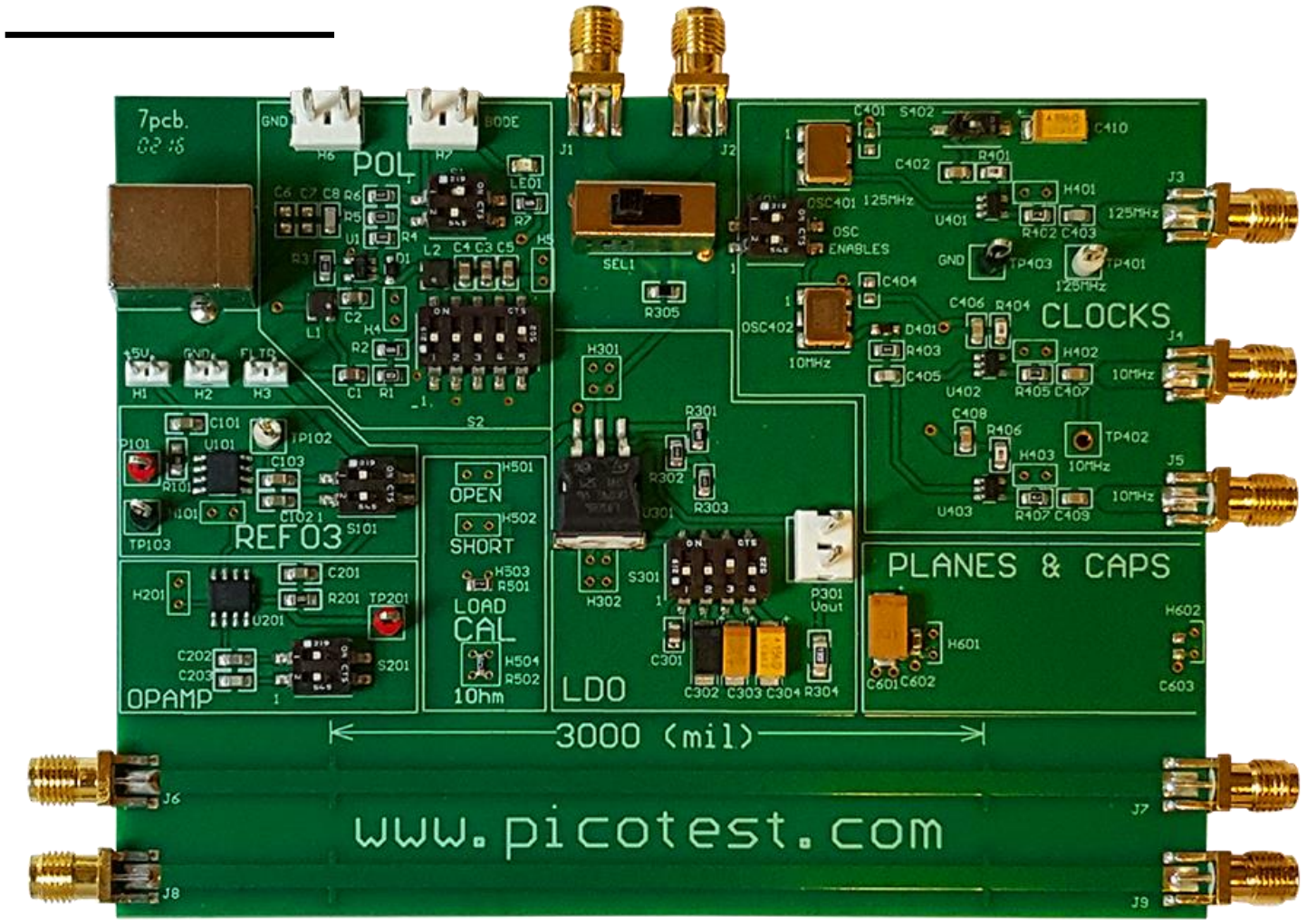
"To achieve good power integrity, we want the PDN to have the lowest impedance possible. At dc, that means having as low a resistance as possible in the plane shapes. At ac, that means minimizing the impedance between power and ground….." Patrick Carrier, What's The Difference Between Signal Integrity And Power Integrity?, Electronic Design May, 2, 2012

"Power integrity is all about the quality of the power seen by the circuits on the die." Eric Bogatin, What Exactly is Power Integrity?, Signal Integrity Journal, May 18, 2017

We All Disagree

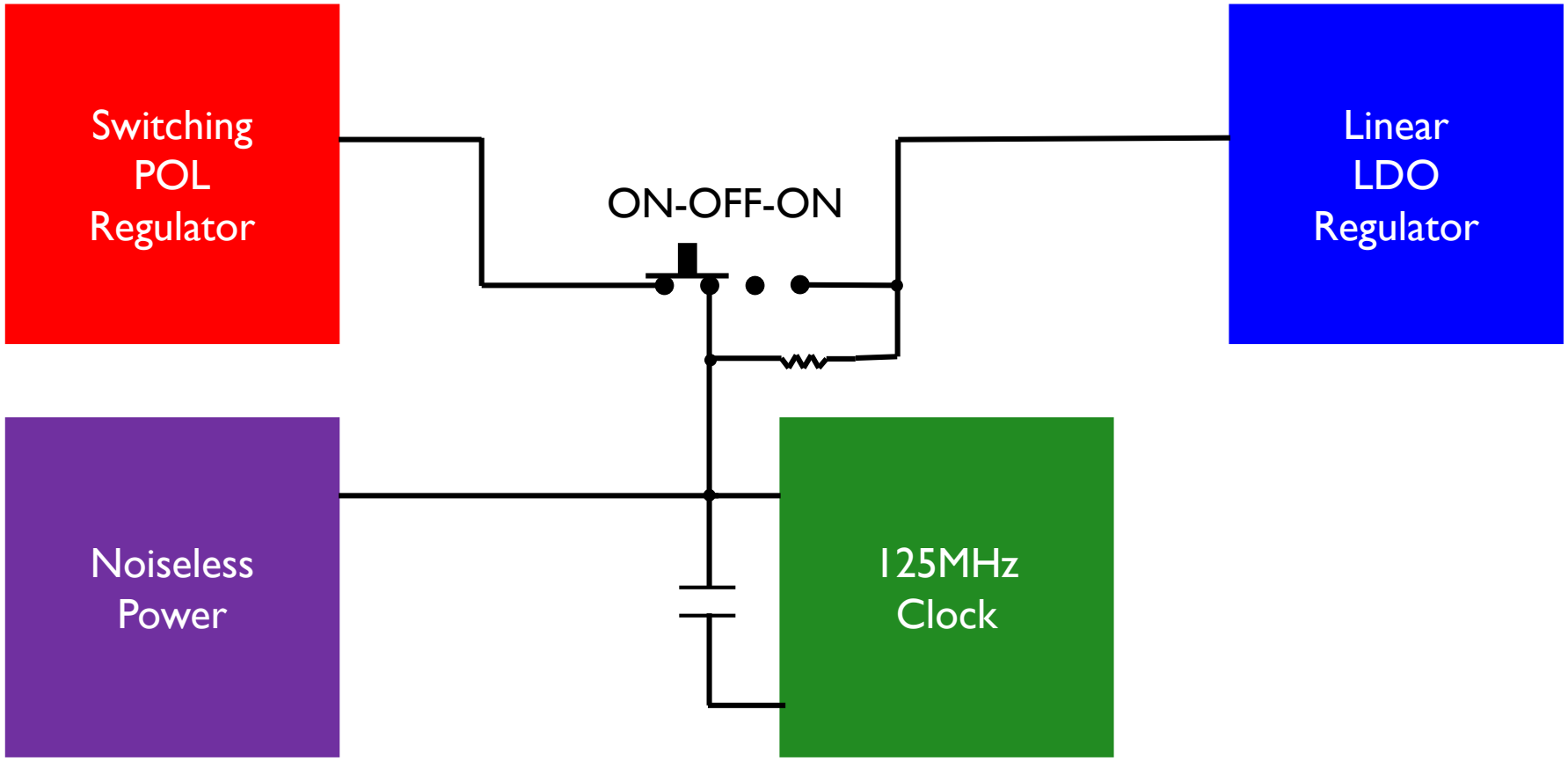
We could agree to disagree, but that won't result in a path to success

Demo Board

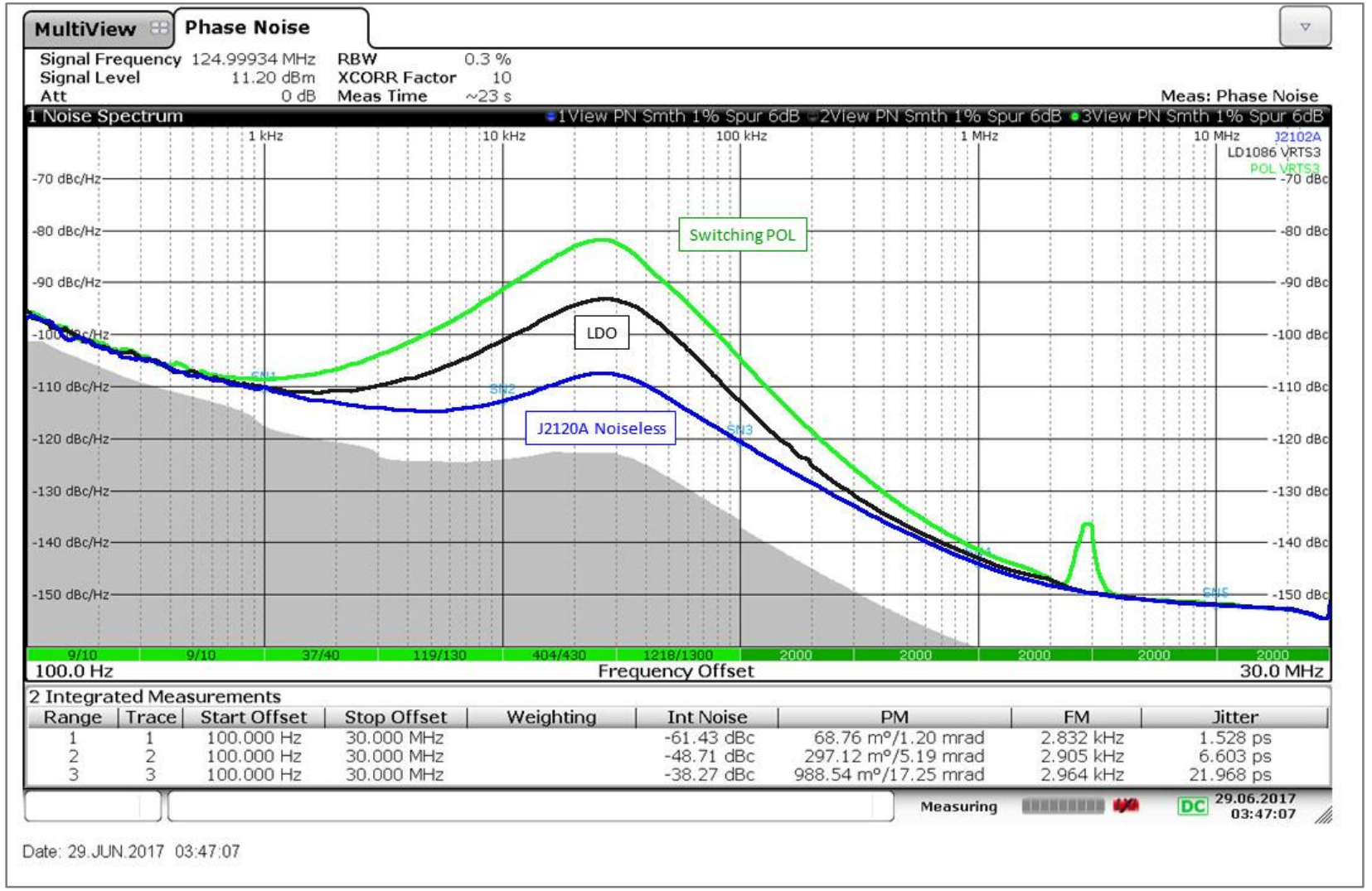


Today I'll share my own definition and hopefully convince you that Power Integrity is an ecosystem that every engineer contributes to…. either in a good way or in a bad way

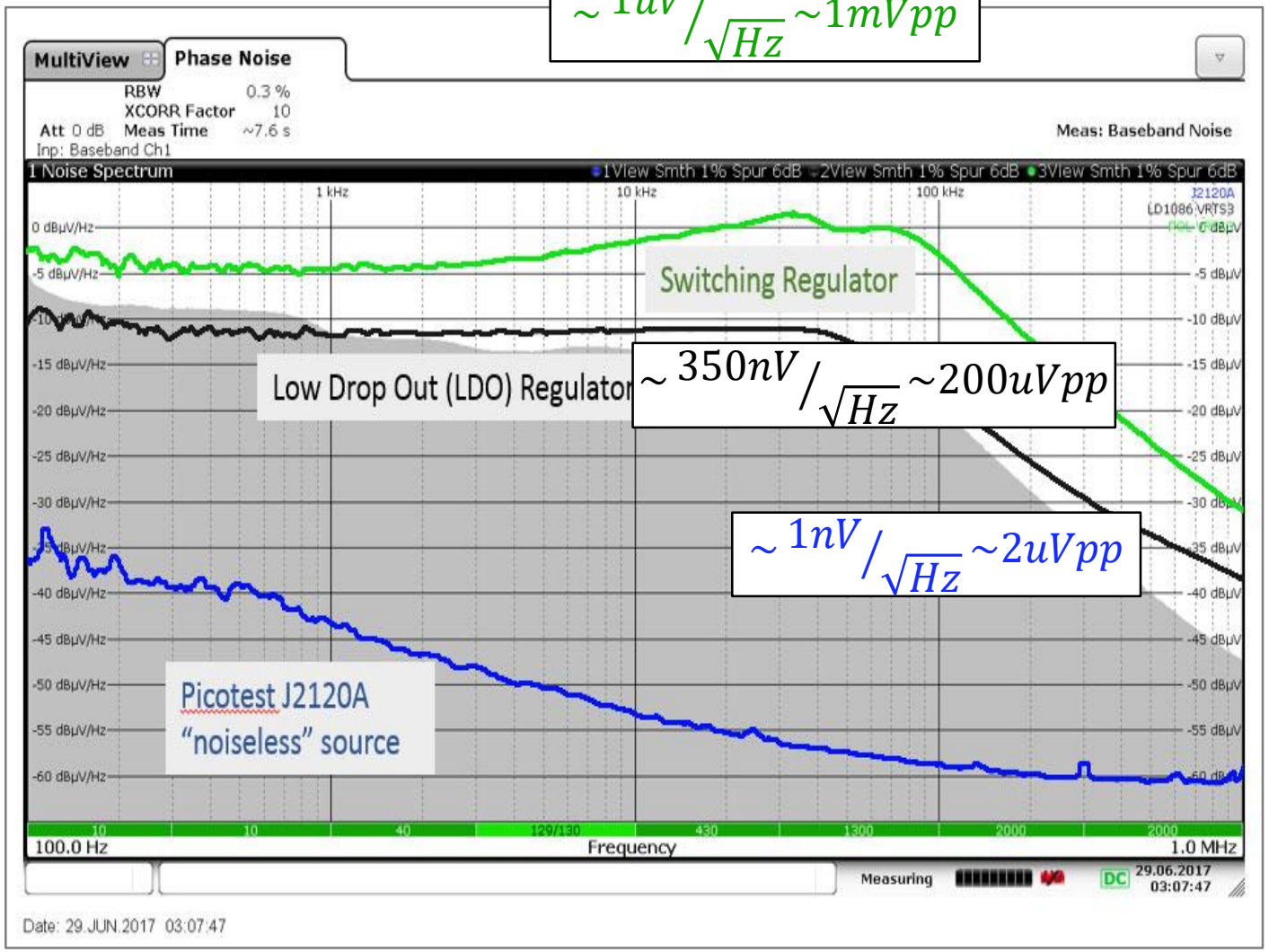
Power Integrity Ecosystem



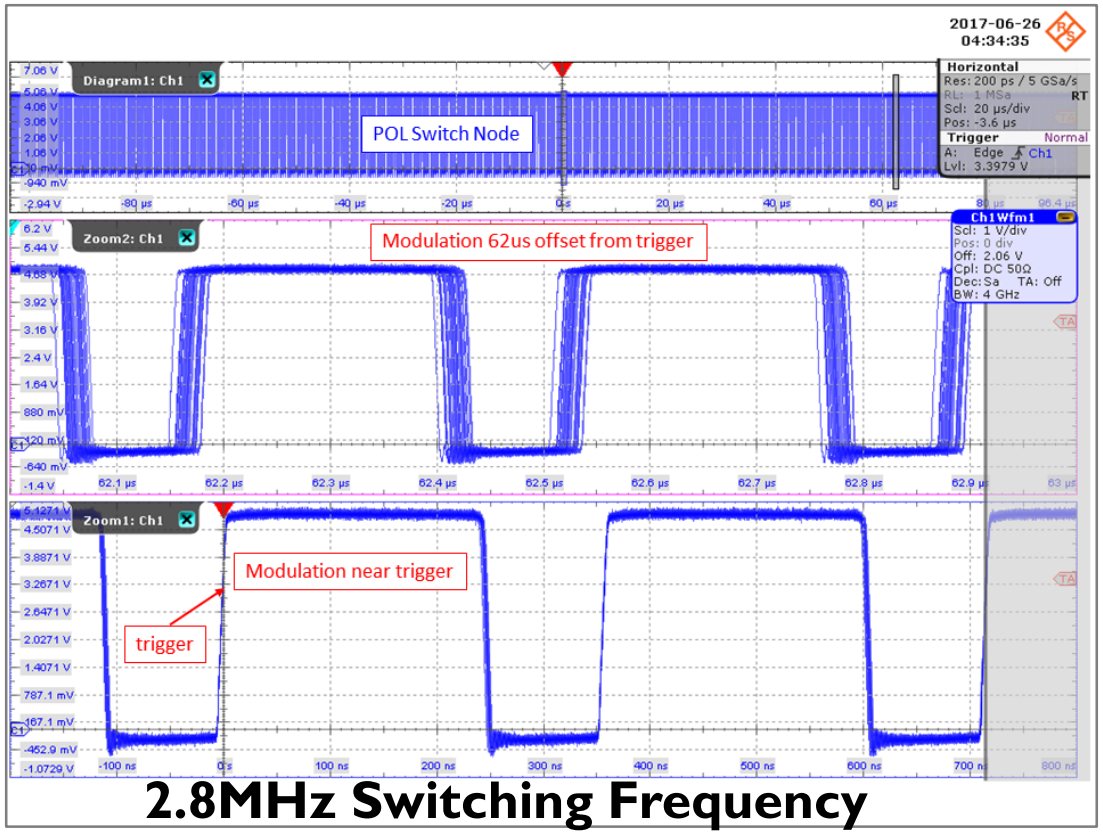
VRM Contributes to Phase Noise and Jitter



VRM Contributes to Jitter



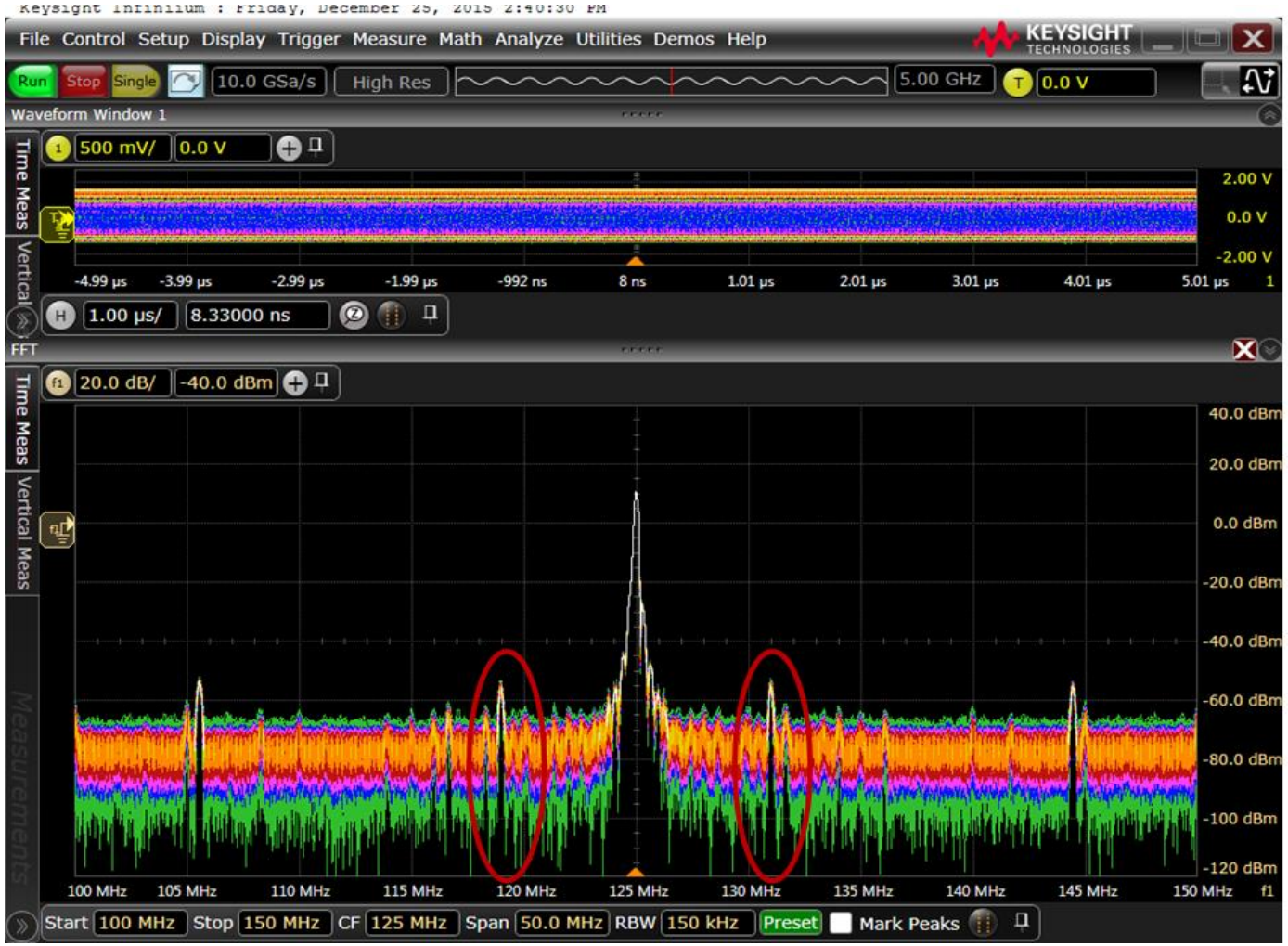
Switching Frequency Jitter Contributes to the Phase Noise!



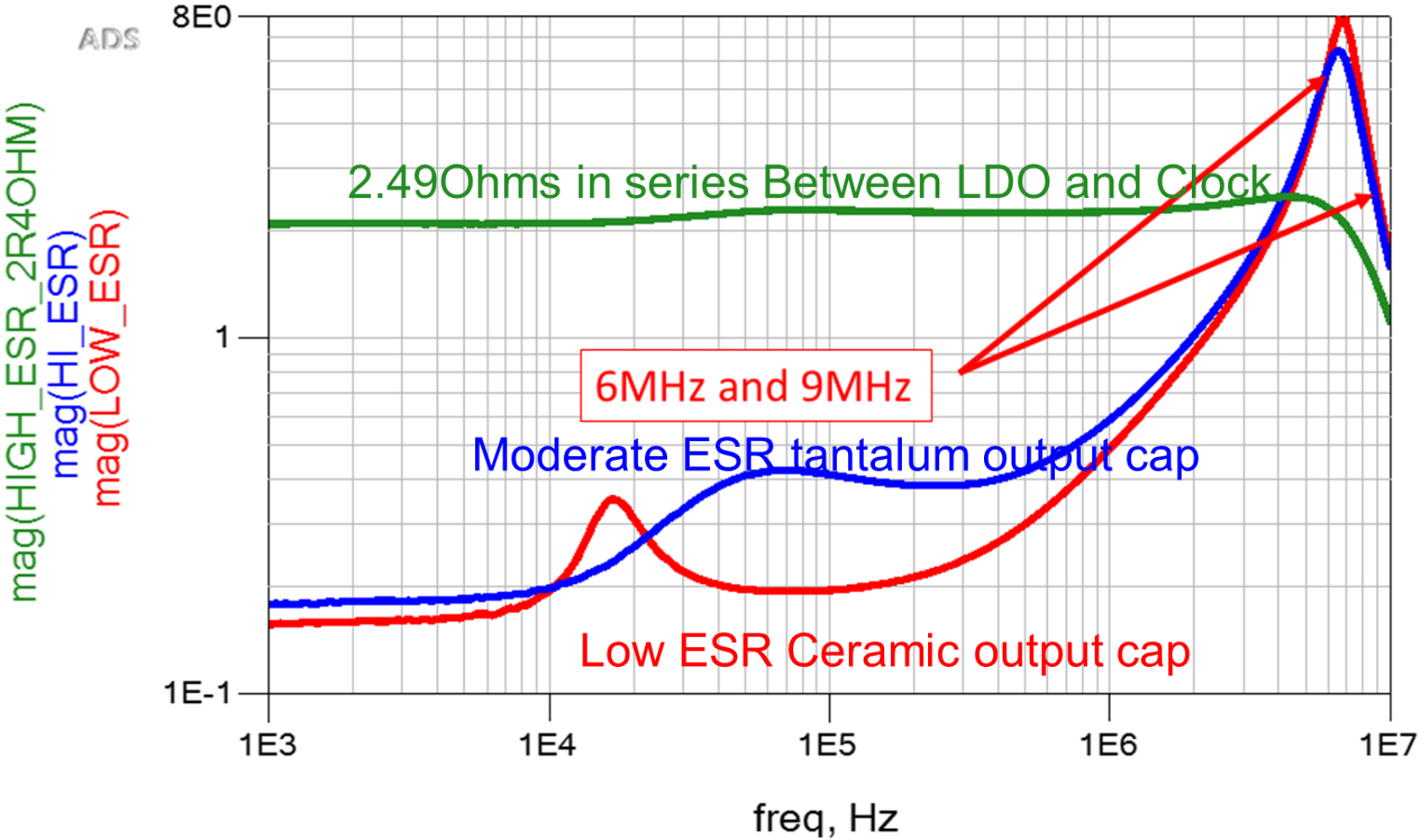
2.8MHz Switching Frequency

VRM Contributes to Phase Noise

spurs at 6MHz offset from the 125MHz clock frequency



Impedance Seen By the Clock

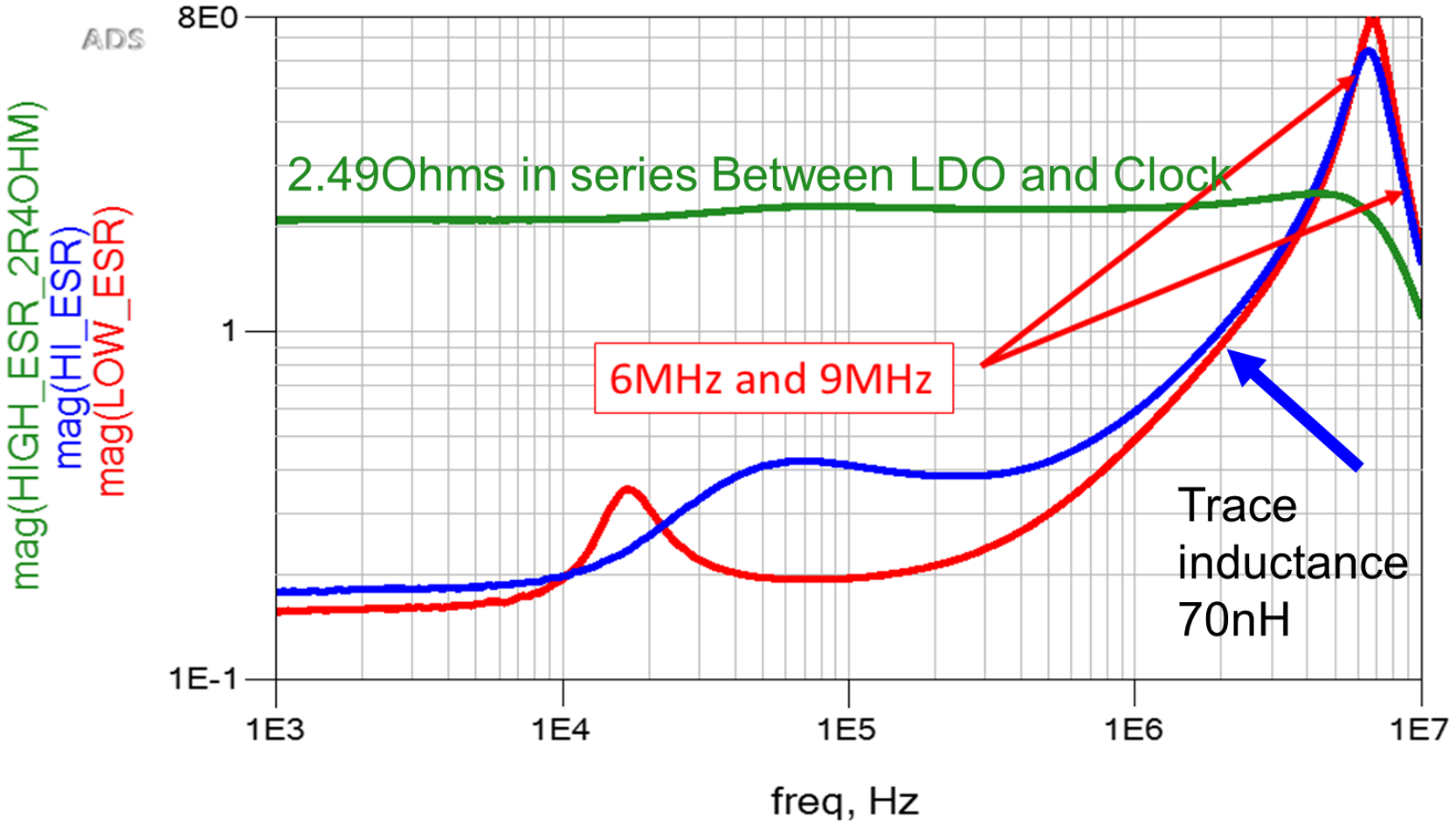


Flat Impedance Profile and Phase Noise

2.49Ω series resistor eliminated the impedance peak and eliminated the 6MHz spur

Origin of 6 MHz Antiresonance

The 6MHz impedance peak is the resonance of a 70nH PCB trace impedance and a 10nF clock decoupling capacitor



Obtaining Flat Impedance Profile

$$Trace\ Inductance = 70nH$$

$$Clock\ capacitor = 10n\text{F}$$

$$Cap_{esr} = 0.4\Omega$$

$$F_r = \frac{1}{2\pi\sqrt{L \cdot C}} = \frac{1}{2\pi\sqrt{70nH \cdot 10nF}} = 6MHz$$

$$Q = \frac{\sqrt{\frac{L}{C}}}{AC_{impedance}} = 1$$

$$Z_{clock} = \sqrt{\frac{L}{C}} = \sqrt{\frac{70nH}{10nF}} = 2.65\Omega$$

$$R_{series} \geq 2.65\Omega - 0.4\Omega = 2.25\Omega$$

Solving for C with a Q=1 results in

$$C = \frac{L}{(AC_{impedance})^2}$$

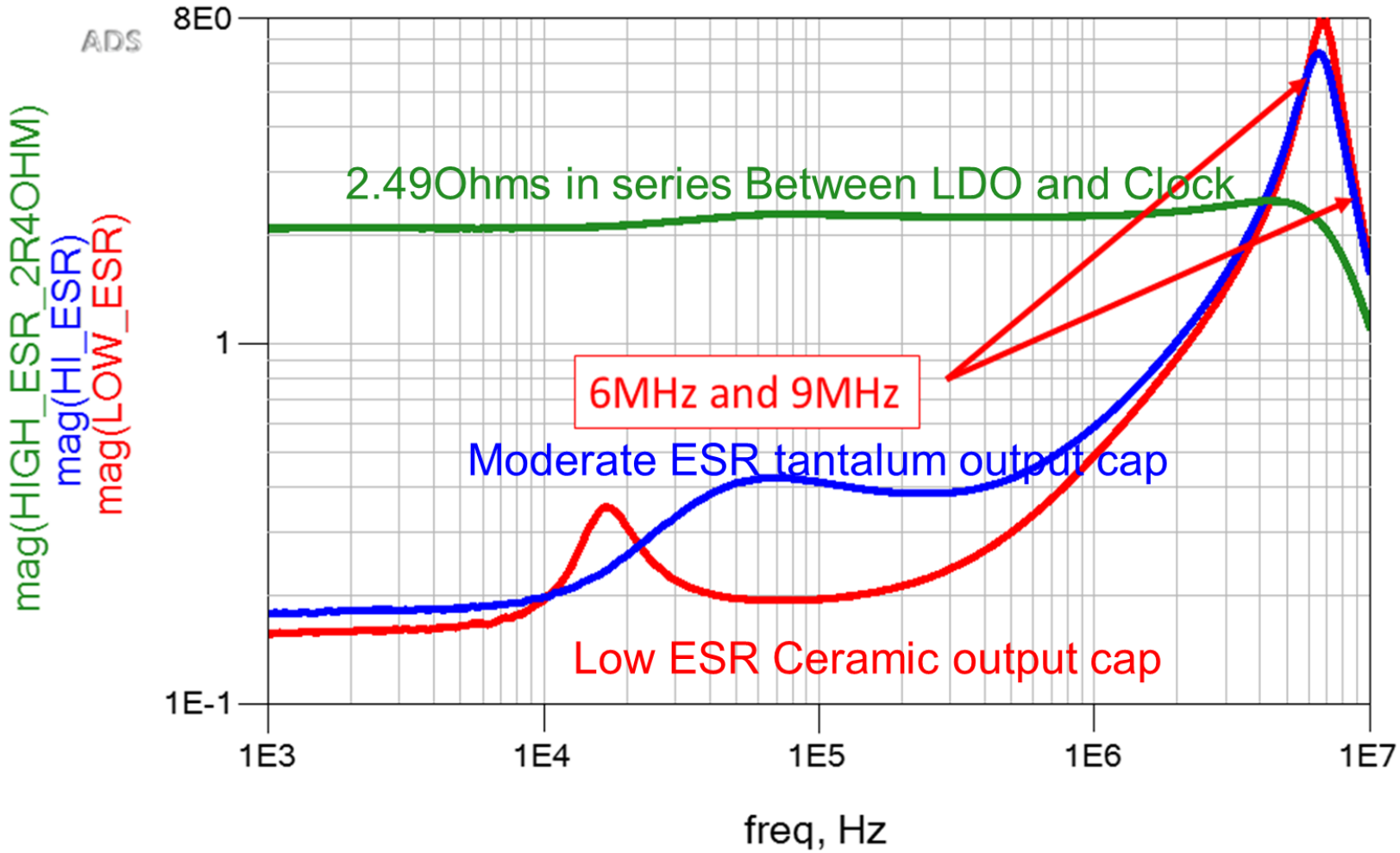
$$\text{ESR} = \sqrt{\frac{L}{C}}$$

Excitation Source for 6MHz Peak

2.8MHz switching regulator

- 2nd harmonic - 5.6MHz
- 3rd harmonic - 8.4MHz

Neither of these frequencies perfectly align with the resonant frequency, there is some small energy close to the resonance and this small energy generates the spur



Tolerance Effects

Some of the switching regulators perfectly aligning with the resonant Frequency

F_{SW}	Switching Frequency	LMR10515-X	**1.2**	1.6	**1.95**	MHz
		LMR10515-Y	**2.25**	3.0	**3.75**	

$$F_r = \frac{1}{2\pi\sqrt{L \cdot C}} = \frac{1}{2\pi\sqrt{70nH \cdot 10nF}} = 6MHz$$

$\pm$ 30%, initial, temp, age, bias

$$F_r = 5.26MHz - 6.84MHz$$

Fundamental	2nd Harmonic	3rd Harmonic
2.25-3.75 MHz	**4.5-7.5 MHz**	**6.75-11.25 MHz**

What I demonstrated here:

- Different VRMs produced different jitter
- Some Jitter was NOT related to power supply impedance, but due to regulator noise voltage
- The voltage regulator includes internally generated **expected** noise
- The voltage regulator may also include internally generated **unexpected** noise
- Creating a lower impedance power rail **increased** the noise at a spur, which was corrected by **increasing** the impedance, so we don't want the lowest AC impedance
- We had no information about the package or the die, but we **didn't really need** to
- We won't always see a power integrity issue in our measurements, so we are looking for **potential** power integrity issues in our measurements

Power Integrity is a complete ecosystem, dedicated to providing appropriate power to all load devices, without degrading other system performance. This is inclusive of **all** noise sources, both expected and unexpected.

-Steve Sandler 2019

Please feel free to:

- Connect with me on Linkedin
- Contact me directly at steve@picotest.com
- Visit www.picotest.com/blog to learn more
- Look for my next book ***Power Integrity with ADS***