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Analysis and research of sigrity integrity in the DDR Full link simulation

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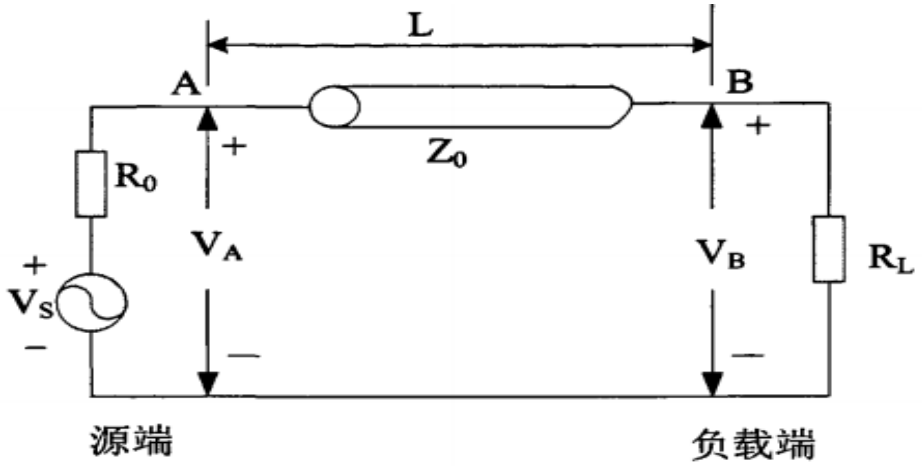
The concept of signal integrity

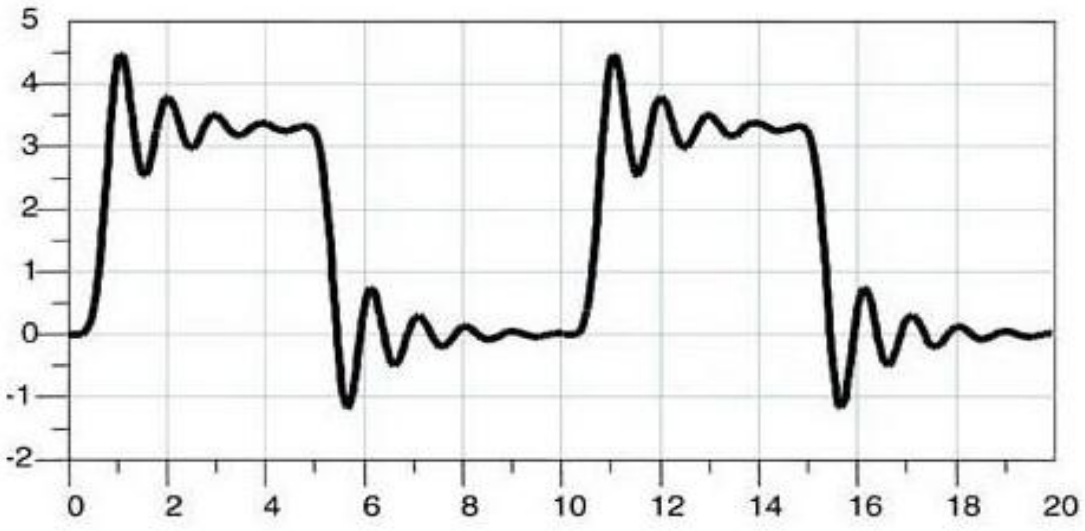
- Reflection:
- The dismatch of the impedance of driver and receiver may cause the reflection of signal . When load impedance is lower than the driver impedance ,it will be the negative reflection voltage. in contrast, it will be the positive reflection voltage. Reflection may caused by the geometry of the transmition line , dismatch terminating, and discontinuity of power and ground plane.



The concept of signal integrity

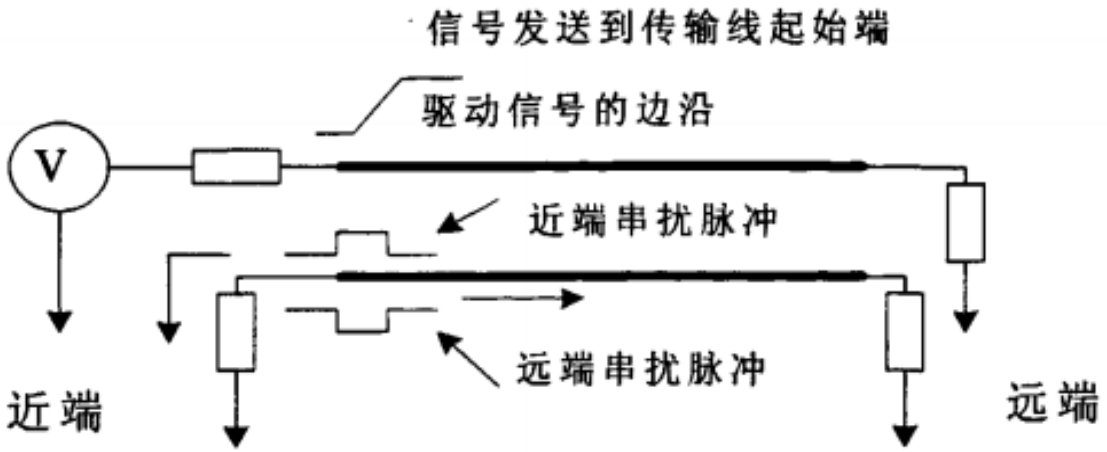
- Ringing:

The excess inductance and capacitance caused the ringing,it may be cause EMI of sinnal and make uncertainty of Judgement threshold.



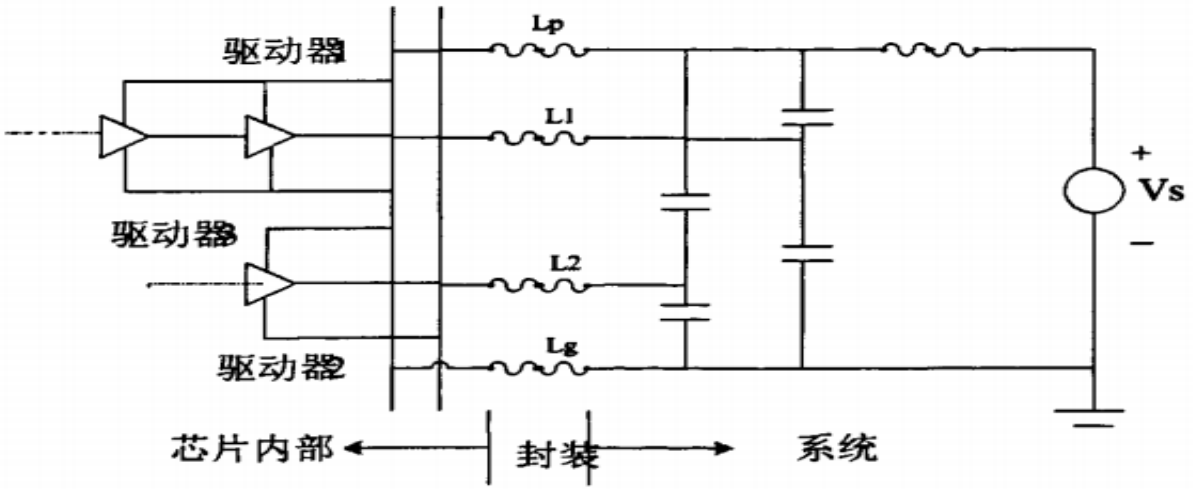
The concept of signal integrity

- Crosstalk:
- Crosstalk may be happened between the two signals coupling, mutual inductance and mutual capacitance . Parameter of PCB layers , the distance between the singlas ,the elcectrical characteristic of driver and receiver and the termination of signal ,both can bring crosstalk between signals.



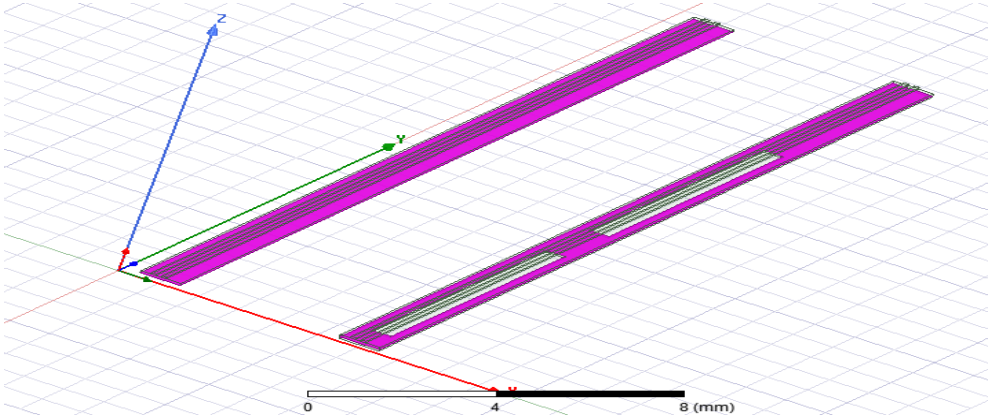
The concept of signal integrity

- SSN:
- SSN noise is caused by transient current change, when the current changed , pass through the return path's inductance, it will bring the AC voltage drop and noises. It is not only the problem of the power system ,also the appearance of ground bounce.



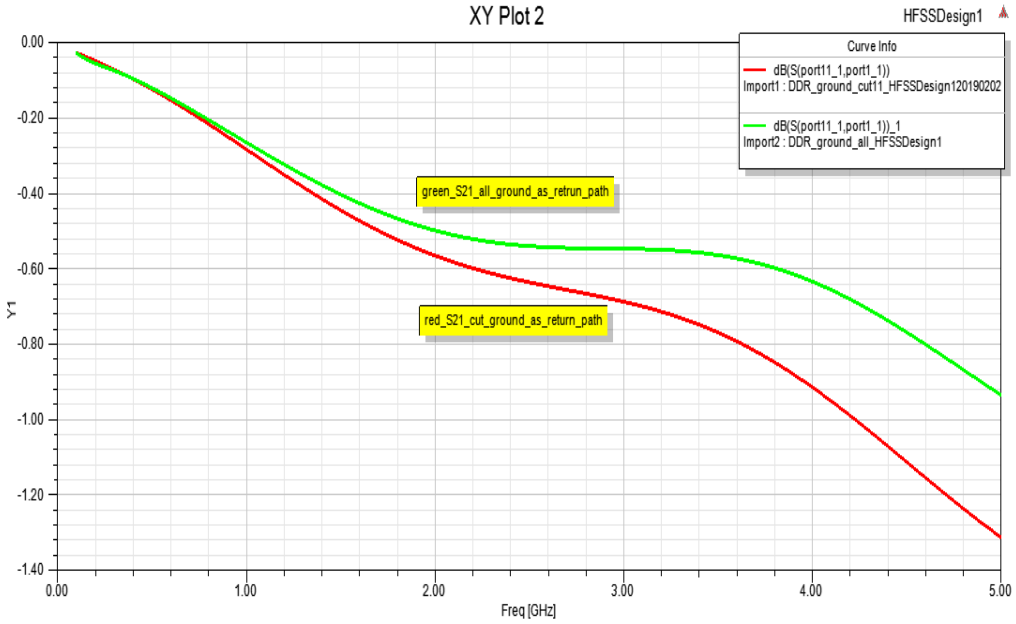
DDR full link integrity simulation

- 50ohm transmission line modeling: distance=10inch
- Left is the transmission lines with the total ground.
- Right is the transmission lines with the cutting ground.



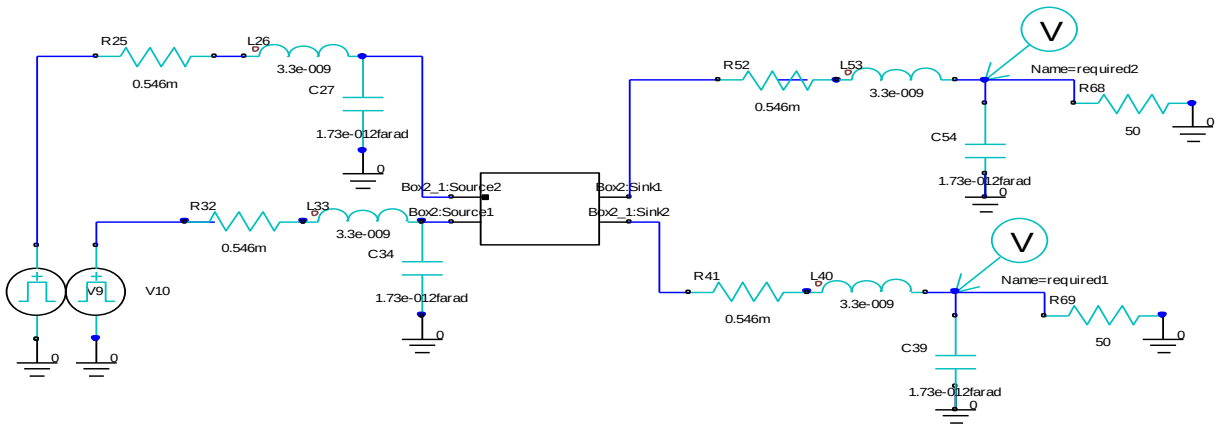
DDR full link integrity simulation

- **The simulation results of S21:**
- Green curve is the S21 parameter with the total ground as return path
- Red curve is the S21 parameter with the cutting ground as return path.



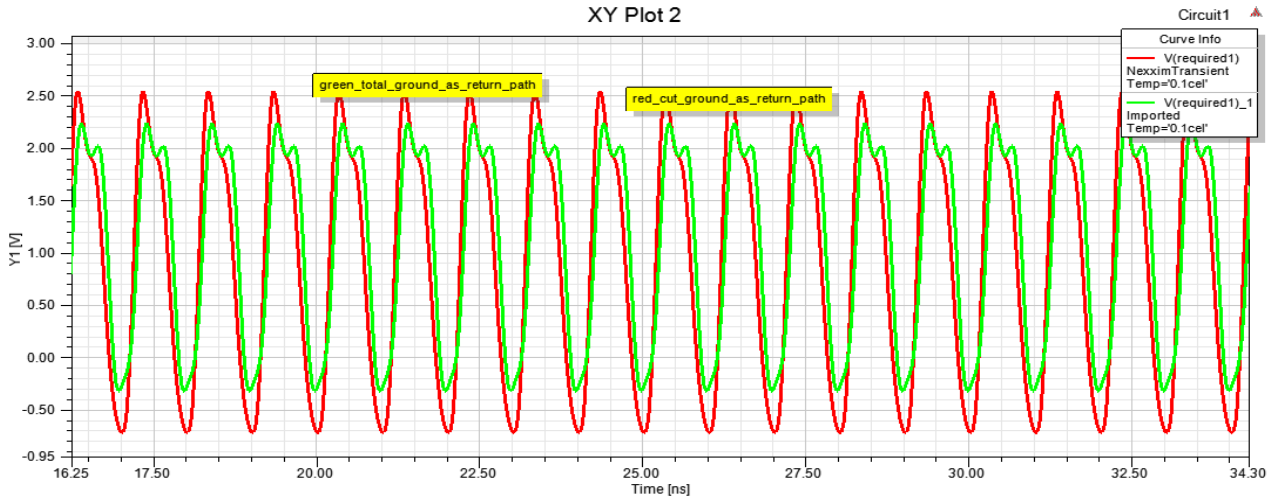
DDR full link integrity simulation

- **The simulation diagram of time domain:**
- The picture is the modeling of time domain,V pulse is the driver signal .
- V pulse parameter tr=tf=0.1ns,pw=0.5ns,per=1ns, the signal voltage=1.8V



DDR full link integrity simulation

- **The simulation results of time domain:**
- Red curve is the waveform of receiver with the cutting ground
- Green curve is the waveform of receiver with the total ground.



Thank you