Power Distribution Network Testing through Impedance Analysis

Andrea D'Aquino

Phone: +49 89 4129 13044 – E-Mail: andrea.daquino@rohde-schwarz.com
Address: Rohde&Schwarz, Dept. 1EP2, Muehldorfstrasse 15, 81671 Munich, Germany.

***Abstract* — Power distribution networks (PDN) have a primary role in printed circuit boards (PCB). The correct design of these important electronic structures ensures stability across the whole board, allows the transit of high-speed signals in a low-noise environment, and has direct influence on electromagnetic emissions reduction. This paper explains how the impedance of these circuits is a metric of stability and a yardstick for the board optimization. Finally, a PDN test setup is proposed, where the impedance of a device under test (DUT) is evaluated through the impedance analysis function of a vector network analyzer (VNA).**

I. INTRODUCTION

In the electronics industry, the use of printed circuit boards is nowadays very common, and phenomena such as miniaturization and integration of components, have brought emphasis on the topic of board surface optimization in a market already hungry for cost-efficient solutions. Furthermore, considering a global PCB market value of 63.1 billion USD in 2017 and a forecast of 76.9 billion USD in 2024 [1], it is clear why this aspect of engineering has gained popularity. The power distribution networks (PDN) often present the biggest challenge for the above-mentioned task, since the interconnects from the voltage regulator module (VRM) to the various components, traces, wires, etc. usually constitute the largest conductive network on the board. This makes PDNs the object for most of the trade-off choices between costs, features, minimization of unwanted electromagnetic effects, and adaptation to the served loads. Therefore, it is important that testing solutions for PDN are precise as well as low-priced.

II. DEFINITION OF PDN

PDN defines the network of connections between the VRM and all the terminations on the board that require a power supply (usually chips, but also capacitors, other circuits, etc.). Each single path from VRM to load can be represented by a transmission line. The combination (series and/or parallel) of each individual branch, whose load is also the combination of each individual load, models the complete PDN.

Consider the simplest case of PDN, where a VRM is connected to a single chip via a conductive trace: Z_L is the impedance of the chip and Z_{PDN} the impedance of the conductive path from VRM to chip, as seen by the chip pads due to the well-known physical effects of a generic transmission line. It is possible that the current I_L drawn by the load fluctuates, and if this happens, the VRM compensates by regulating its output, so that the voltage at the chip's pads is kept stable. In this transient phase, the ripples of the PDN input current contain a spectrum of frequencies, which "see" different impedances Z_{PDN}, and subsequently affect the voltage on the chip pads V_L:

$$\boldsymbol{V_L}(f) = \boldsymbol{Z_{PDN}}(f) \cdot \boldsymbol{I_L}(f) \qquad (1)$$

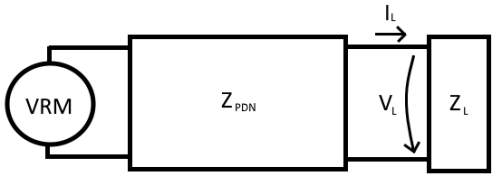

Figure 1 – Simple model of a power distribution network

VRMs can compensate low frequency transients without problems [2], and it is instead interesting to see how the circuit behaves in presence of noise at higher frequencies due to VRM switching, during power-on phase, due to interferences, etc., because in the worst case the above-mentioned noise can even destroy the load.

III. PDN DIMENSIONING

Chips usually allow some voltage deviation (ripple or voltage noise tolerance) from the specified required one ($V_{L\ spec}$), but undoubtedly Z_{PDN} should be dimensioned in a way that does not let V_L exceed these deviations in order to keep the chip working as intended with the lowest possible noise.
This happens if[1]

$$Z_{PDN\ target} < \frac{V_{L\,noise}}{I_{L\,worst-case}} \qquad (2)$$

[1] $Z_{PDN\ target} \cong \frac{V_{L\,noise}}{I_{L\,worst-case}}$ *usually represents an optimization "sweet spot", where the PCB circuit development costs are minimized. More information on the dimensioning of the PDN target impedance can be found in [2] and [7].*

where $V_{L\ noise}$ is equal to $V_{L\ spec}$ multiplied by the maximum allowed percentage of ripple

$$V_{L\,noise} = V_{L\,spec} \cdot V_{ripple\%} \quad (3)$$

and $I_{L\ worst\text{-}case}$ the highest peak of transient I_L in the frequency range from direct current (DC) to the highest significant frequency of the noise (possibly its main harmonics – usually > 100 kHz [5]).

When more loads are served by the same VRM, not only all the resistive, inductive and capacitive effects of every supply path play a role, but also those of their interconnects.
Additionally, the constant electric potential that allows DC currents, causes voltage drops at every instance of PDN interconnect due to their impedance (voltage divider principle). This does not only affect other components' required input voltage, but may lead to more fluctuations in the current, which ultimately alter the Z_{PDN} as explained in equation (1).
It should be taken also into account that different components might be connected, and each load could even be subject to changes depending on its working mode.

The optimal fit of a PDN to a certain circuit will not be discussed further, because its design is not the focus of this article. The curious reader will be able to find a vast amount of literature (e.g.: [7]) on the topic.

In fact, this paragraph's aim is to argue for the test setup starting assumption: in equation (2), since the voltage noise tolerance $V_{L\ noise}$ is usually small in respect to $I_{L\ worst\text{-}case}$, the resulting $Z_{PDN\ target}$ is most often a fraction of Ohm. This applies from DC to frequencies well above the clock [5].

IV. IMPEDANCE MEASUREMENT WITH A VNA

In order to determine if the power supply on a PCB works as intended, it is necessary to assess whether the PDN has the correct impedance. This kind of test can be easily performed with a VNA by probing the PCB on its PDN "access points" (usually capacitors).

A VNA is an *n*-port device capable of sending waves (a_p) from the *p*-th ($p = 1, 2, \ldots, n$) port to a device under test, and receiving both the reflected wave at the same port (b_p) and the transmitted ones at other ports ($b_q = b_1, b_2, \ldots, b_n$, *when* $q \neq p$).

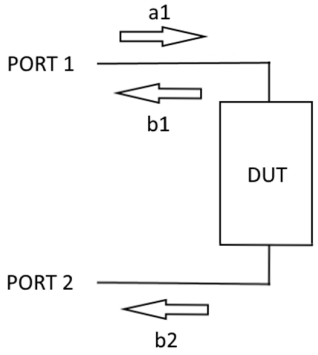

Figure 2 – Simplified model of a 2-port, unidirectional (port 2 does not deliver any stimulus) VNA connected to a DUT

Most of the VNAs have their ports matched to 50 Ω, which means that the impedance that the DUT sees at its connection planes with the VNA is 50 Ω. A straightforward consequence is that in this case a wave incident to a DUT whose impedance is 50 Ω is not subject to any reflection[2].

The reflection coefficient Γ of the DUT measured at the *p*-th port is in fact [3] equal to the ratio between the reflected wave and the incident one when there is no wave transmitted (see also (6)), and depends on the port and DUT impedances:

$$\Gamma = \frac{\frac{Z_L}{Z_p} - 1}{\frac{Z_L}{Z_p} + 1} \quad (4)$$

or

$$\Gamma = \frac{Z_L - Z_p}{Z_L + Z_p} \quad (5)$$

where Z_L is the DUT (or load) impedance, and Z_p the impedance at the same *p*-th port that transmitted the wave.
The ratio between b_p and a_p when $b_q = 0$ is the quantity measured from the VNA known [3] as scattering parameter (or S-parameter) S_{pp}:

$$\Gamma = \left.\frac{b_p}{a_p}\right|_{b_q=0} = S_{pp} \quad (6)$$

$b_q = 0$ is a condition realizable by not connecting the DUT to any other port *q*, and instead shorting that end.

The impedance of the DUT can be calculated by using the formulas (5) and (6):

$$Z_L = Z_p \cdot \frac{1 + S_{pp}}{1 - S_{pp}} \quad (7)$$

[2] *When the impedance between ports, cables and DUT does not change, there is in reality no mismatch between them. A calibration ensures that the VNA ports' characteristics shift to the DUT connection plane: the path of the wave from/to DUT through the cables and to/from the VNA ports is corrected in post-processing.*

Notice that (7) is also the solution of the following circuit when V_S is the VNA voltage source, and the waves are described by (8) and (9):

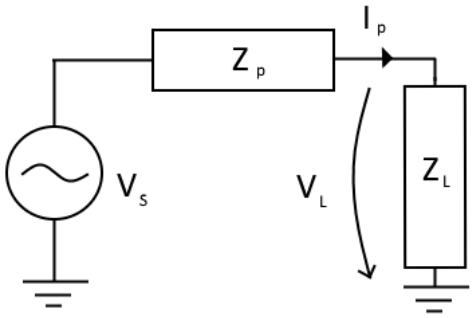

Figure 3 – Equivalent circuit of impedance measurement with VNA through reflection setup

$$a_p = \frac{\sqrt{|\mathrm{Re}(Z_p)|}}{2|Z_p|}(V_L + Z_p I_p) \qquad (8)$$

$$b_p = \frac{\sqrt{|\mathrm{Re}(Z_p)|}}{2|Z_p|}(V_L - Z_p I_p) \qquad (9)$$

These formulas are useful only if Z_L is measured with a certain accuracy. According to the example in [4] for reflection measurements, enough accuracy is obtained when $1\ \Omega \le Z_L \le 2\ k\Omega$. Considering the statement at the end of paragraph III, this measurement is not helpful to calculate $Z_{PDN\ target}$. However the theory explained up to this point helps further.

Until now, the transmitted wave was neglected, but it can actually be used to measure Z_L too. Given equation (6), the transmission coefficient, also defined as the ratio between incident and transmitted wave, must be:

$$1 - \Gamma = S_{qp} = \left.\frac{b_q}{a_p}\right|_{a_q=0} \qquad (10)$$

Let p = port 1 and q = port 2.
Notice that in this case the impedance at the ports (Z_1 and Z_2) can differ due to a VNA imperfect symmetry, finite accuracy, etc.
Similarly to (7), $1 - \Gamma$ can be measured from a VNA as the S-parameter S_{21}.

Consider the following circuit:

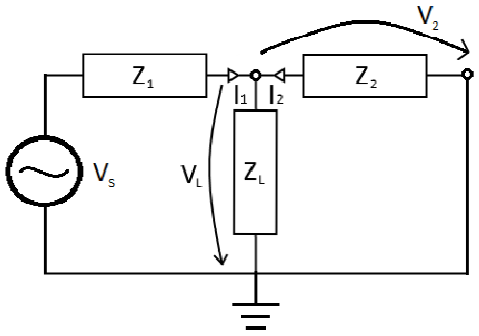

Figure 4 – Equivalent circuit of impedance measurement with VNA through shunt transmission setup

Setting this up with a VNA is very easy: Z_L is on one end connected in parallel to both port 1 and port 2, and on the other end with the VNA ground.
In this setup, the information on Z_L is contained in S_{21}, that is the ratio of the wave received by port 2 (V_2) and emitted by port 1 source (V_S).
For this setup it can be demonstrated (see appendix) that the load impedance is calculated as follows:

$$Z_L = \frac{\sqrt{Z_1 Z_2}}{2} \cdot \left(\frac{S_{21}}{1 - S_{21}}\right) \qquad (11)$$

In the example shown in [4], the impedance for this setup could be measured with a sufficient accuracy for $1\ m\Omega \le Z_L \le 225\ \Omega$, which is the range needed to measure low (considering (2)) impedances[3], thus making the shunt setup ideal for testing the PDN.

V. PDN IMPEDANCE MEASUREMENT SETUP

It is paramount, for the measurement of PDN impedance, to select a VNA with specific characteristics that support the measurement itself. In accordance with the previous paragraphs, a VNA should feature:

- Two ports, so that the S_{21} can be measured
- Frequency range starting as low as possible and stretching at best to the highest frequency of third harmonics of transient currents
- High reflection and transmission accuracy to be able to measure a broad range of impedances with low uncertainty[4]
- Good test port matching to avoid imprecise measurements: (11) shows a clear dependency of the measured Z_L from the test ports' raw impedance
- A function allowing impedances calculation with the shunt-connection formula (11)

[3] *Another example in [4] shows by connecting the load in series with Z_1 and Z_2, a sufficient accuracy is obtained for $10\ \Omega \le Z_L \le 2.5\ M\Omega$.*
[4] *Both measurement techniques (reflection and transmission) rely respectively on reflection and transmission accuracy. Low-performance VNAs measure with a very high percentage of uncertainty. A mathematical explanation for this will be provided in the appendix.*

- Availability of a OSM/OSL (open-short-match/load[5]) for the reflection measurement technique and at least "one-path-two-ports" calibration for the shunt measurement technique

Additionally, most VNAs require special probes that work in the same frequency range and can be placed on access points to the PDN.

These probes play a role in (11) as well. It is in fact worth noticing that when $S_{21} \rightarrow 1$, the measurement of Z_L loses significance because $Z_L \rightarrow \infty$, and that the addition of a probe with an impedance different from 50 Ω between the DUT and a port acts as an impedance (Z_P) in series with the port's own Z:

$$Z_L = \frac{\sqrt{(Z_1+Z_{P1})(Z_2+Z_{P2})}}{2} \cdot \left(\frac{S_{21}}{1-S_{21}}\right) \quad (12)$$

This has an interesting aftermath: when $S_{21} \rightarrow 1$, $Z_L \rightarrow \infty$ slower than in (11), and this makes the measurement of higher impedances possible.
More precisely, the measurable impedance is indicated in comparison with (11) by a multiplier:

$$m = \sqrt{\frac{(Z_1+Z_{P1})(Z_2+Z_{P2})}{(Z_1 Z_2)}} \quad (13)$$

Ideally, both the test ports impedances Z_1 and Z_2 are resistive and perfectly matched to *50* Ω. Considering a pair of probes just as ideally resistive, if $Z_{P1} = Z_{P2} = R_P = 450$ Ω, then m would yield 10:1, which is also the jargon to define a specific kind of probes.
According to the example in [4], by using these probes in a shunt setup, it is possible to determine impedances within $10\ m\Omega \leq Z_L \leq 2.25\ k\Omega$ with acceptable accuracy[6].

In order to reduce the costs of the proposed setup without renouncing performance, the R&S® ZNL3 was selected amongst other choices. A calibration at the probes' tips was preferred among other choices to compensate for the their contribution to the measurement and to obtain the maximum measurement accuracy (in [6] the accuracy curves are valid for calibrated instruments). For this task, a calibration standard printed on the same PCB to be tested was used, in order to make sure that no effect originated from a change in substrate properties when measuring the DUT. The PCB selected for the tests presented in this paper was Picotest's VRTS (Voltage Regulator Test Standard) v3.0.

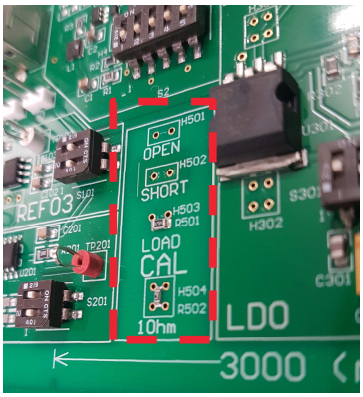

Figure 5 – Calibration standard on Picotest's VRTSv3.0

VI. 2-PORTS SHUNT TRANSMISSION TEST SETUP WITH 10:1 PROBES

Even though no correction data for the calibration standard on the PCB was available, assuming it to be ideal provided sufficient precision for measurements at low frequency. This was proven thanks to a benchmark on the R&S® ZNL3. A high-quality baseline was obtained by using the TOSM calibration (through-open-short-match) technique and the mechanical high-end R&S® ZV-Z235 calibration kit in combination with phase-stable R&S® ZV-Z193 cables. With this setup, the transmission (S_{21}) between the ports J6 and J7 of the board was measured (green curve in the following figure).

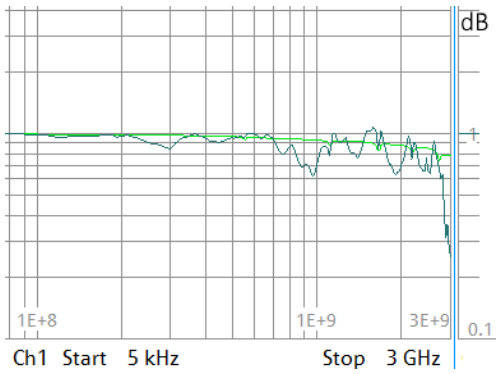

Figure 6 - Transmission calibration plausibility (picture cropped for better visualization). Deviations from the baseline are in the 0.1 dB order up to 800 MHz

The results were compared with those (blue curve in the following figure) obtained by probing J6 and J7 terminals' soldered surfaces with two R&S® RT-ZZ80 (10:1 probes), after having calibrated them with the VRTS v3.0 coupon by using the "one-path two-

[5] *The nomenclature is different amongst VNAs, and "load" can be found as an equivalent to "match".*
[6] *A high-Z probe has the advantage not to change the analyzed circuit's impedance, since the current that flows into the probe is negligible. On the other hand, the mismatch between test port and probe lowers the signal levels at the VNA input.*

ports" technique[7] and selecting the correction data for an ideal 3.5mm (male) calibration kit.
In this case, the deviations from the green pattern above 700-800 MHz (for example 0.3 dB at 1 GHz) were not only caused by the correction data being based on ideal calibration standards, but also from uncertainties due to the probes' tips parasitic at higher frequencies, and their positioning variation between calibration and measurement. In order to minimize the last effect, two R&S® RT-ZAP positioners were used to hold the R&S® RT-ZZ80 firmly in place. Finally, some phase-instability of the probes' cables might have affected the calibration and the measurement too.

Figure 7 – R&S® RT-ZZ80 probe with the selected tips for the measurement

The R&S® ZNL3 was set to 10 Hz inter-frequency bandwidth (IFBW) and -10 dBm output power. According to the instrument datasheet [6], this delivered from 5 kHz to 800 MHz a typical 110 dB to 130 dB dynamic range, thus ensuring a minimal noise floor.

Finally, the output impedance of a low-dropout regulator (LDO) on Picotest's VRTS v3.0 board was measured.
For this measurement, very low uncertainty could be obtained for the whole curve (see appendix).

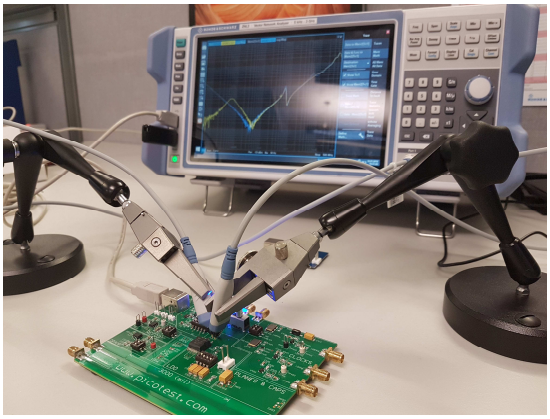

Figure 8 – Shunt transmission measurement setup. Two R&S® RT-ZAP hold the R&S® RT-ZZ80 probes connected to the PCB terminals

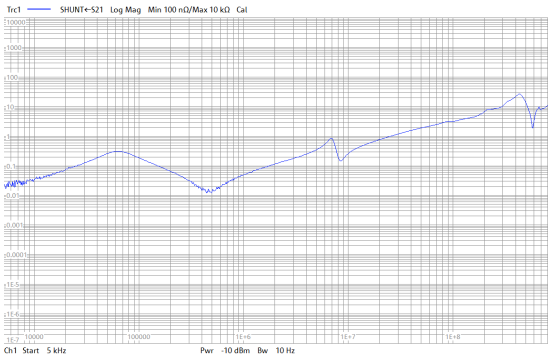

Figure 9 – LDO (powered on) output impedance between 5 kHz and 800 MHz. The noise around 10 mΩ can be reduced with the use of a higher power output

Notice that in the setup above the "probe tip impedance" value was not set, because even though *m* in equation (13) has a physical meaning, the calibration post-processing correction always uses 50Ω as a reference at the calibration plane, and does not need any "probe tip impedance" input when the calibration is executed at the probe tip.

VII. COMPARISON OF 2-PORT SHUNT TRANSMISSION AND 1-PORT REFLECTION IMPEDANCE TEST SETUP

Similarly to the previous paragraph, a calibration plausibility test was made for a 1-port impedance measurement. Port J6 was closed with a 50 Ω match and a 100 Hz IFBW was selected. The chosen calibration technique was OSM (open-short-match), and the probe that was tested against the high-quality baseline was Picotest's P2100A 1:1 probe, which was held in place by the stand supplied with it. In this case, the probe provided a trustworthy performance up to 200 MHz.

Finally, the output impedance of a point-of-load converter (POL) on Picotest's VRTS v3.0 board was measured.

The uncertainty of most of the displayed curve for this particular measurement was higher than 10% (see appendix). Therefore, this test setup is not appropriate for the entire impedance range of the measured DUT over the whole frequency range, and the 2-port shunt transmission setup should be preferred instead.

[7] *For the "Through" calibration step, the probes' tips were shorted through the "Short" terminals of the calibration coupon, while the probes' grounding-tips were manually connected without using any terminal.*

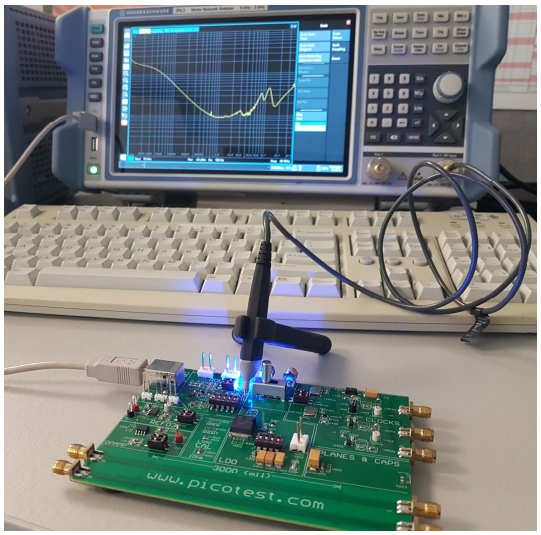

Figure 10 – Measurement setup for the 1-port impedance measurement

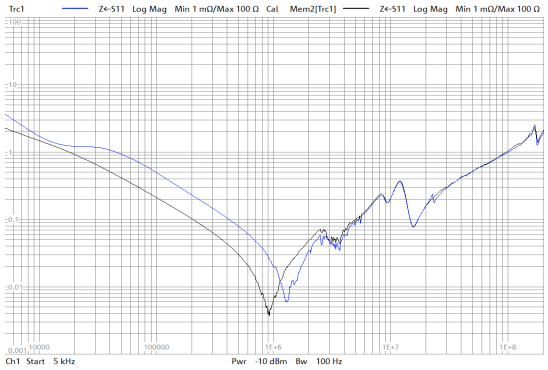

Figure 11 – POL (black trace: powered off – blue trace: powered on) output impedance between 5 kHz and 200 MHz. The noise below 100 mΩ was mitigated through the use of averaging

VIII. CONCLUSION

Different ways to measure the impedance of a DUT were described in theory and practice. All of them can be used to test a PDN, but each one's pros and cons should be kept in mind because of their influence on the results. 1-port impedance measurements are faster because they do not require longer calibration procedures, but are also noisier at low impedances.

2-port shunt setups provide sufficient precision to for a broader range of impedances (here extended thanks to 10:1 probes) even starting from below 1 mΩ, but are more complicated to set up. Precise and repeatable measurements can be easily performed within bands up to several hundreds of megahertz by using an ideal calibration, and repurposing the R&S® RT-ZZ80 probes (originally designed for oscilloscopes) in order to contain the test setup costs.

Measurements in higher frequencies require a more precise calibration correction along with probes designed for radio-frequency testing with VNAs.

The selection of a R&S® ZNL proven to be an outstanding cost-efficient solution to address PDN impedance testing. Its low measurement uncertainty is ultimately very important to obtain sufficient accuracy: the mathematical fundamentals for this are explained in the appendix to this paper.

References

[1] Nagi, Manas, "Global Printed Circuit Board (PCB) Market to Witness a CAGR of 3.1% during 2018-2024" Energias Market Research, July 2018, *https://globenewswire.com/news-release/2018/07/30/1543947/0/en/Global-Printed-Circuit-Board-PCB-Market-to-Witness-a-CAGR-of-3-1-during-2018-2024.html* (requested March 15, 2019)

[2] Bogatin, Eric "Signal and Power Integrity - Simplified", Prentice Hall, 2010.

[3] Hiebel, Michael "Fundamental of Vector Network Analysis", Rohde & Schwarz, 2016.

[4] Sandler, Steven M. "Extending the usable range of the 2-port shunt through impedance measurement", IEEE MTT-S Latin America Microwave Conference (LAMC), 2016.

[5] Limjoco, Aldrick S. "Understanding Switching Regulator Output Artifacts Expedites Power Supply Design", Analog Dialogue 48-08, 2014

[6] Rohde & Schwarz "R&S®ZNL Vector Network Analyzer – Datasheet V03.00", November 2017, *https://www.rohde-schwarz.com/broschuere-datenblatt/znl/* (requested March 15, 2019)

[7] Sandler, Steven M. „ Power Integrity - Measuring, Optimizing and Troubleshooting Power Systems", McGraw-Hill Education Ltd., 2014.