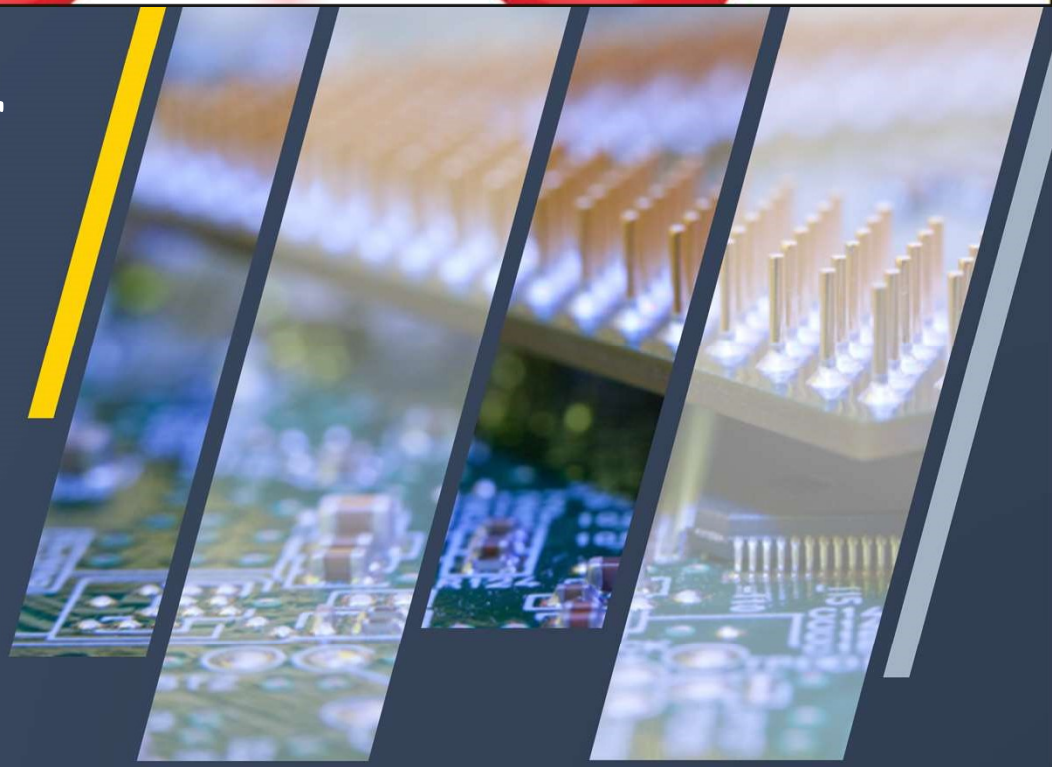
ANSYS®

EDI CON 2019
Electronic Design Innovation Conference
电子设计创新大会

April 1-3, 2019
China National Convention Center
Beijing, China

Exhibition Hours
April 1: 11:00-17:00
April 2: 9:30-17:00
April 3: 9:30-13:00

Modeling and probing for accurate PDN impedance measurements in sub-kilohertz range



Presenter:

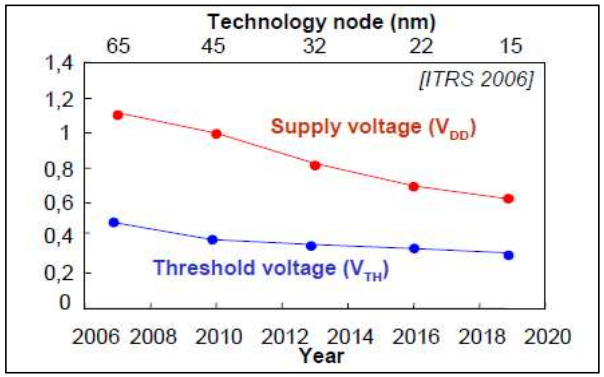
Abstract

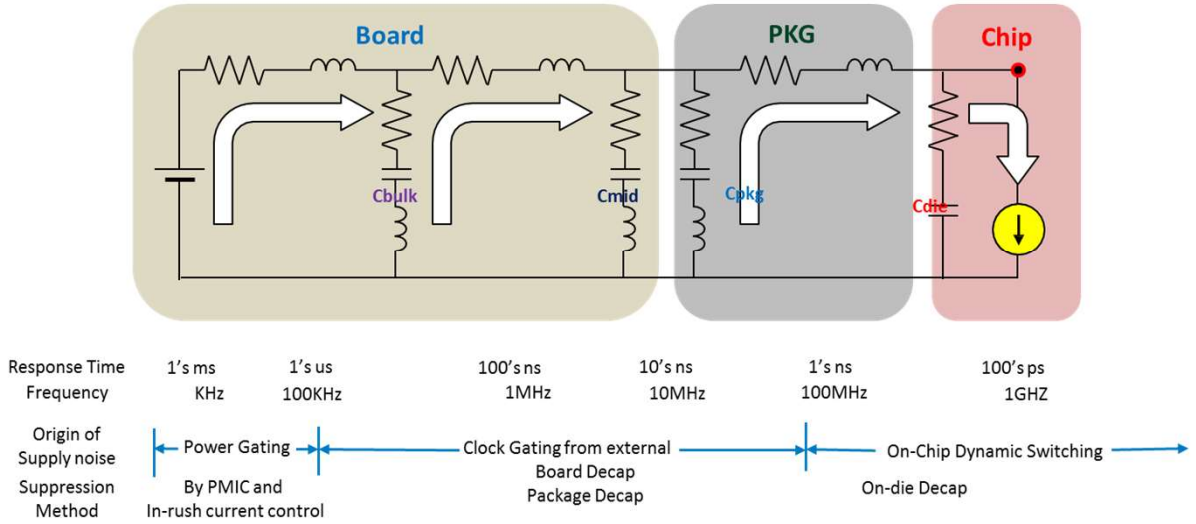
- Why sub-kilohertz
- Challenges of sub-kilohertz analysis accuracy
- Simple case study
- Real case
- measurement correlation
- Conclusion

Why sub-kilohertz

- Power Integrity compassing overall frequency
  - Sub-kilohertz power impedance is dominated by Voltage Regular Model, while PCB/PKG structure also influence it.

- When low power supply goes lower, but total current volume is till high, that means it requires low power impedance for BOTH VRM and PDN.

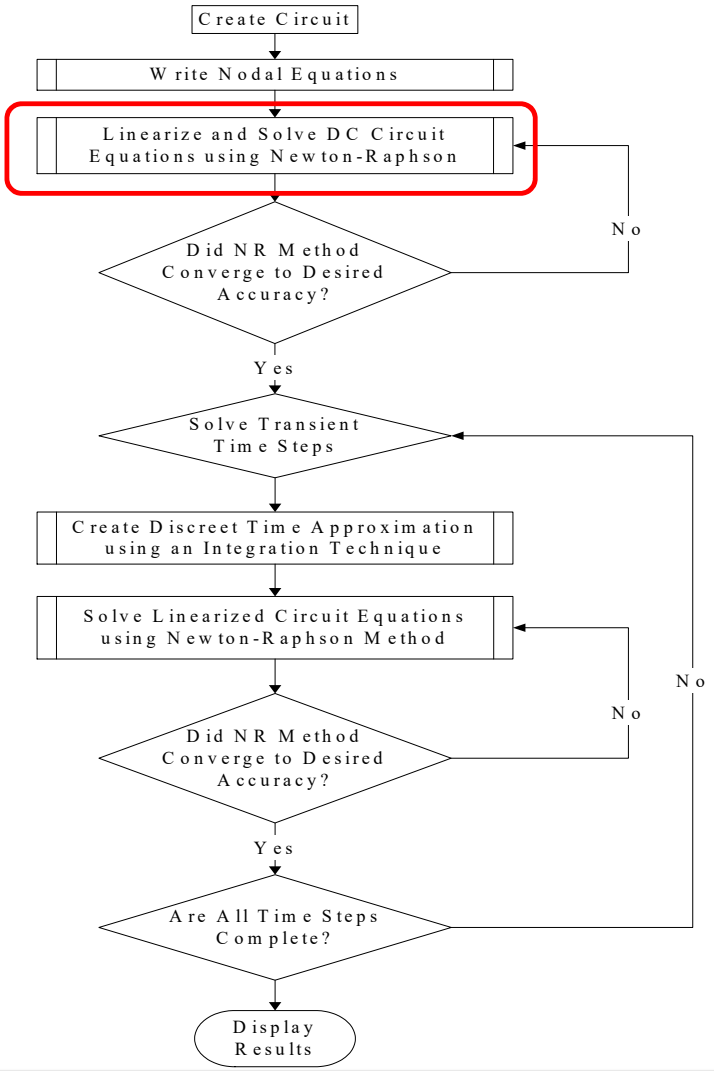




Why sub-kilohertz (count.)

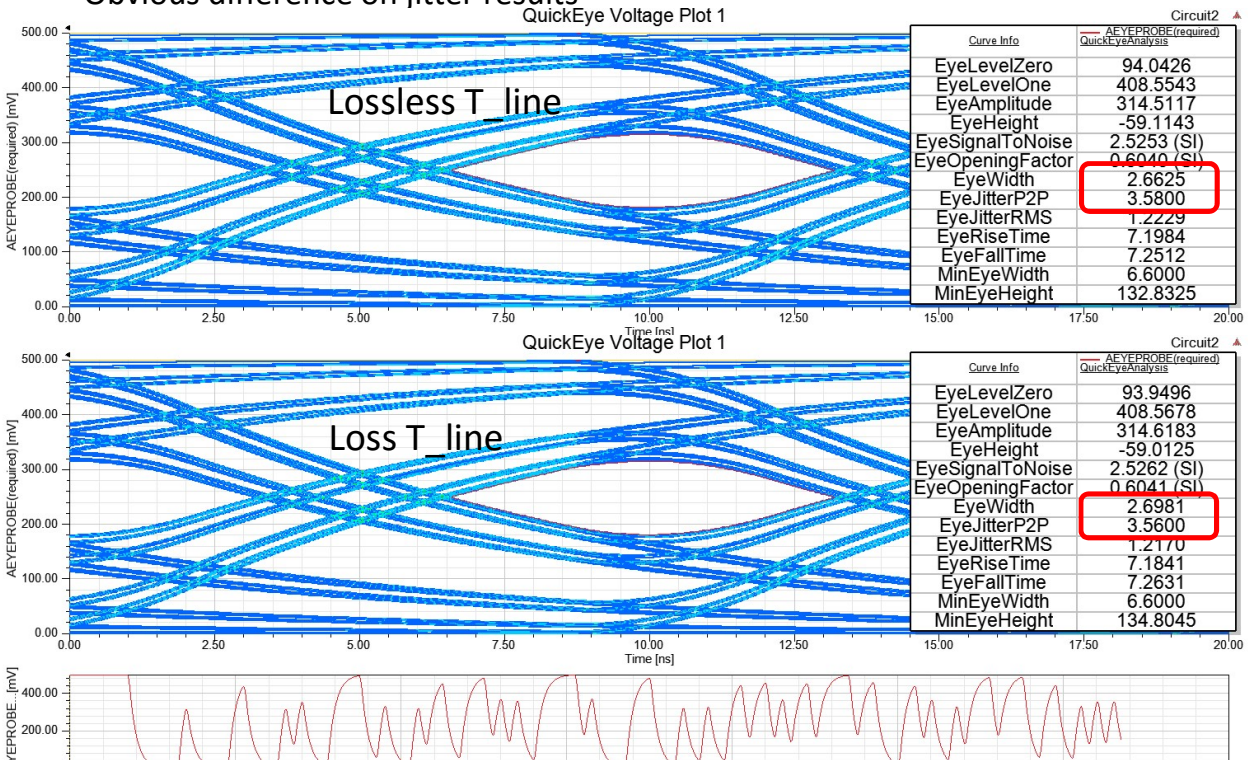
- In Timing domain simulation, first step is to Solve DC Circuit Equations.
  - DC's shift will affect transient voltage absolute value, subsequentially eye jitter.

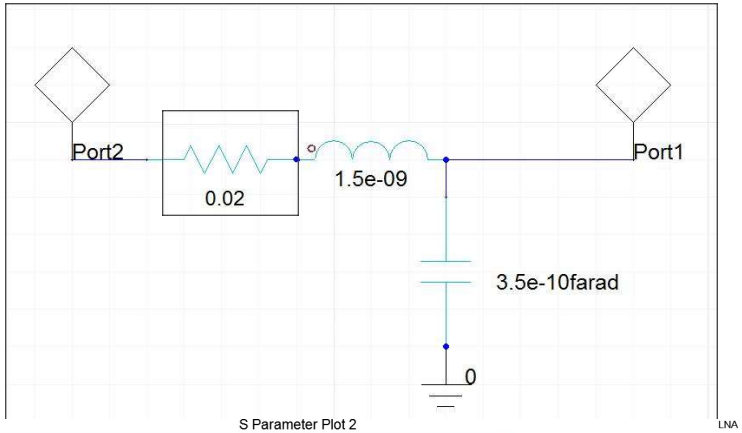
- While S parameter or full wave spice(or broad band spice) doesn't have real DC point, the DC and low frequency points are extrapolated.

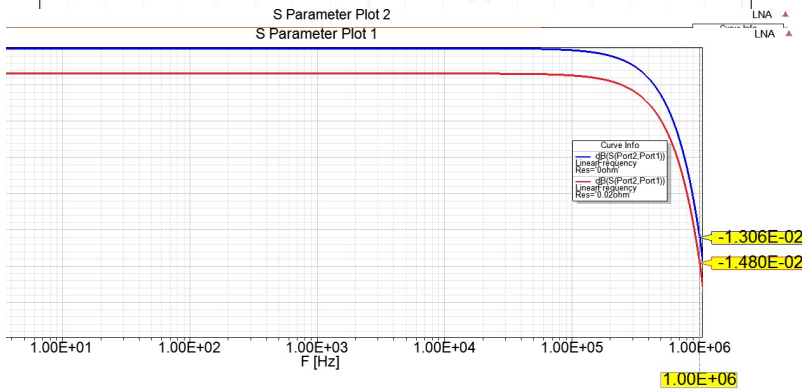


Example

- Lossless T_line Model vs. loss T_line model
  - Significant difference below 1MHz, almost same on high frequency.
- Test the two T-line models on transient analysis
  - 1Gbps, 300psTr/Tf PRBS
  - Obvious difference on jitter results







Challenges of sub-kilohertz analysis accuracy: Governed by different laws

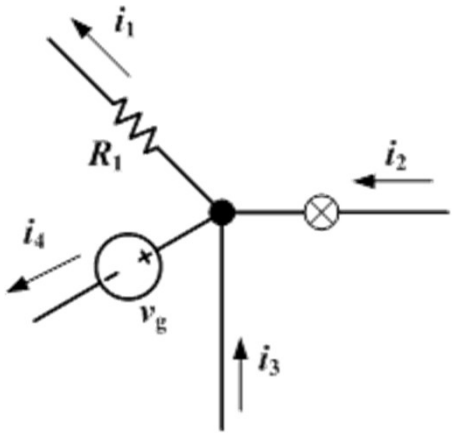
- Maxwell equation doesn't cover DC

$$\nabla \times E = -\frac{\partial B}{\partial t}$$
$$\nabla \times H = J + \frac{\partial D}{\partial t}$$
$$\nabla \cdot D = \rho$$
$$\nabla \cdot B = 0$$

- DC problem was solved by Kirchhoff's current law

$$KCL: i_1 + i_4 = i_2 + i_3$$

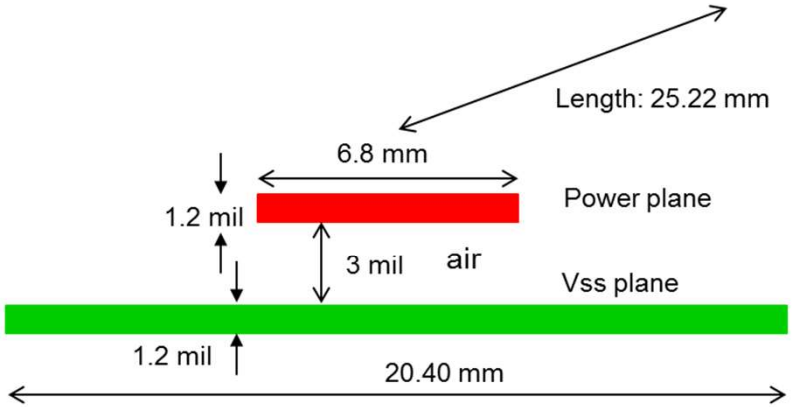
$$KVL: v_4 = v_1 + v_2 + v_3$$



Simple case study

- Simple microstrip line
- Calculate DC resistance and inductance, 1Hz resistance inductance, 1KHz resistance, inductance, 1MHz resistance and inductance, 100MHz resistance and inductance.
- Tools to be used
  - Q2D: 2D FEM analysis tools
  - Q3D: 3D FEM for DC, 3D MoM for AC
  - HFSS: 3D FEM for AC

Ground plane is 3X of power plane. Power plane is centered.

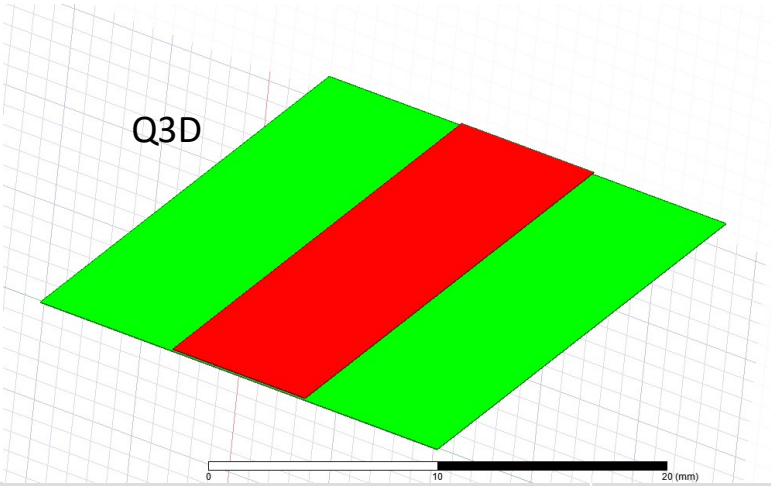


Conductivity	4.60E+07
ε_r	1.0
μ_r	1.0

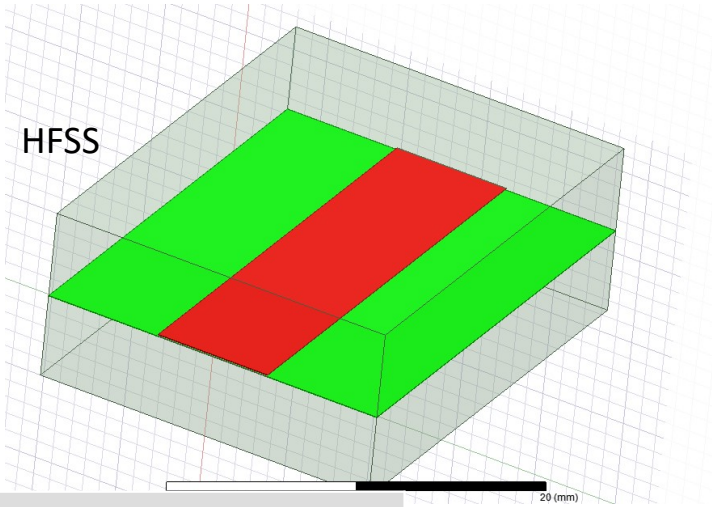
Models and initial results

Q2D

Q3D



HFSS

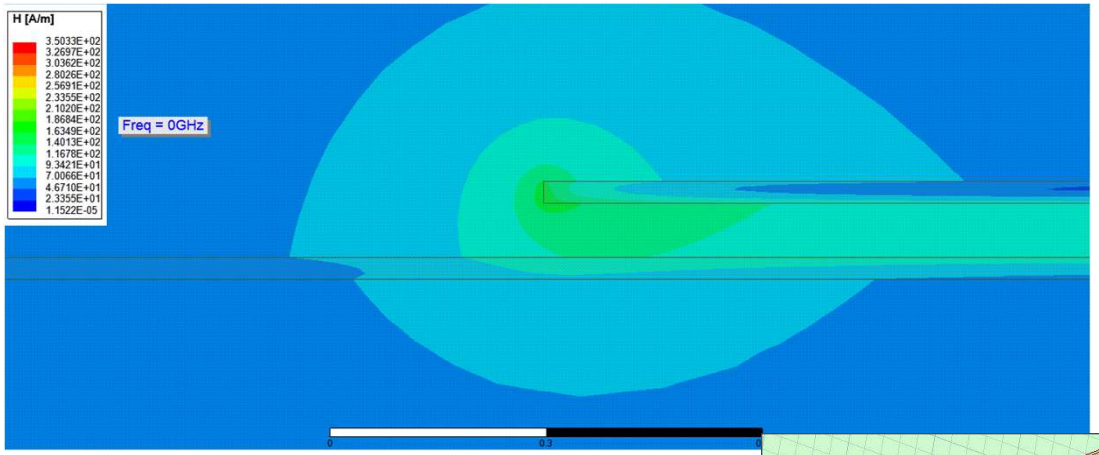


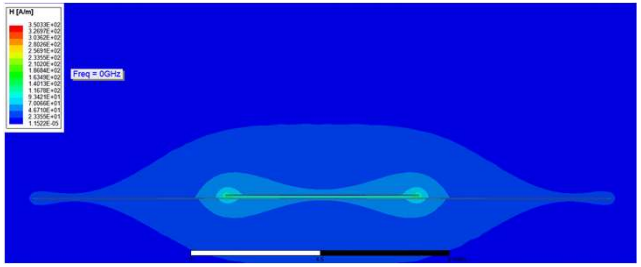
	Resistance (mohm)			Inductance (nL)		
	Q2D	Q3D	HFSS	Q2D	Q3D	HFSS
DC	3.53	6.8		3.91	3.66	
1Hz	3.53	6.8	3.83	3.91	3.66	3.926
1KHz	3.53	6.8	3.83	3.91	3.66	4.207
1MHz	5.05	8.44	5.05	0.448	0.705	0.439
1GHz	63.8	65.309	61.796	0.348	0.397	0.364

Question: Why Q3D DC R/L are off with Q2D and HFSS?

Close look the model

- **Return path**
  - DC current distributed broader than AC.



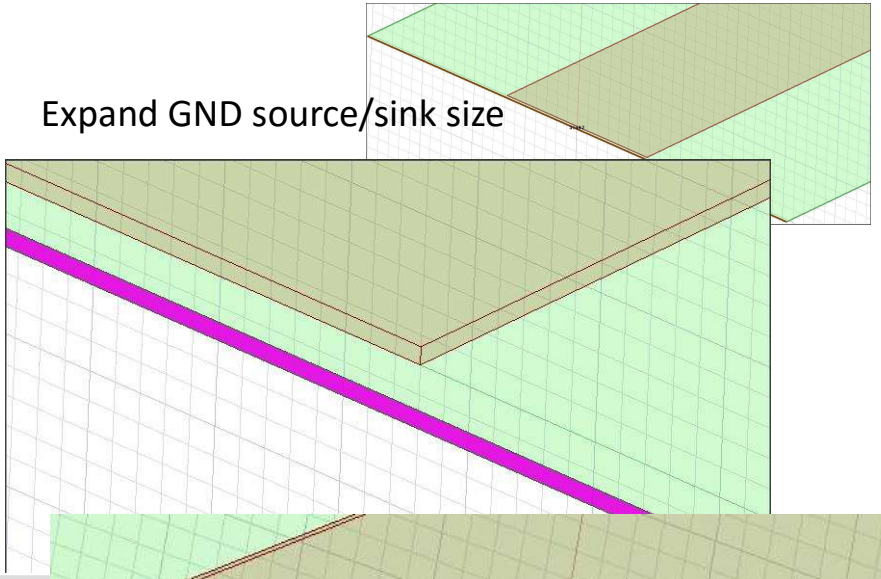


- How Q3D calculate return path
  - The GND sink size is as same as trace width
  - This caused low frequency R/L bigger.

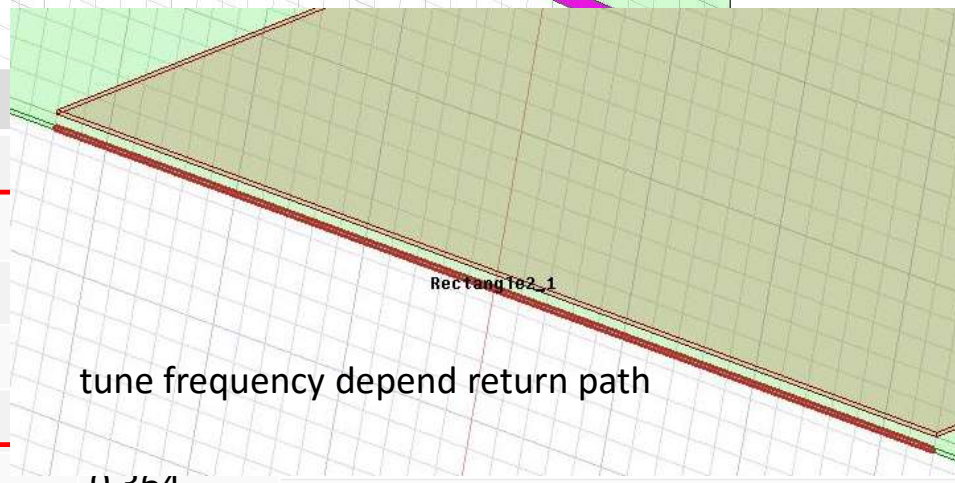
Revised return path model

	Res (mohm)		Ind (nH)	
	Q2D	Q3D	Q2D	Q3D
DC	3.53	3.55	3.91	3.66
1Hz	3.53	3.55	3.91	3.66
1KHz	3.53	3.55	3.91	3.66
1MHz	5.05	5.16	0.448	0.643
1GHz	63.8	65.309	0.348	0.397

Expand GND source/sink size



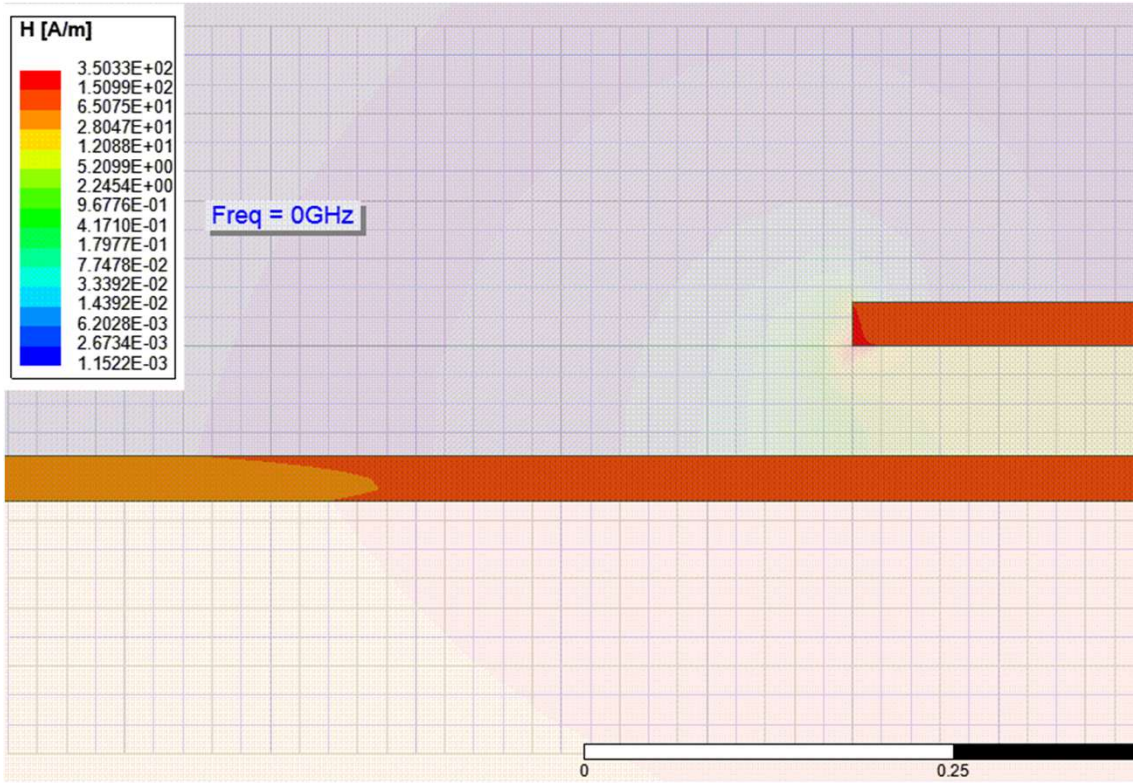
	Resistance (mohm)			Inductance (nL)		
	Q2D	Q3D	HFSS	Q2D	Q3D	
DC	3.53	6.8		3.91	3.66	
1Hz	3.53	6.8	3.83	3.91	3.66	
1KHz	3.53	6.8	3.83	3.91	3.66	
1MHz	5.05	8.44	5.05	0.448	0.705	
1GHz	63.8	65.309	61.796	0.348	0.397	0.364



tune frequency depend return path

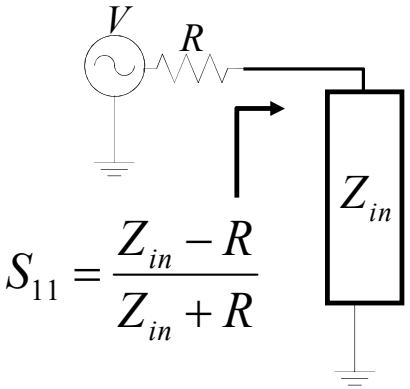
Closer look

- **Skin effect:** when frequency goes high, current will compress on metal's surface
  - increase resistance and decrease inductance value.
- Most electromagnetic high frequency simulation software mesh (solve) metal's surface field only, this may cause DC&low frequency range R/L inaccurate.
  - Q2D mesh everything
  - Q3D DC solver volume mesh metal, AC solver surface mesh metal.
  - HFSS surface mesh metal by default, integrate Q3D DC solver to guarantee DC& low freq's accuracy.



What else?

- **Port Impedance**
  - How T-line S parameter convert to r/L/C?



$$Zin = \frac{1 - S11}{1 + S11} R$$

$$Zin = \underline{r} + jw(\underline{L}/\underline{C})$$

	50ohm Port	0.1ohm Port
1Hz	3.725	3.84
1KHz	3.83	3.824
1MHz	5.05	9.1
1GHz	61.796	72.5

  - Typical T-line magnitude of S11 at sub kilohertz is very small, subsequentially higher numerical calculation error happens when port impedance are very off with DUT.

Rule of Thumb: set port impedance closer to DUT's impedance to reduce the numeric error

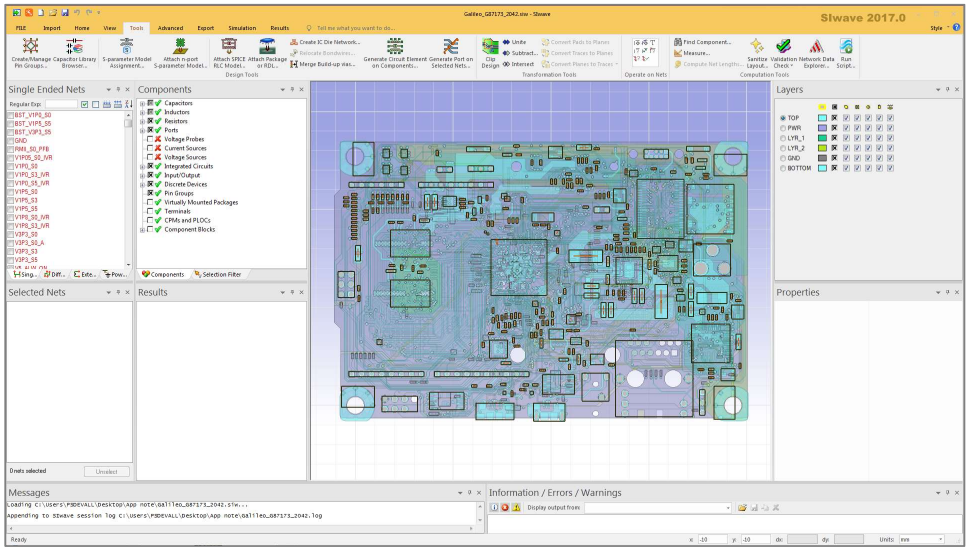
New hybrid solver approach

- **SIwave**
  - **Hybrid EM Field Solver** [FEM Based]
  - Models Printed Circuit Boards and Packages
  - Analyses Performed
    - *DC Analysis (with Thermal coupling)*
    - *Signal Integrity*
    - *Power Integrity*

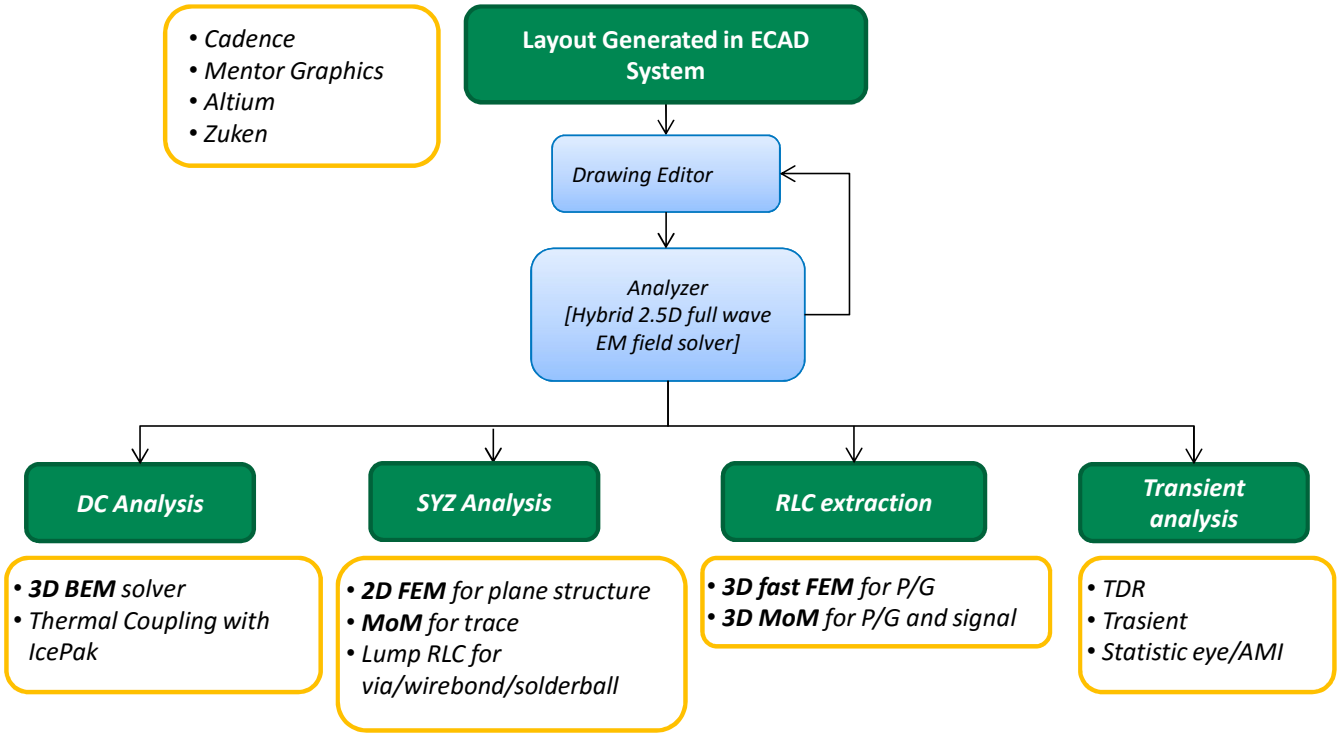
    } ***Frequency and Time domain***

    - *Electromagnetic Compatibility/Interference*

SIwave Objective:
Generate Virtual Laboratory Data Set from ECAD for Prototype Design with Fast and Accurate Electromagnetic Simulations

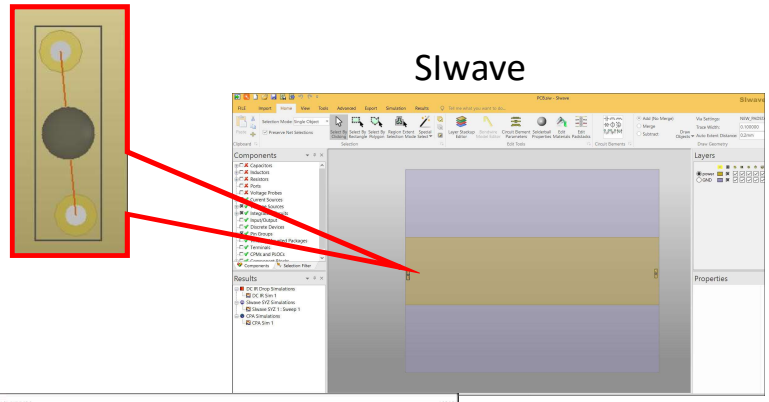


SIwave hybrid solver in detail

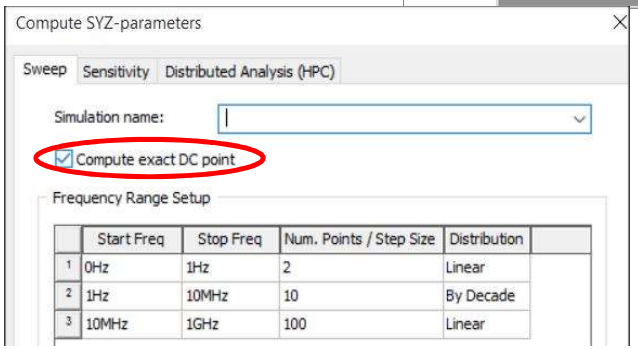


How does hybrid solver overcomes problems

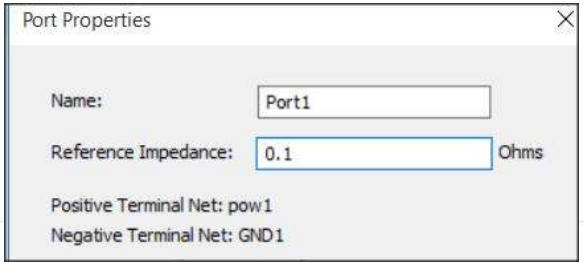
- **Return path**
  - Both AC and DC current will return by component pin



- **Skin effect**
  - True DC solver and AC solver will interpolate sun kiloherhz frequency range skin depth caused loss

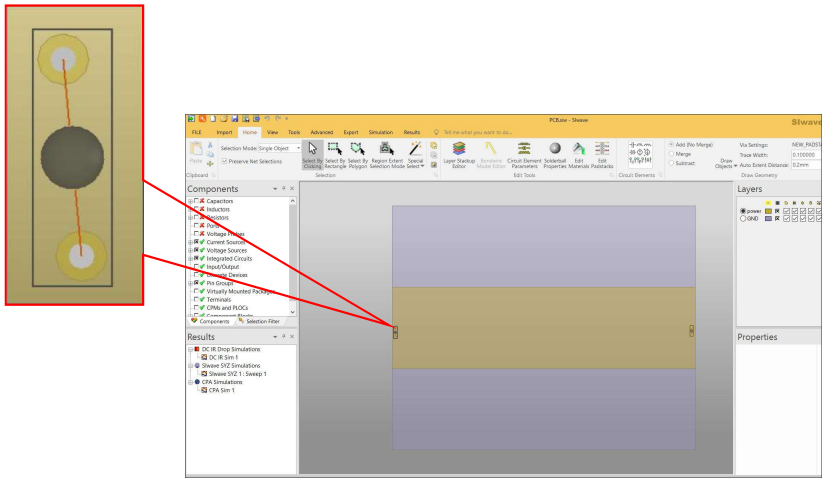


- **Port Impedance**
  - Tune port impedance closer to DUT



SIwave hybrid solver results

	SIwave DC	SIwave SYZ @1Hz	SIwave CPA @1Hz	Q3D DC
Resistance (mohm)	6.311	6.548	6.381	6.8



	SIwave SYZ Resistance (mohm)	Q3D Resistance (mohm)
DC	6.311	6.381
1Hz	6.311	6.381
1KHz	6.311	6.381
1MHz	7.114	9.475
1GHz	9.41	13.75

SIwave hybrid solver shows consistent DC and sub kilohertz's accuracy with Q3D.

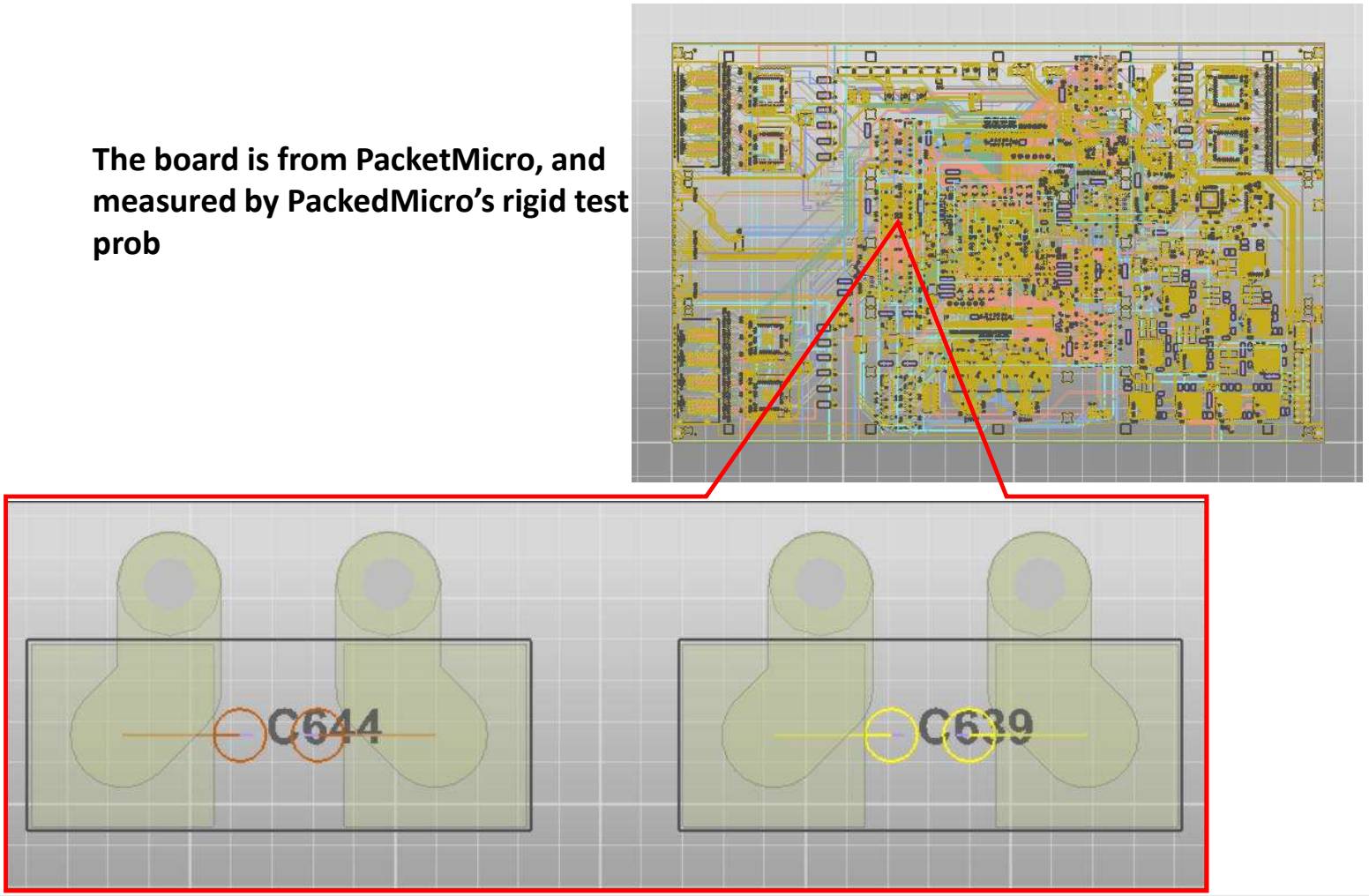
Real case study

- 22 layers PCB

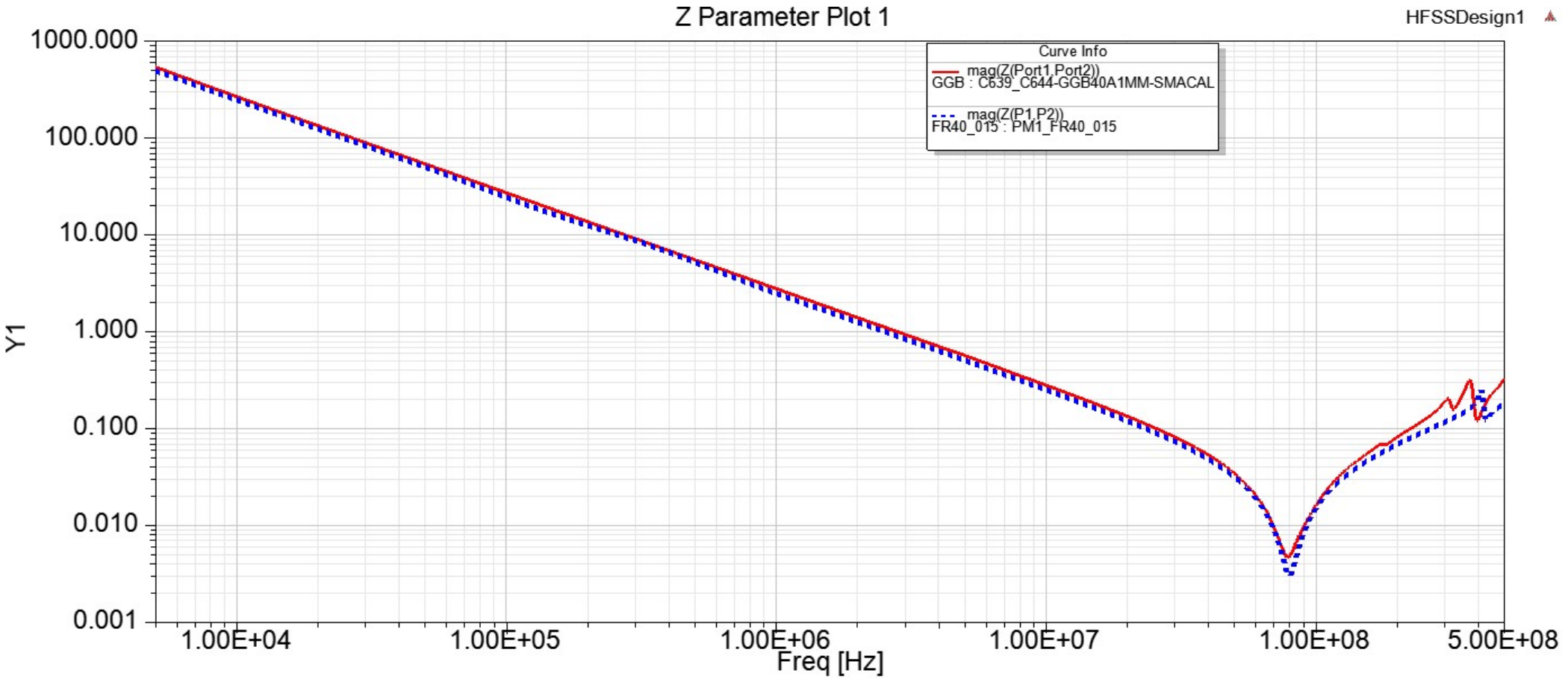
- Target nets
  - 0.9V PWR
  - GND

- Prob point

The board is from PacketMicro, and measured by PackedMicro's rigid test prob



Simulation versus. Measurement



SIwave result matched well with VNA test results from 5KHz to 5MHz.

conclusion

- DC and sub kilohertz accurate is critical for SI/PI analysis.
- Sub kilohertz PCB and package parasitics simulation are sensitive of **return path, skin depth** calculation and **port impedance** setting.
- SIwave hybrid solver shows solid PCB/package extraction accuracy from DC up to GHz.
- Simulation and measurement correlation proves the hybrid solvers accuracy.

Thanks PacketMicro Richard Zai (rzai@packetmicro.com)to supply test PCB and VNA measurement results!
https://www.packetmicro.com/

