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Advances in Recent PCB Design Verification Flows

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EM in Microwave Office: Design and Verification Flows

- Design Flow: EM is used while making the circuit.
  - Checking a model's accuracy: e.g. – a wide output line on a power amplifier.
  - A model doesn't exist: e.g. – An octagonal spiral inductor.
  - Coupling between parts of the circuit: e.g. – lines coupling to a distributed filter.
  - The completed circuit is sent out to external tools for manufacturing and other layout.
  - MWO has nice technology for this flow: e.g. – Extraction, parameter based layout, shape simplification rules, PDK cells, hierarchical layout.
- Verification Flow: A layout is brought into Microwave Office to simulate in EM.
  - Checking a completed layout to see if any signal integrity issues: e.g. – sufficient grounding or radiation.
  - The finished layout might be very complicated: e.g. - multiple power planes, traces.
  - The EM simulator, AXIEM, is setup: e.g. – port type and location.
  - The layout is meshed and simulated.

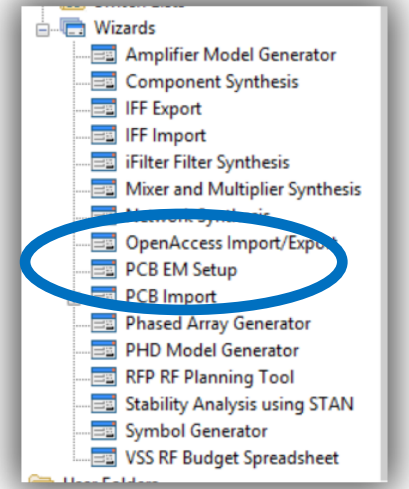
V14 – EM Verification Flow Requirements

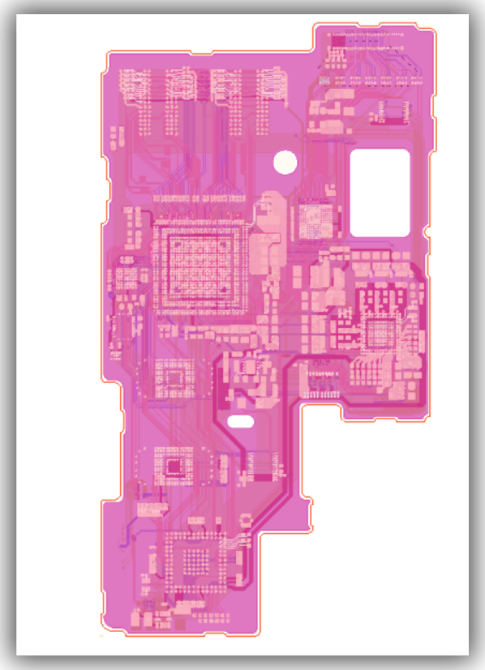
- Must work well for commercially complicated board topologies.
  - Hundreds of nets.
  - Multiple power planes connected by many vias.
  - Dozens of surface mount parts.
- Must work with commercial layout tools.
  - Cadence Allegro, Zuken, Mentor Graphics, Altium.
- Should have knowledge of board stackup, and material properties.
- Ability to select nets and surrounding layout easily.
- Ability to simplify layout as needed to get reasonable mesh.
- Ability to easily have ports added.

What We Did in V14

- ODB++ and IPC-2581 layout languages based. (Had some of this V13.)
  - Supported by all commercial tools.
  - Have a lot information besides the layout: nets, materials, and board stackup.
- Imports directly into Microwave Office (V13 – had to go through a third party tool.)
- Controlled with a PCB Import Wizard
  - Tabular display and control of nets, layers, and materials.
  - STACKUP block is automatically created for EM simulation.
- Nets can be identified easily and layout simplified as needed.
- Ports (pin ports) are automatically added at selected nets.
- Net selection understands surface mount part gaps, and more complicated multiple connected parts.
- S-parameter block in schematic has layout-like symbol and appropriate net names.

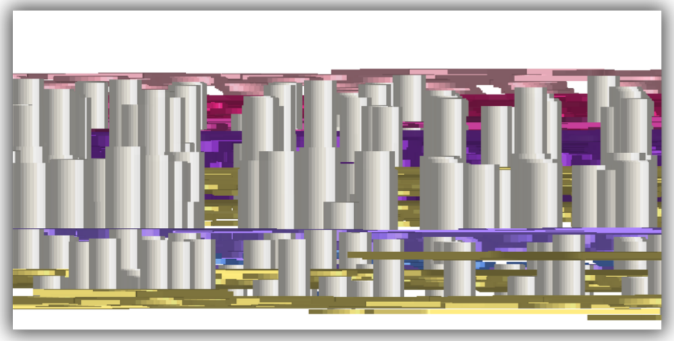
An Example – A Board Made in Zuken





Imported Board

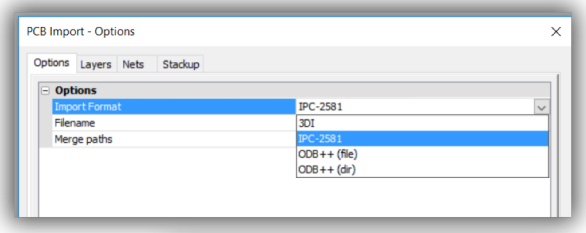
- Imported as IPC 2581
- 11 layer FR4 Board
- 10 conducting layers
- 14 via types



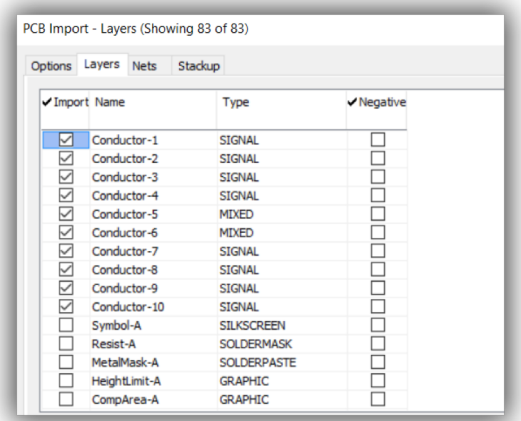
Close-up 3D View of Vias

The Import Wizard

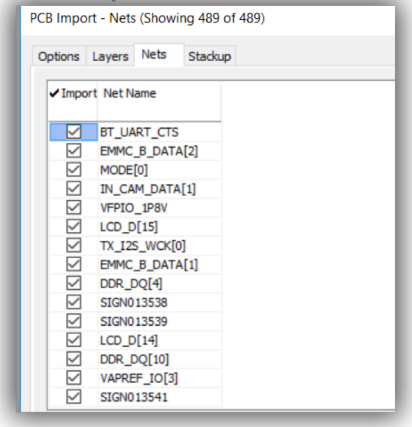
Select Import Format



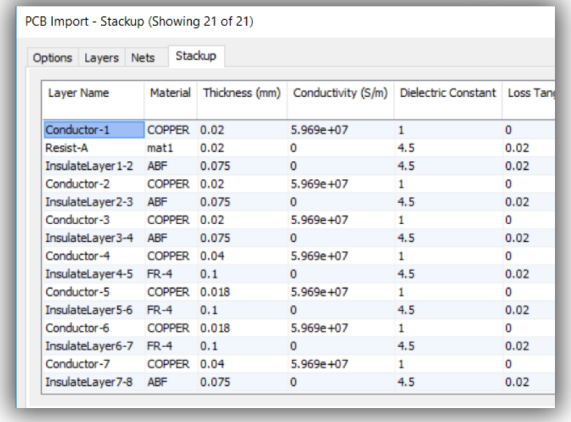
The Layers Imported



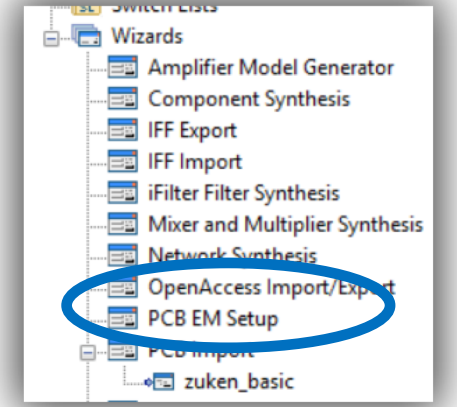
Nets Imported

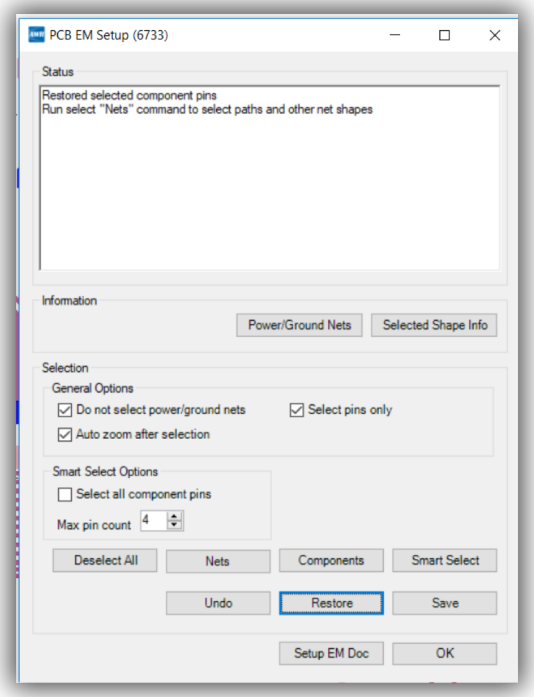


Stackup Creation



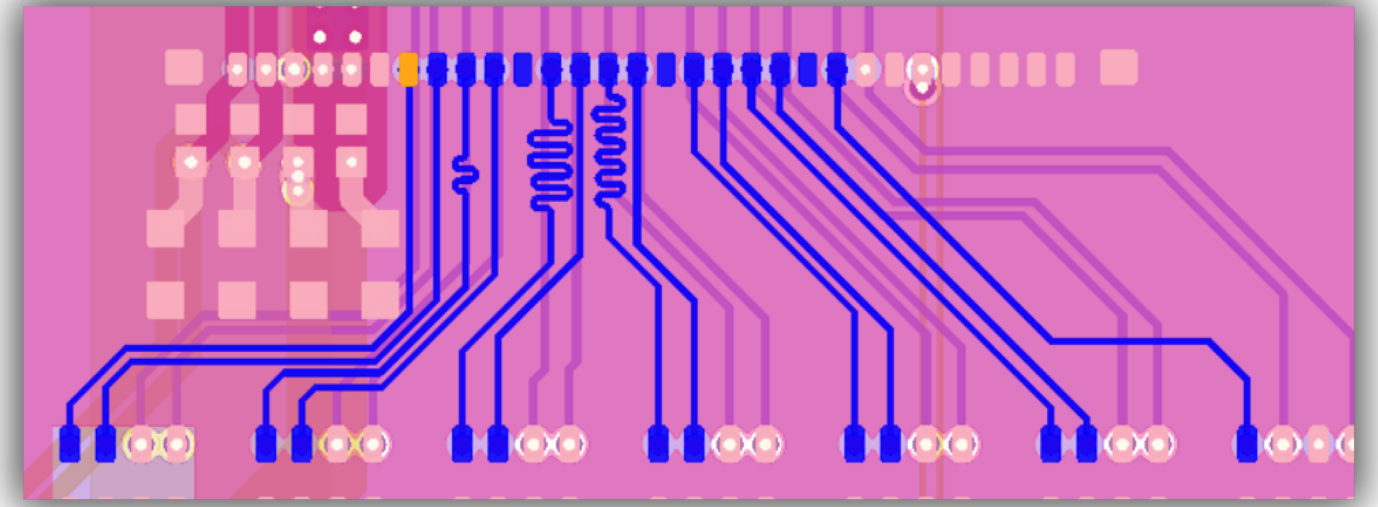
The EM Setup Wizard



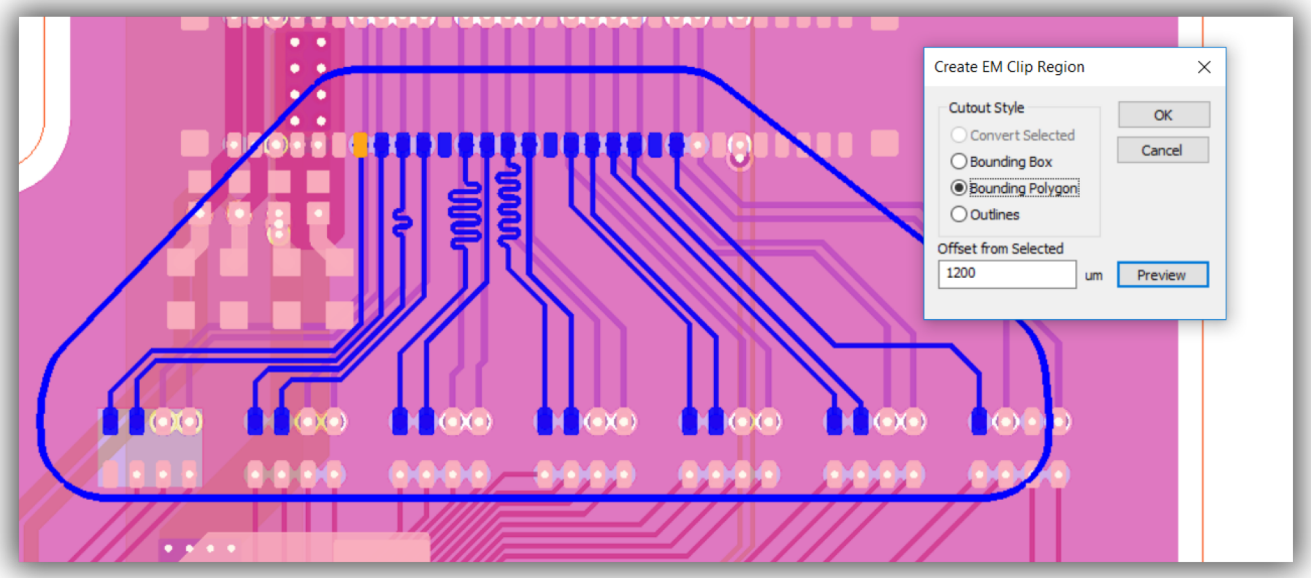


- Normally – we select the pins we want.
- Smart Select – selects net attached to pin.
- Can select other pins on component with Smart Select.
- Can propagate through series component.

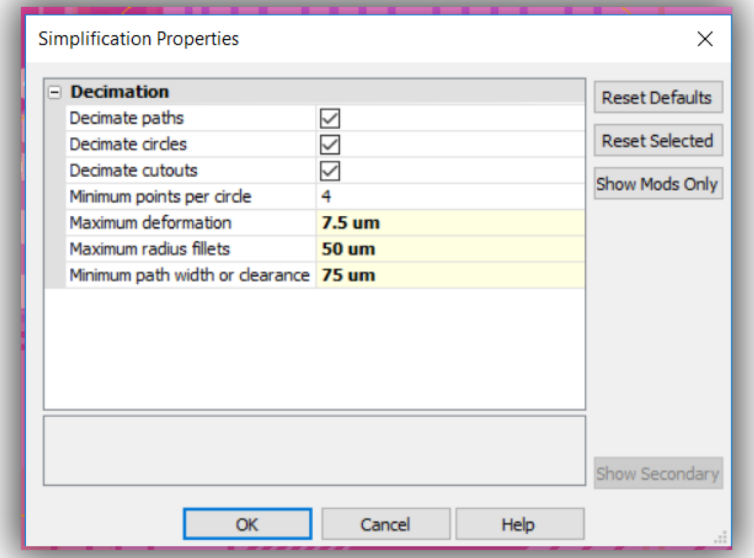
The Selected Pins and Nets



Create the Boundary for the Region for EM

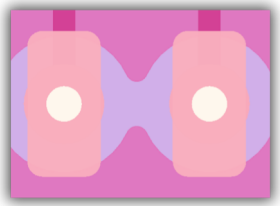


Shape Simplification



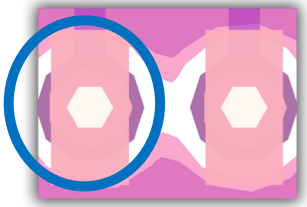
Before

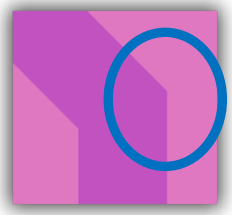
Vias



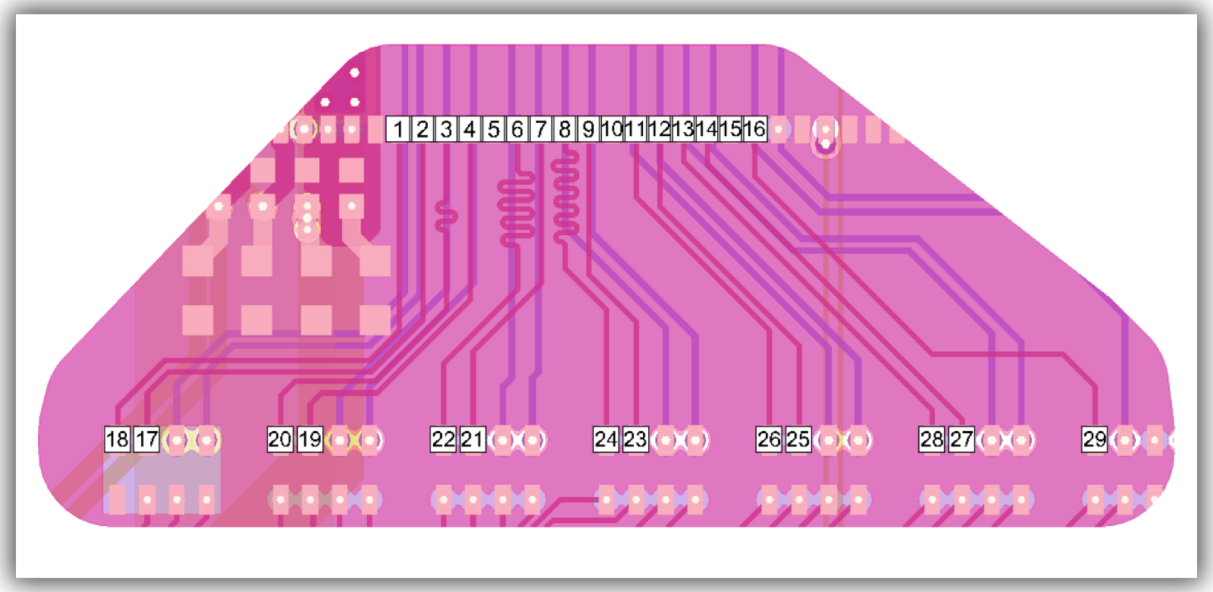
Bends

After





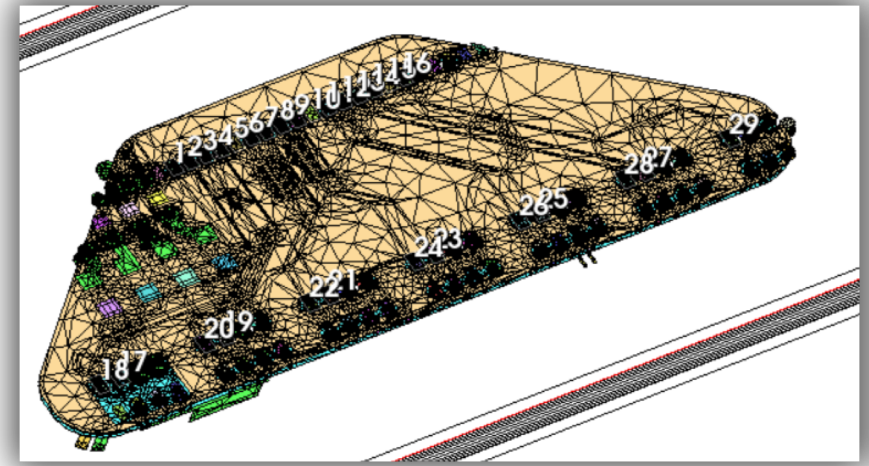
Ports Have Been Added Automatically



These ports are called Pin Ports

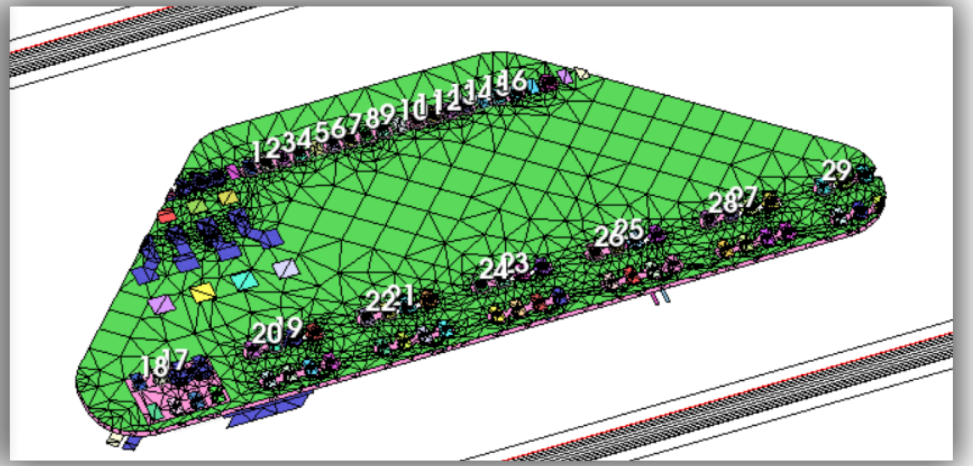
Improved Meshing in AXIEM

V13 Mesh



81K Unknowns

V14 Mesh

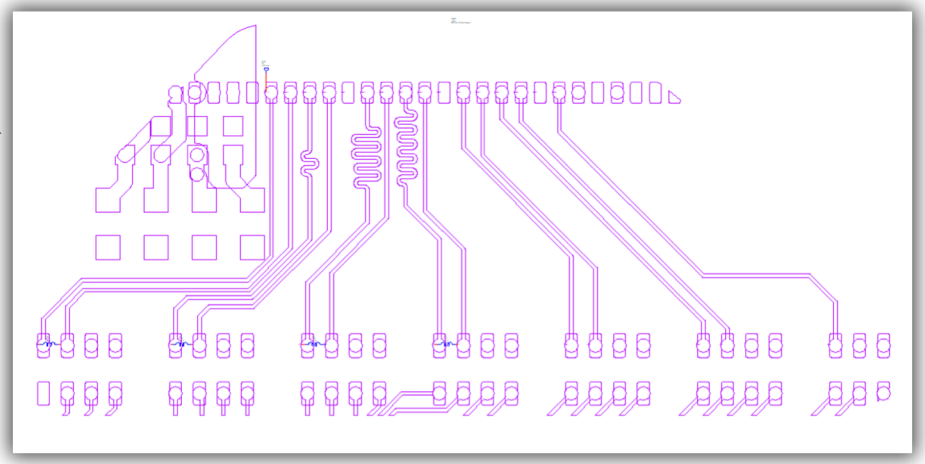


22K Unknowns

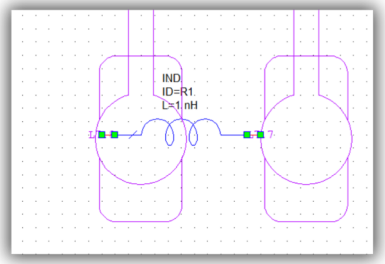
Meshing – Why is it Better

- We have fewer meshes.
  - Faster to simulate
  - Solve time for iterative solver is N^1.6.
- They are more square and equilateral triangles – fewer slivers.
  - Better conditioned matrix – easier to solve iteratively.
- We don't mirror the mesh through planes.
- Shape simplification reduced rounded corners and circular vias.
- … and – we spent a lot of time working on mesh algorithms!

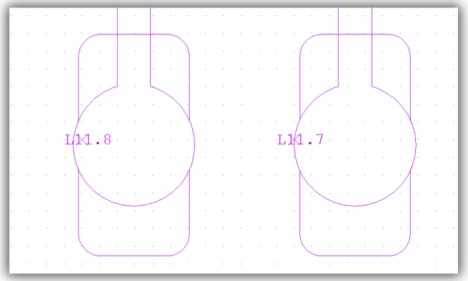
S-parameters Used in a Schematic



The sub-circuit block looks like the layout.



Easy to place elements.



The pin names are in the symbol.

Conclusions

- V14 has improved layout import for verification flow.
- It directly can read ODB++ and IPC-2581 layout files.
  - Layers, materials, pins and nets are included.
- It is controlled by a new PCB Import Wizard.
- A new EM Setup Wizard allows:
  - Selection of the desired pins and nets.
  - Creates a cutout region of the layout automatically.
  - Simplifies bends and vias.
- AXIEM has been improved:
  - Pin ports are automatically added without manual placement.
  - Meshing has been improved for board layout geometries.