EDI CON 2019
Electronic Design Innovation Conference
电子设计创新大会
April 1-3, 2019
China National Convention Center
Beijing, China

New and Upcoming Power Related Challenges

Instructor: Steve Sandler

Steve@Picotest.com

PICOTEST

Better Products Through Better Test

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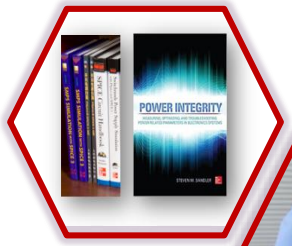
And Just a Bit About Steve

- 40+ Years Experience (1977-present)
- AEi Systems – Founder and CTO (1995-)
- Picotest – Founder and Managing Director (2010-)
- Test Engineer of the Year (2012-2014)
- Experience: Space Shuttle, Space Station, GPS, Large Hadron Collider and many other military and commercial projects
- Primarily focused on RF, Analog, and Distributed Power Systems

I enjoy writing



lab time

lecturing

making pizza

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Outline

Architecture → As power levels increase, the multi-phase buck solution loses steam. Newer topologies are being considered and that means new models and design techniques

Model Development → Manufacturers are sharing less component details, considering these "secret sauce". Much of the data that IS published is incorrect, meaning more measurement by the power designers

Measurement → In addition to the measurements needed for model creation, PDN impedance has fallen below 100μΩ creating new challenges and requiring new test adapters, cables and amplifiers

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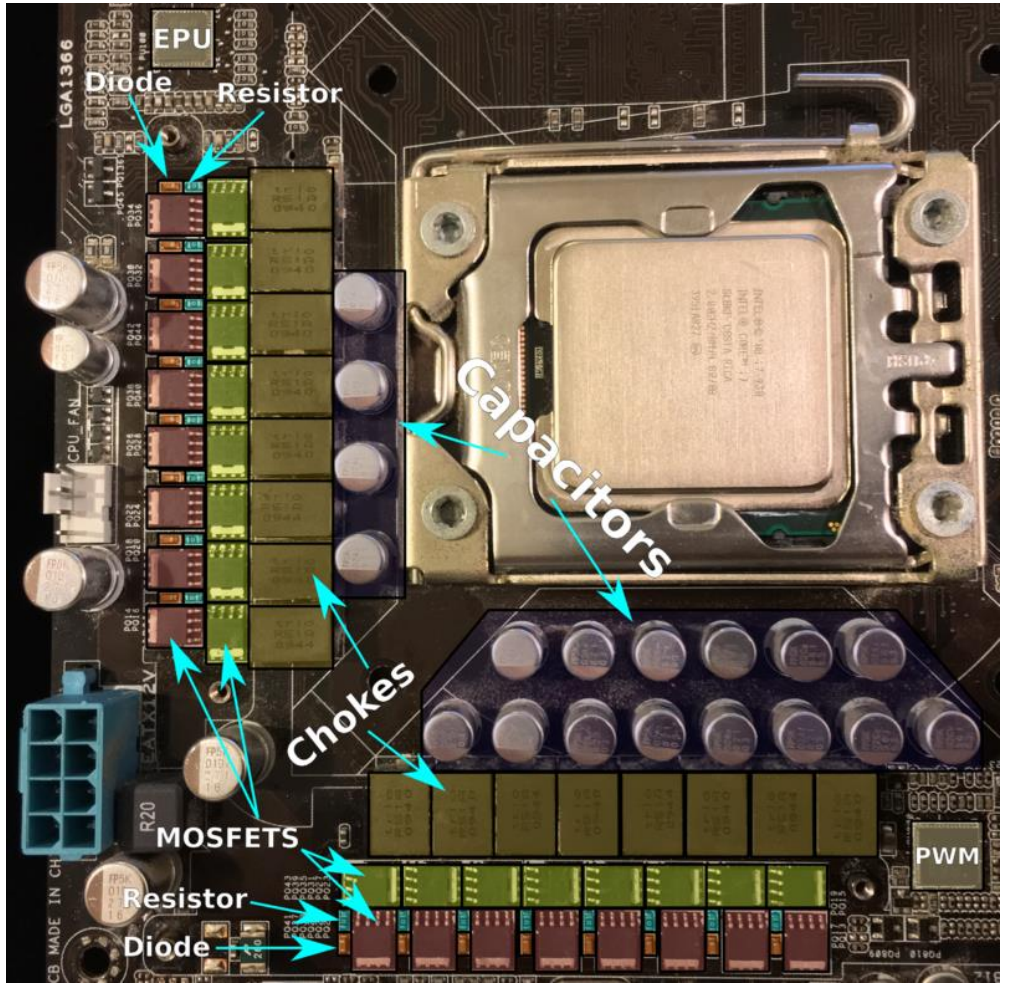
Power is On the Rise

In the portable market they are more highly integrated and more numerous than ever

In the higher power markets power rails are reaching 1,000 Amps requiring much of the available real estate, even at ≥ 1kW/in^3



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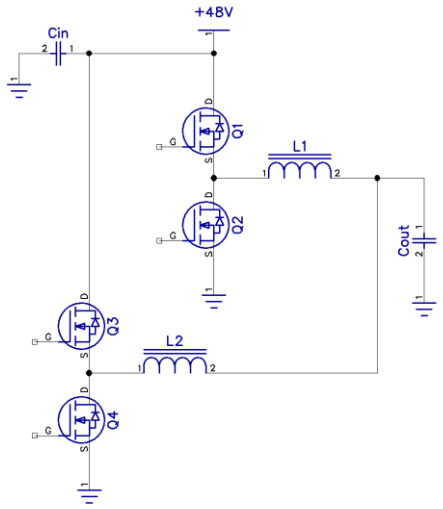
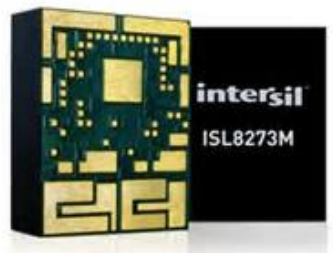
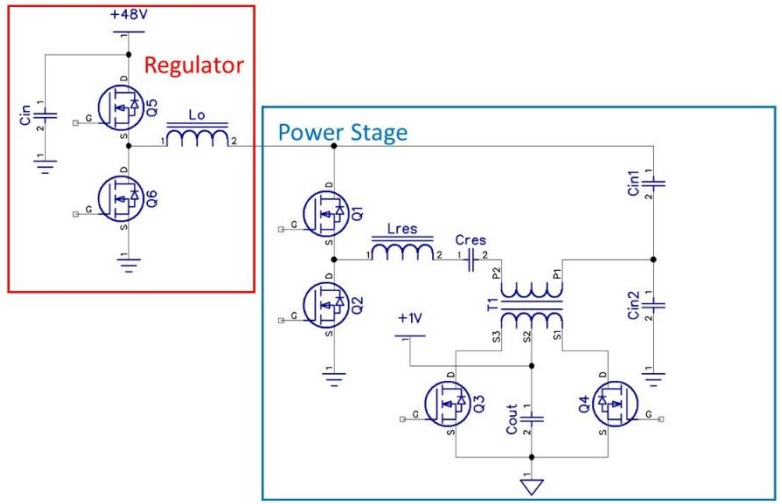
Breeding New Topologies

Multi-Phase Buck





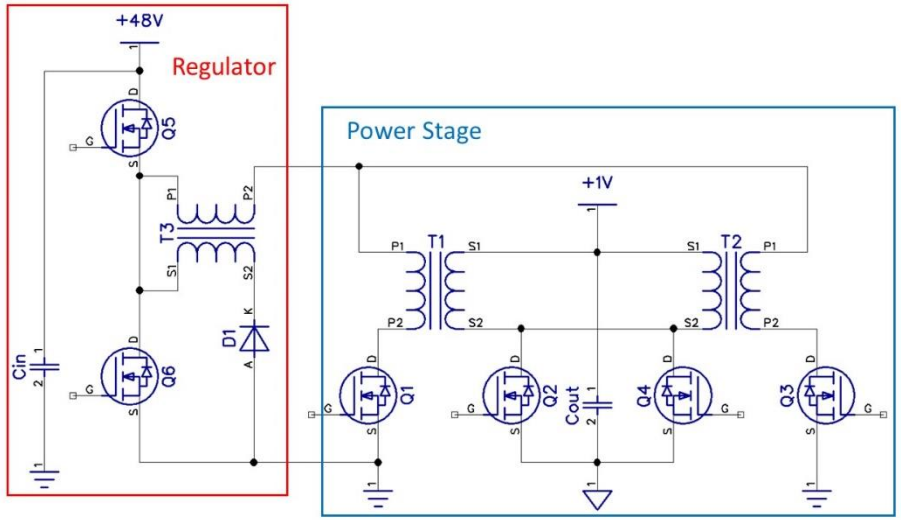
Resonant "Factorized" (Vicor)



440W/in^3

3800W/in^3

New Proposals



Valley-switched current-fed push-push
Sandler, DesignCon 2018

Others including Cuk Buck part 2??

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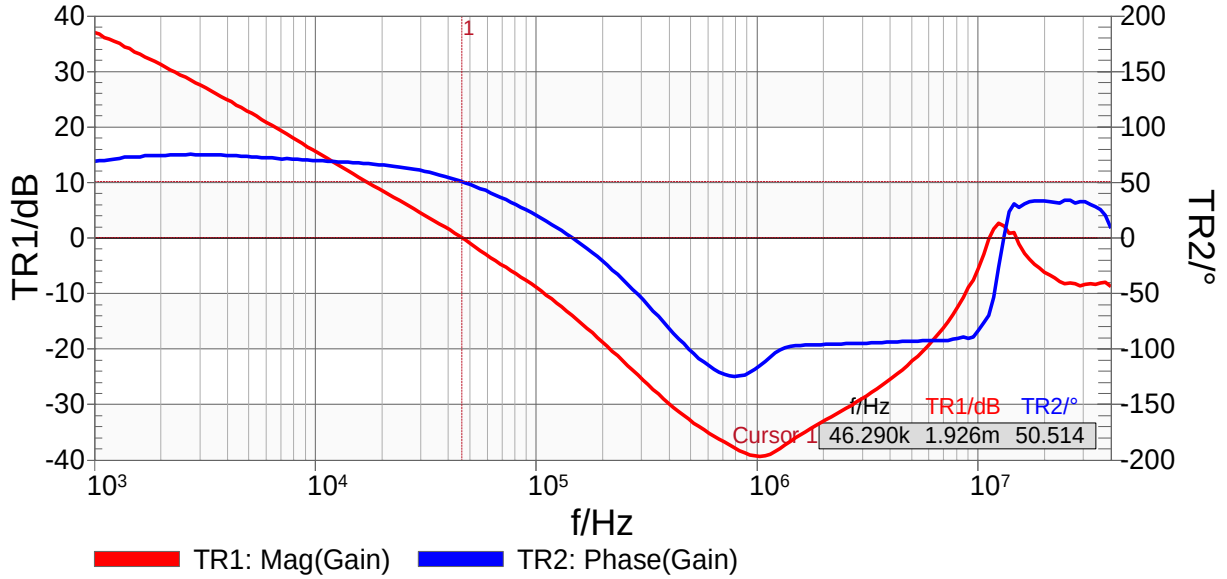
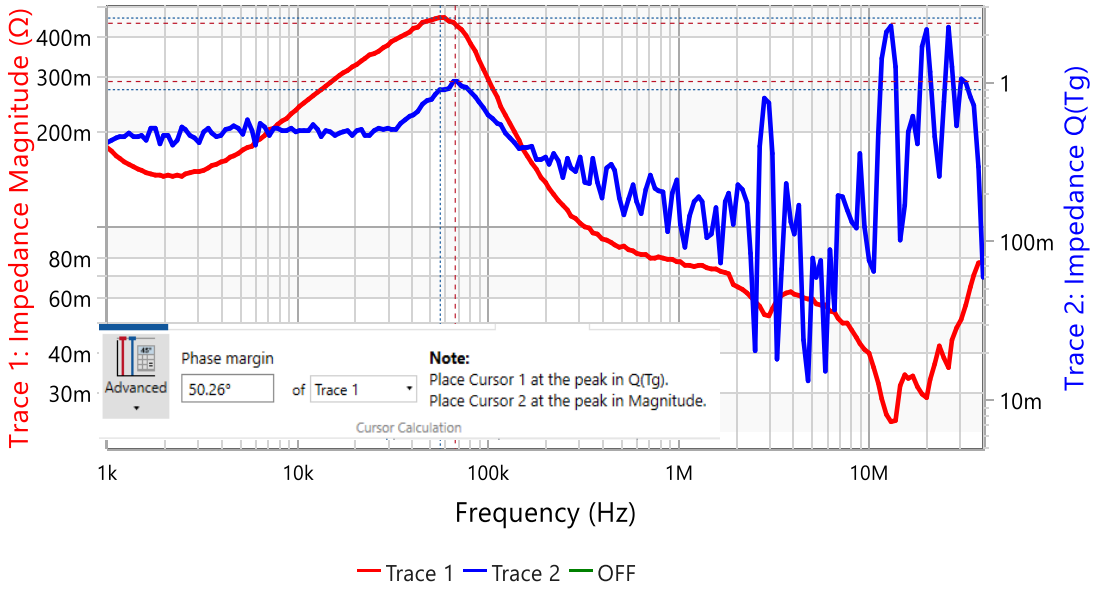
Breeding New Measurement Methods

5V to 3.3P POL
(Simple Switcher Step-Down Buck Regulator)

https://www.picotest.com/products_VRTS03.html
http://www.ti.com/product/lmr10515





	Bode Plot	NISM
Measured	50.26 deg	50.51 deg

Now available for VNA's from many manufacturers and soon to come to the Keysight ADS simulator

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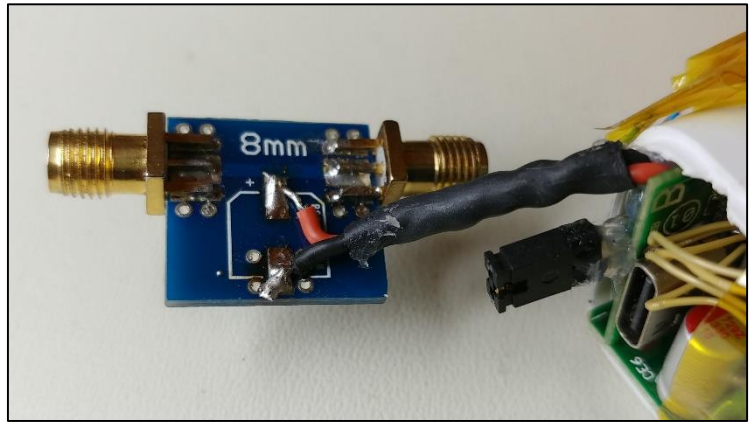
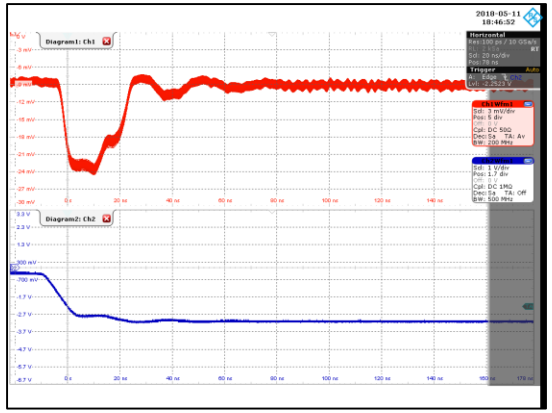
Sometimes EXTREME Methods

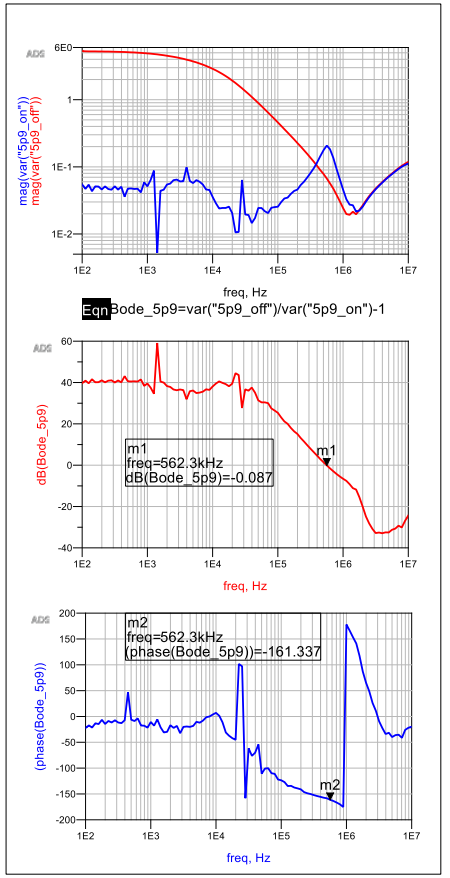


Enclosed USB-C Adapter/Cable

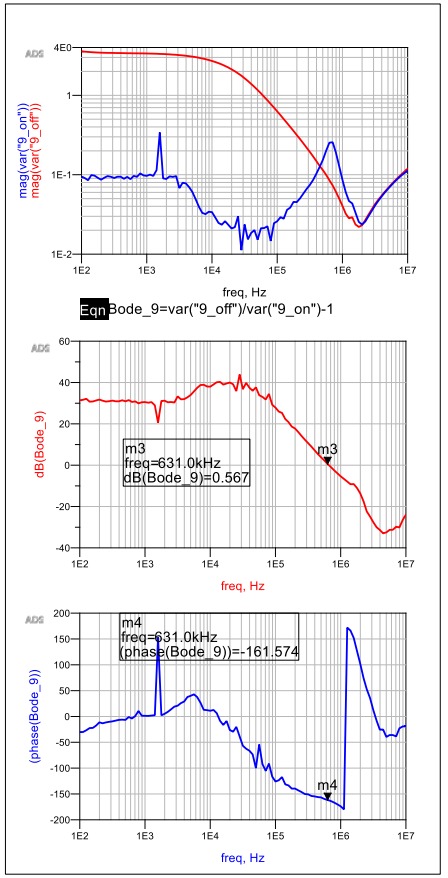
Cable TDR De-Embed



5.9V



9V



Extracted Internal Impedance
Reconstructed Bode Plot

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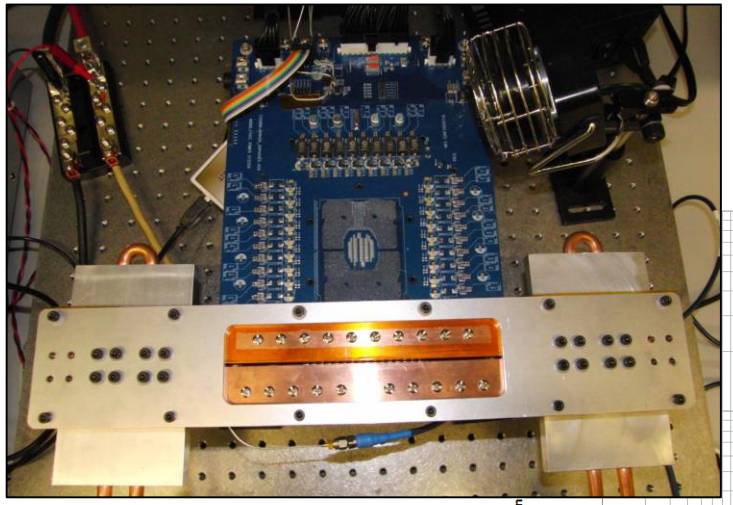
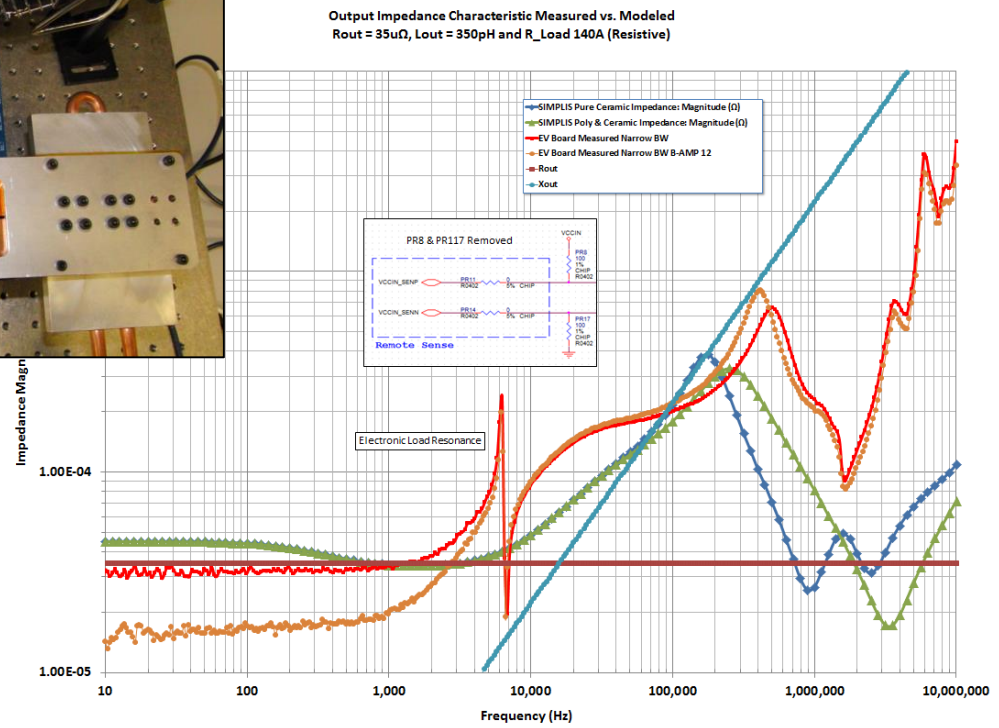
Target Impedance at sub-milliOhms

Even budgeting 5% of operating voltage to transients and limiting dynamic current to 50% results in ultra-low target impedance.



$35\ \mu\Omega\ PDN$



$$Z_{target} = \frac{0.7V \cdot 5\%}{1000A \cdot 50\%} = \frac{35mV}{500A} = 70\mu\Omega$$

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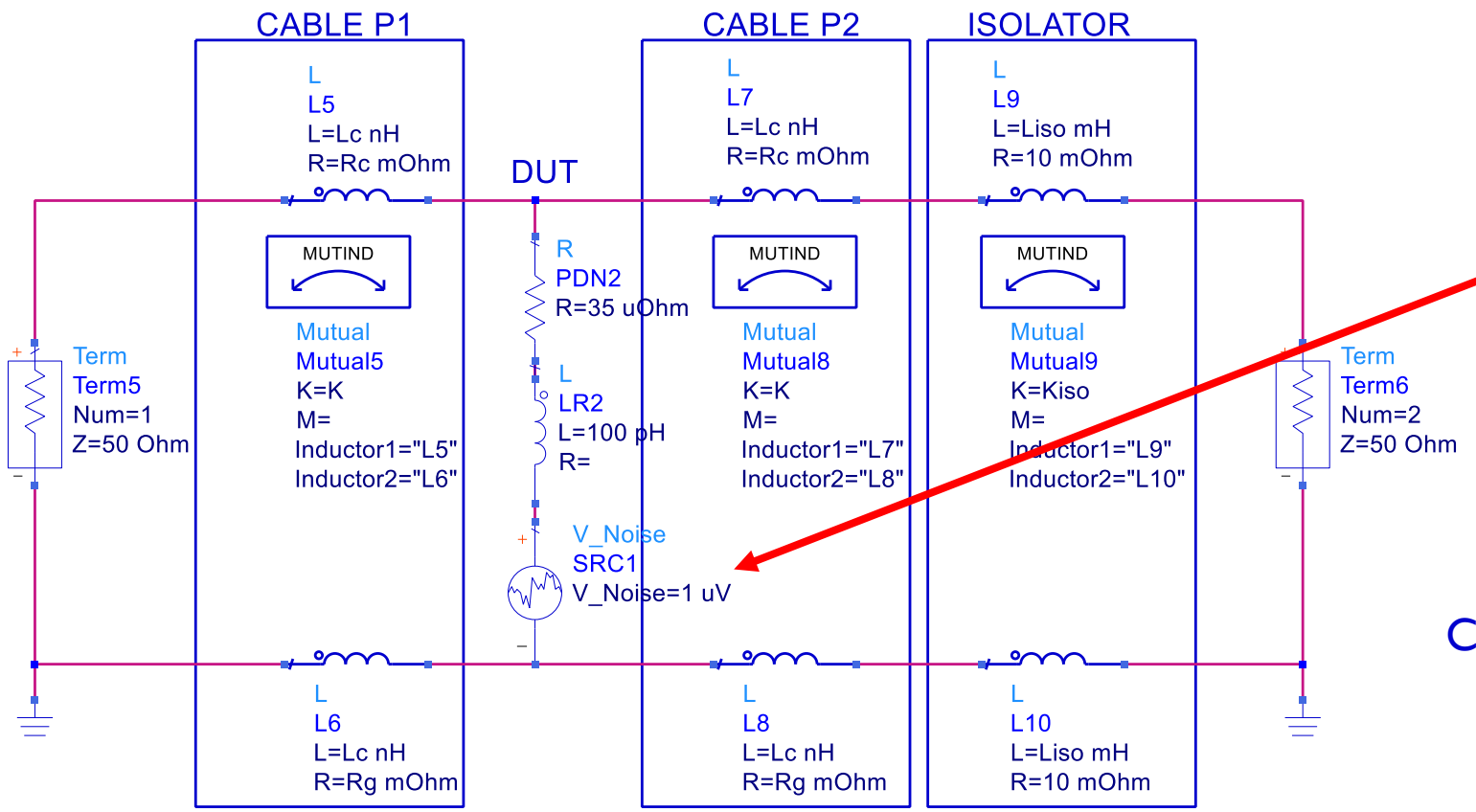
Low Z Measurement Circuit



The power rail includes noise due to switching ripple, load dynamics, switching frequency modulation noise and other system generated noise.

This noise is seen by VNA Port 2.

J2102B

Cable Parameters

Var Eqn

VAR
VAR1
K=0.98613
Lc=60

Isolator Parameters

Var Eqn

VAR
VAR2
Kiso=0.99993
Liso=0.32

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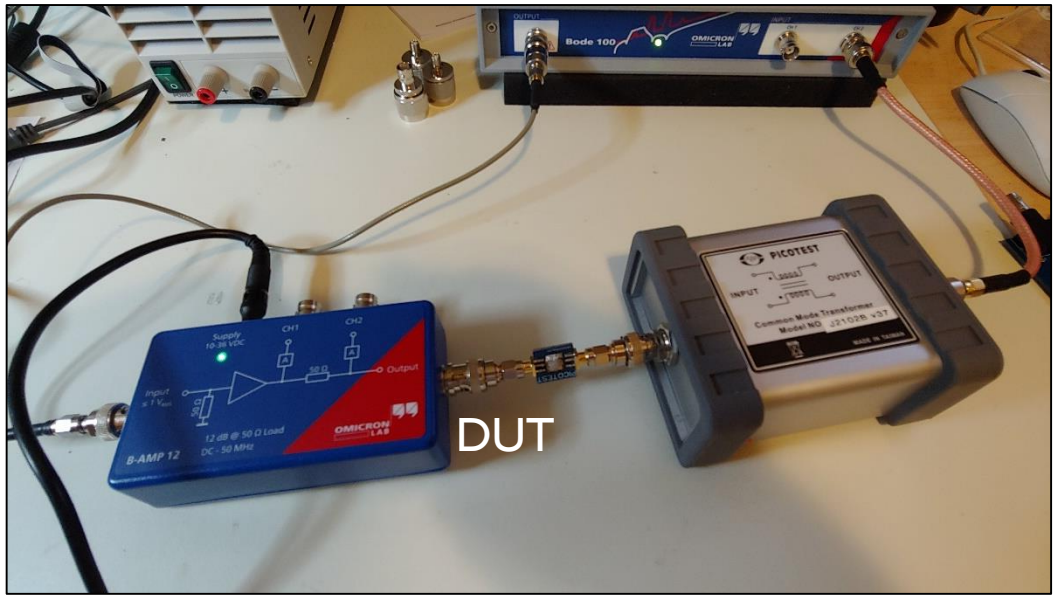
Power Rail Impedance Error Terms

$$V_{measured} = 0.223 \cdot \sqrt{e^{0.2306 \cdot dBm}} \cdot \left[\frac{DUT}{DUT + \frac{R_{port}}{2}} + \frac{1}{CMRR} \cdot \frac{R\_shield\_1}{R\_shield\_1 + R_{port}} + \frac{1}{10^{\frac{Noise\_Floor}{20}}} \right] + PDN\_V_{noise}$$

We have control over

We do NOT have control over

Error (Noise)



Performing this measurement required Picotest to:

- Add a source power amplifier
- Design a better isolator
- Develop better cables
- Develop accurate measurement standards for verification

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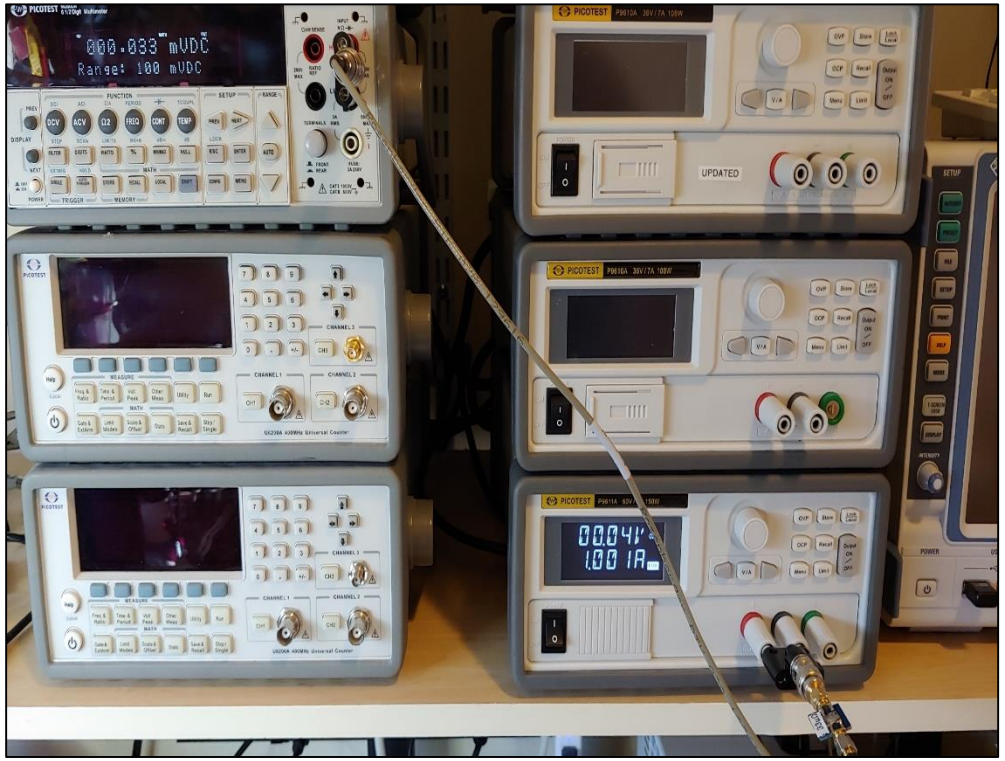
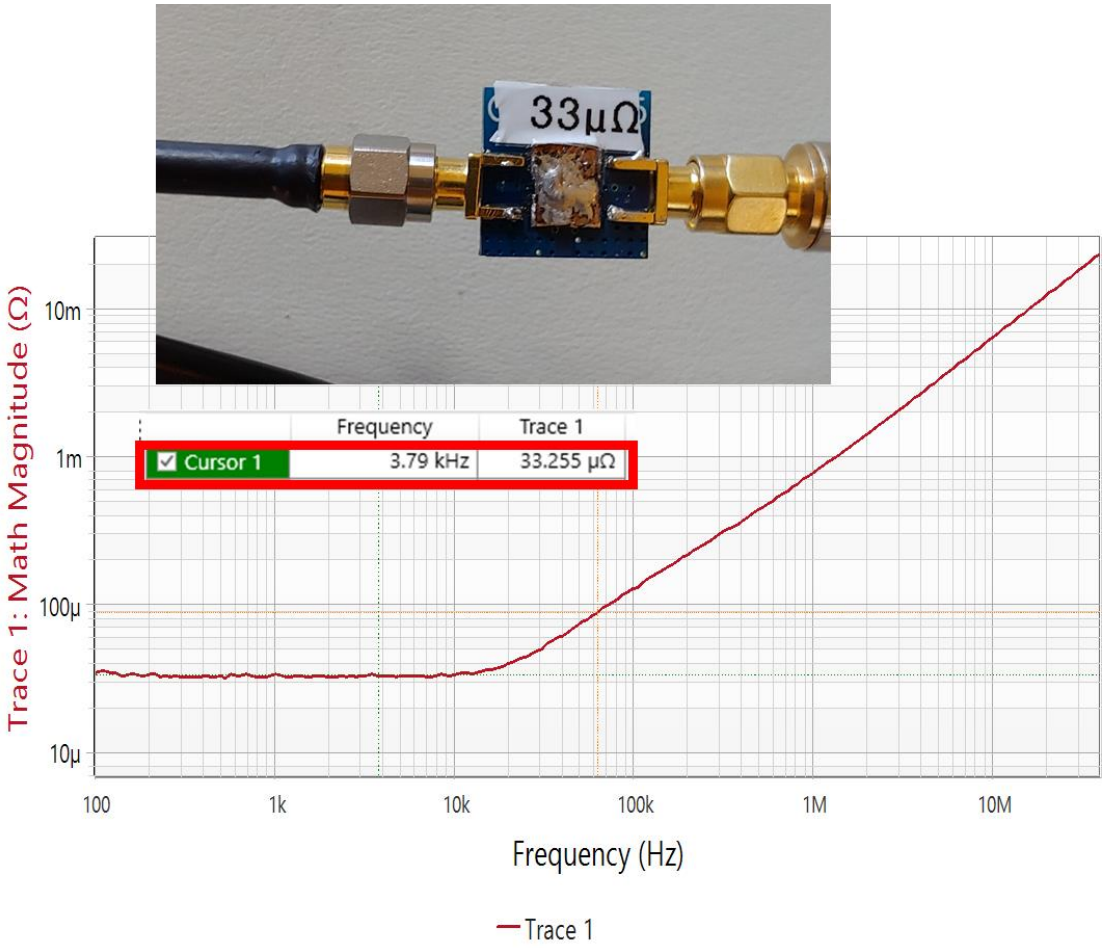
33μΩ with verification



The combined error of the current source, voltmeter and VNA are less than 1.5%.



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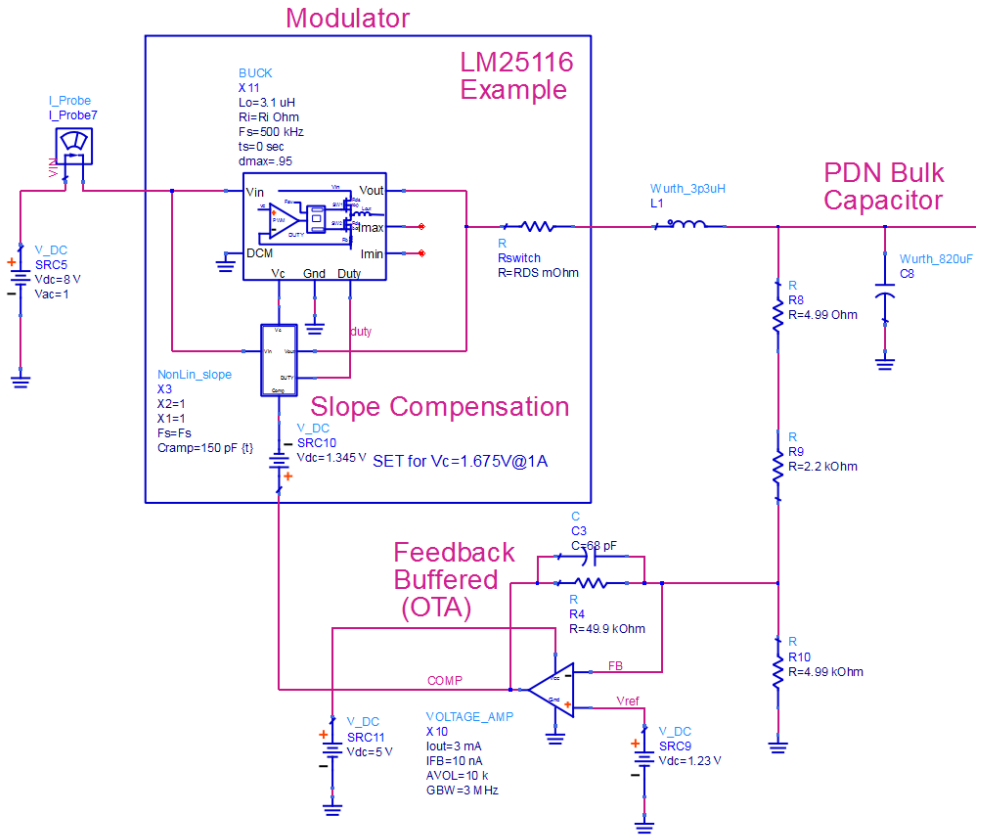
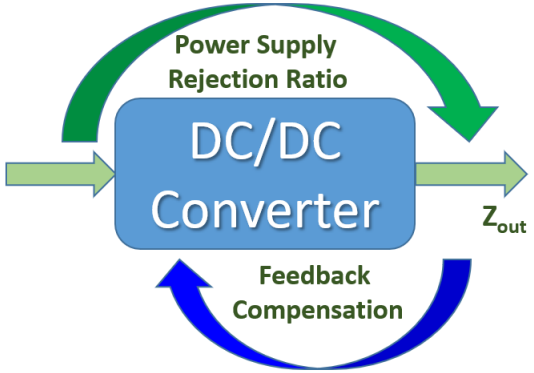
Measurement Derived Model



LM25116

$$PSRR\_dB = 20log\left[\left|\frac{Vo\cdot(Ri\cdot Vo - 2\cdot Fsw\cdot Lo\cdot Vramp)}{Ri\cdot Vin^2 - 2\cdot Ri\cdot Vo\cdot Vin + 2\cdot Fsw\cdot Lo\cdot Vin\cdot Vramp + 2\cdot Av\cdot Fsw\cdot Lo\cdot Vin}\right|\right]$$



$$Rout = \frac{\frac{2\cdot Fs\cdot Lo\cdot Ri\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}}{1 + Av\cdot\frac{2\cdot Fs\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}} + DCR + RDSon$$

$$Ri \cong \frac{\Delta Vcomp}{\Delta Io}$$

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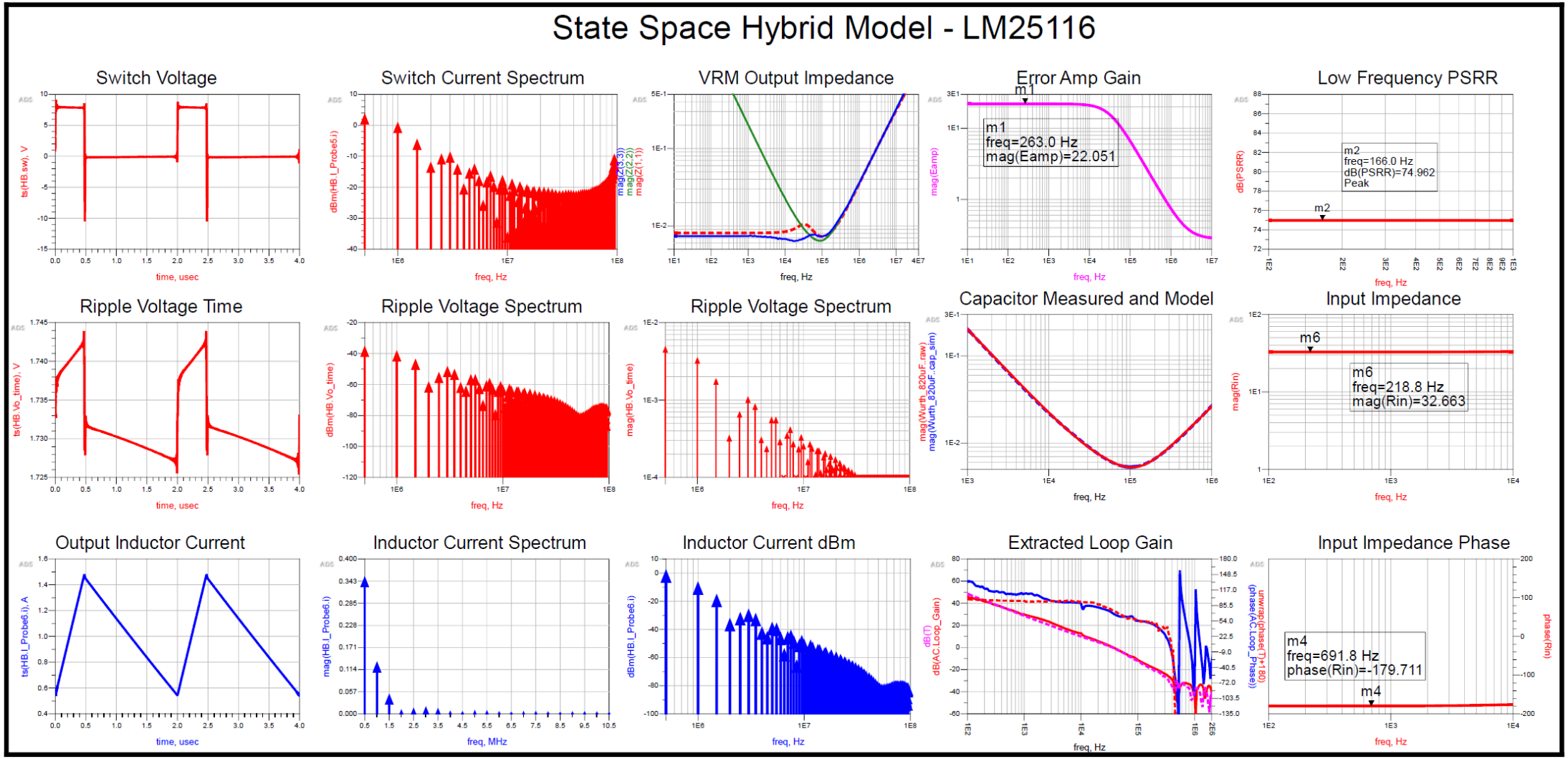
Multi-Domain Simulation Results



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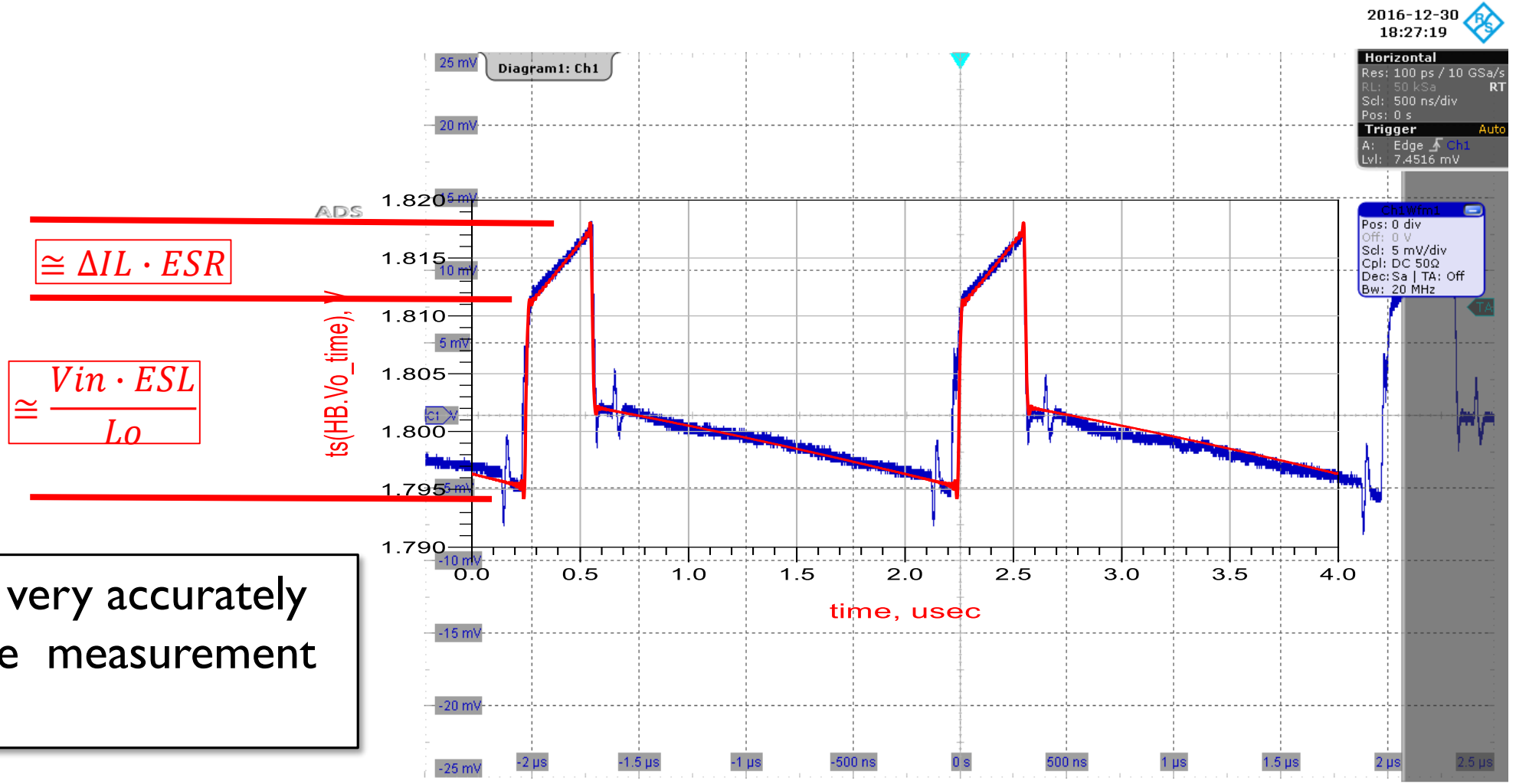
Simulated and Measured Ripple



The model very accurately matches the measurement results.

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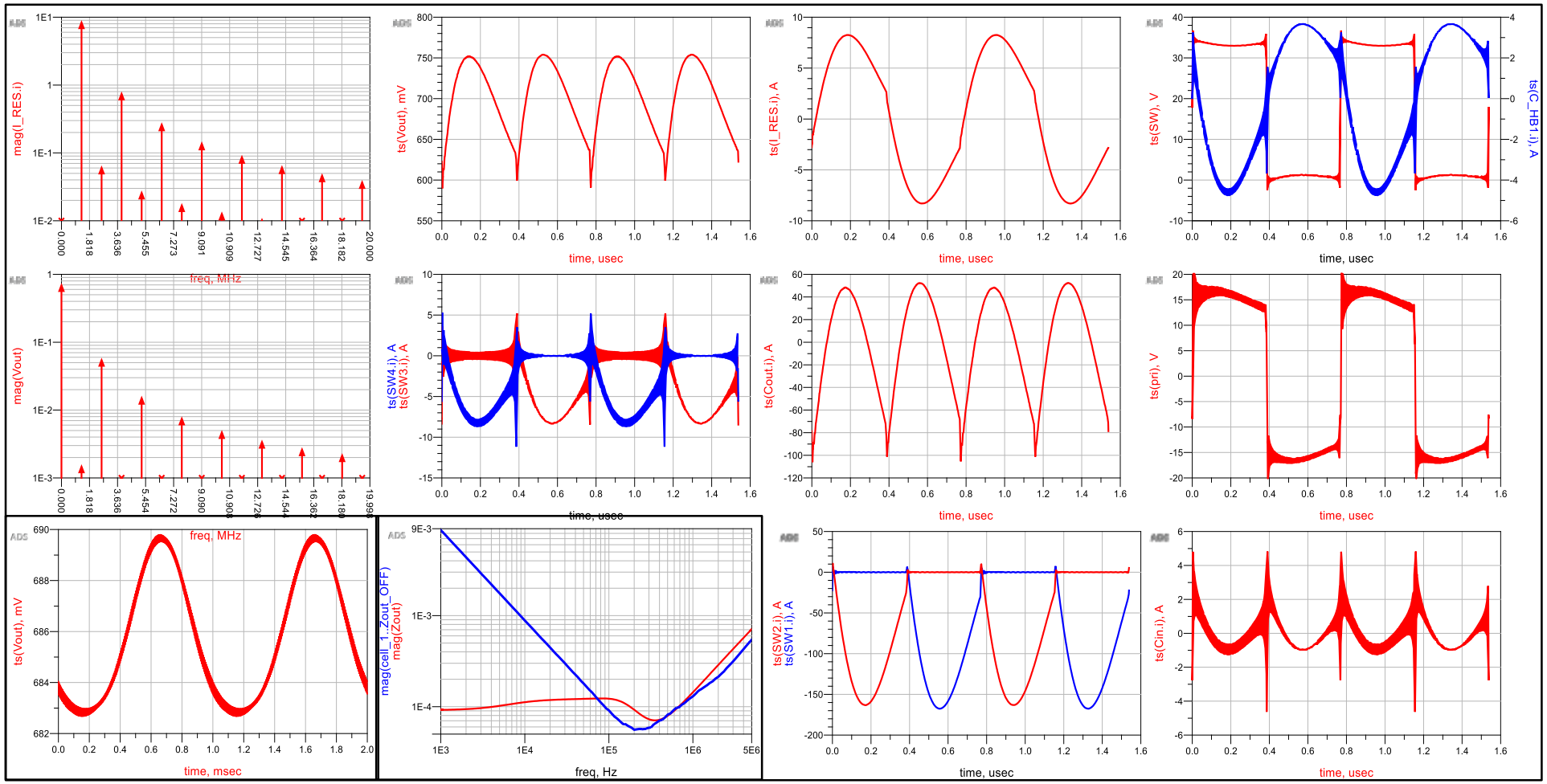
Multi Domain Simulation Results (Vicor VTM)



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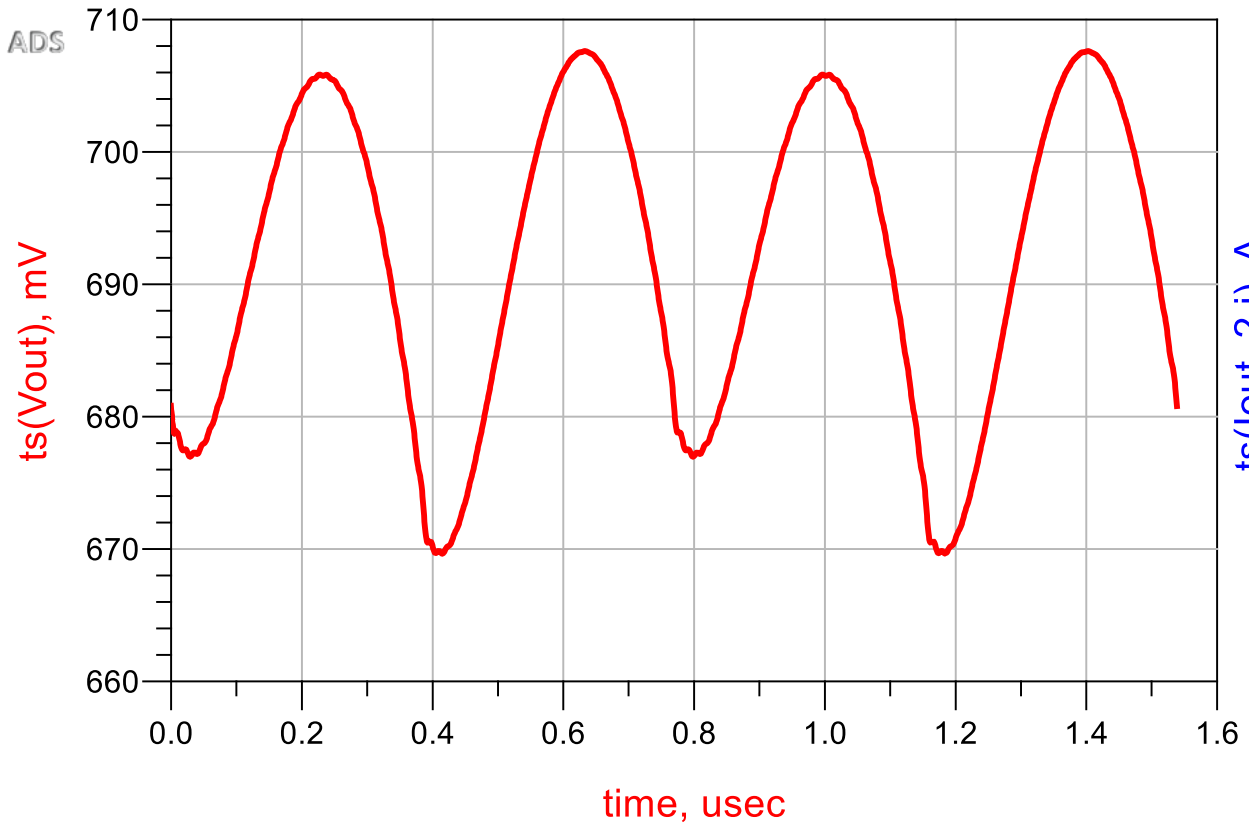
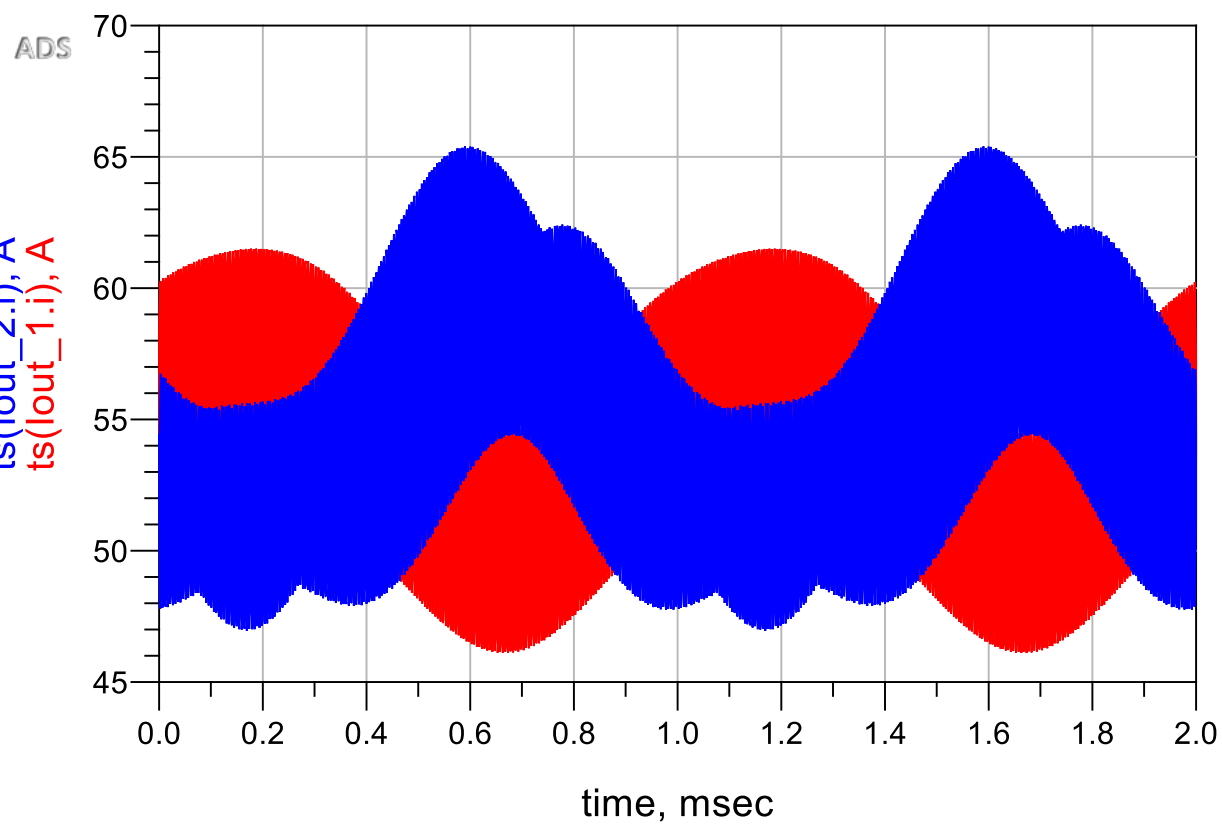
Vicor VTM Also Requires Beat Assessment

Applying Harmonic Balance to assess the beat frequency noise





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GaN Challenges

dV/dt 300kV/us at 600V

Tektronix solved the dV/dt measurement challenge with their near-infinite CMRR optical IsoVu probe

What about measuring current?

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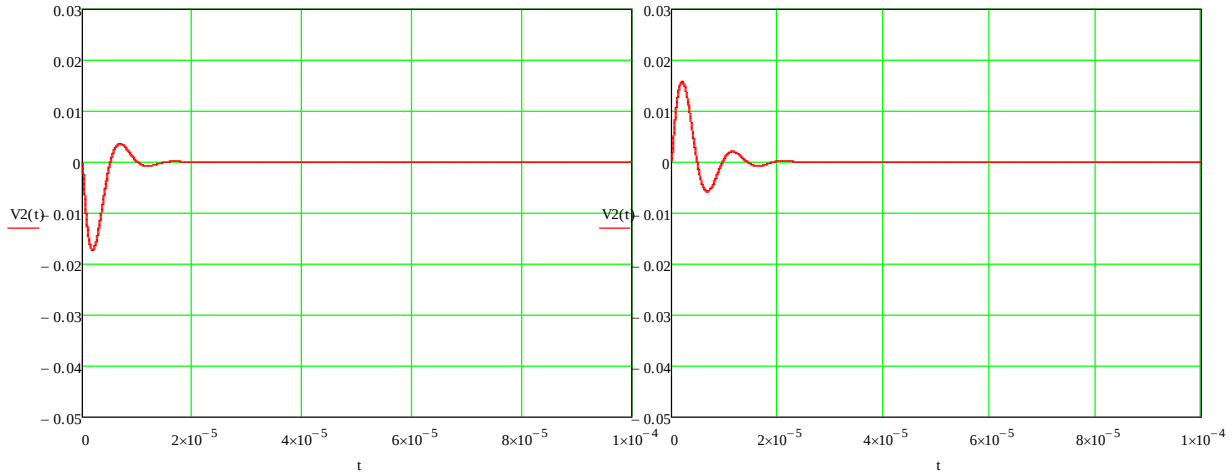
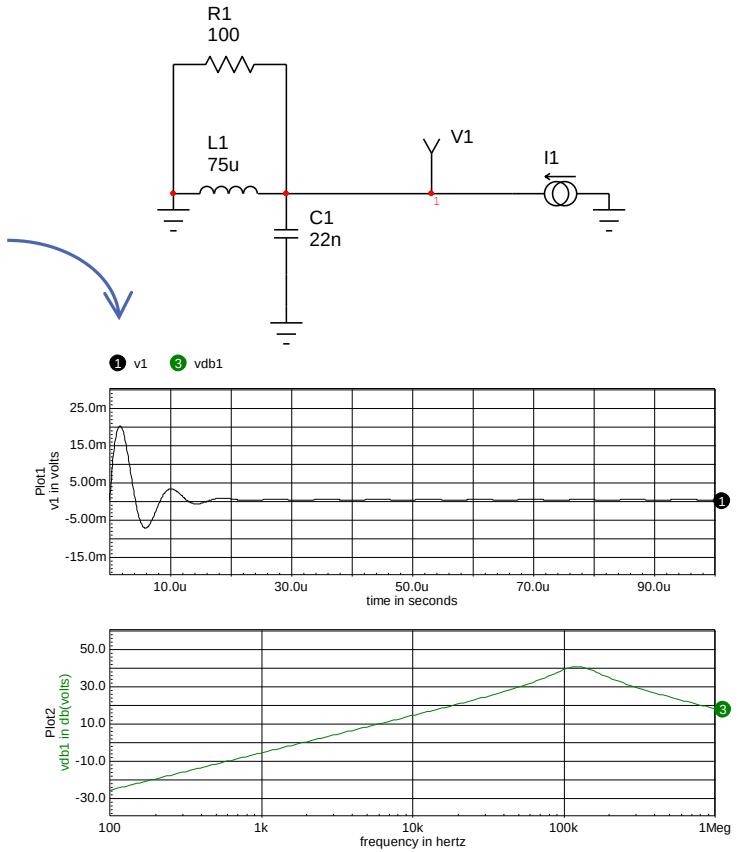
Scope to SPICE and Synthesized Optimization



Q	1.117	Q	1.65
Phase Margin	47.42 Deg	Phase Margin	33.6 Deg
L	75uH	L	65uH
C	.024uF	C	.025uF
fo	115kHz	fo	120kHz
f1	70kHz	f1	105kHz
Zo	55.9Ω	Zo	49.7Ω
Zpk	62.4	Zpk	82.0Ω
Worst Case Vpp*	39.7mV	Worst Case Vpp*	52mV



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Large Signal ASIC Emulation

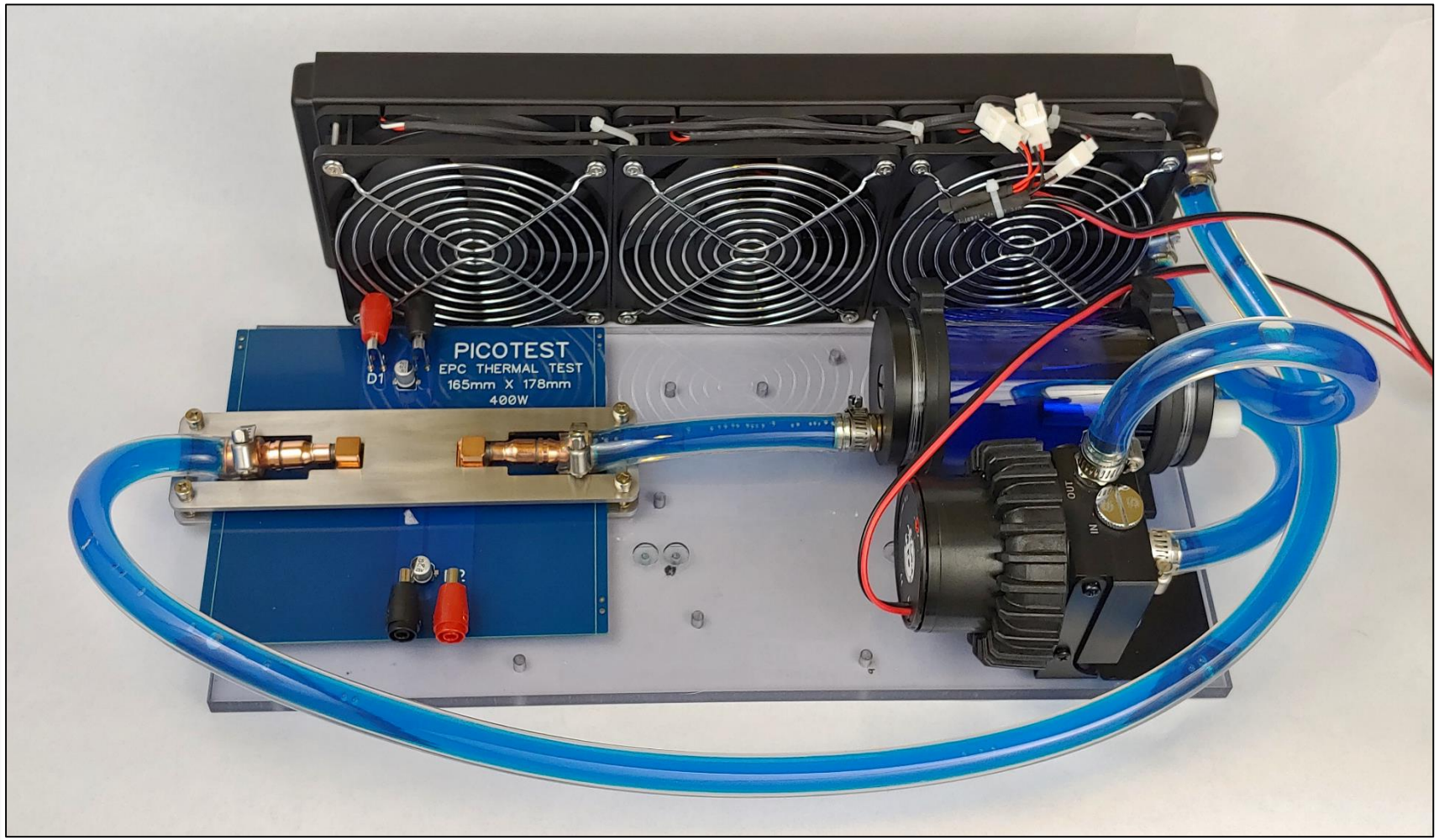
Higher power ASICS also require higher power in-socket loads.

Heat flux of >10W/mm2 is a challenge

Desired DC current >750Amps

Desired slew rate of >10kA/us

We are just beginning our development



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