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Accurately Modeling an Advanced IC Package for Chip/Package/Board Electrical/Thermal Co-Simulation

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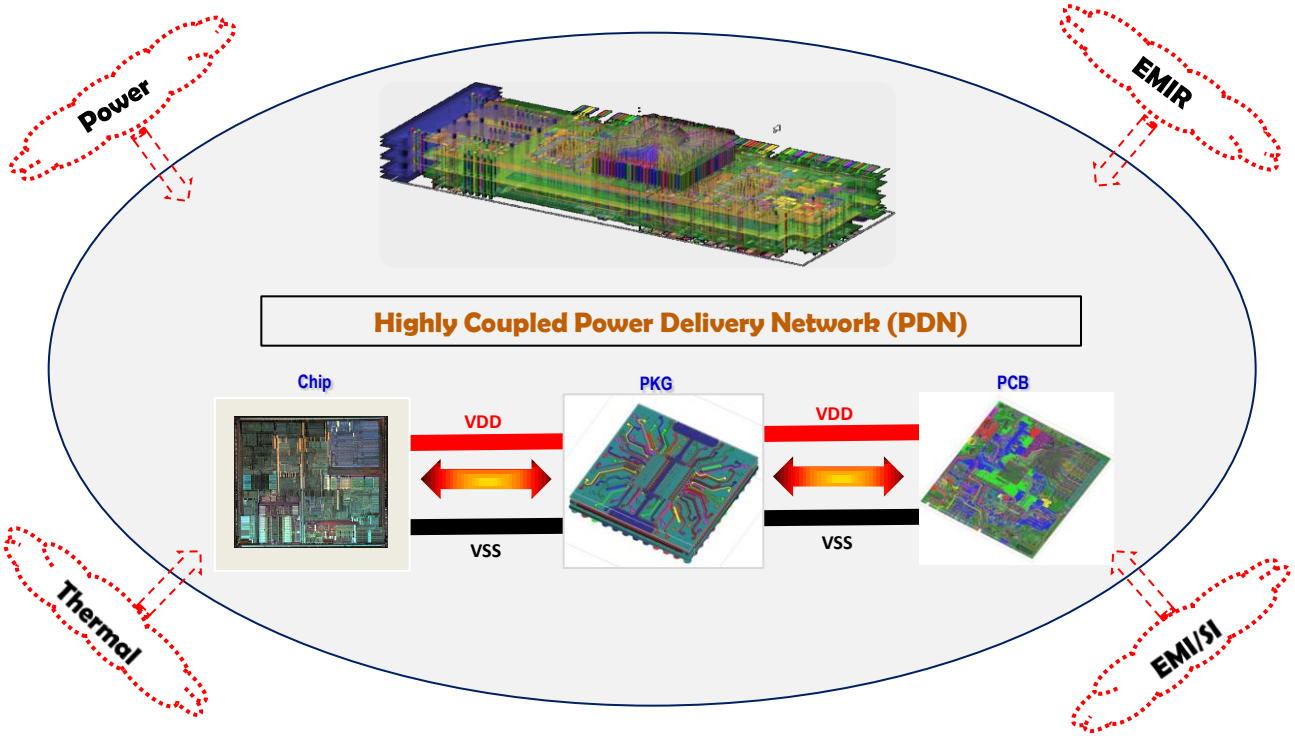
Agenda

- Introduction
- Methods to Model an IC Package for Electrical/Thermal Co-Simulation
- Correlation Results
- Conclusions

INTRODUCTION

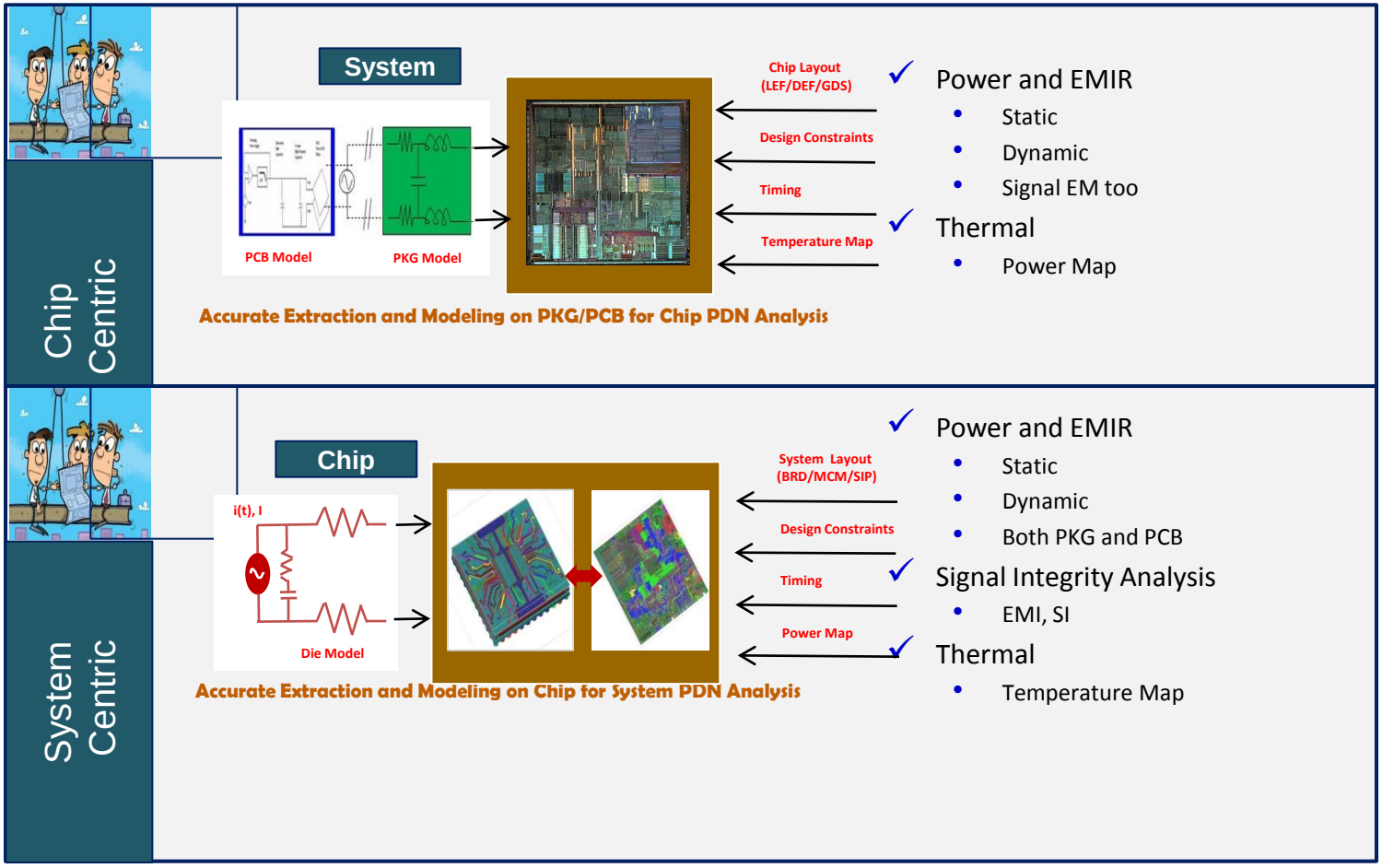
A Complete Power Delivery Network

Power Integrity Analysis from Chip to Package to Board



A Challenging Problem That Requires an Accurate "Chip-PKG-PCB" Co-Simulation

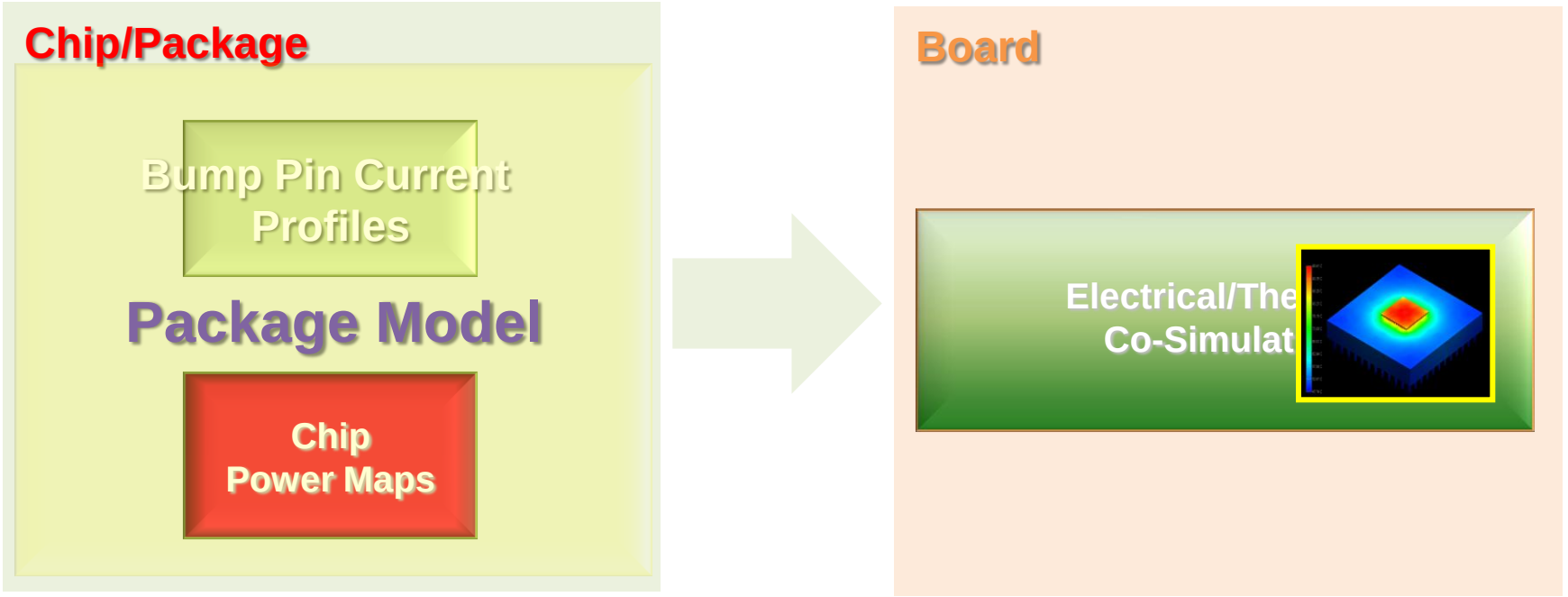
Solutions to IC Designers and System Designers



Background

- More and more IC vendors do NOT provide detailed IC package design for their system designers
  - Detailed package design is IP
  - Advanced package maybe
    - Large pin count/size
    - Multi-chip package
- Instead package model is provide
  - AC
  - DC
  - Electrical/Thermal(E/T) co-simulation
- Reasons
  - Easy for Chip/package/board co-design
    - Same target on chip side
  - Protect IP
  - Performance

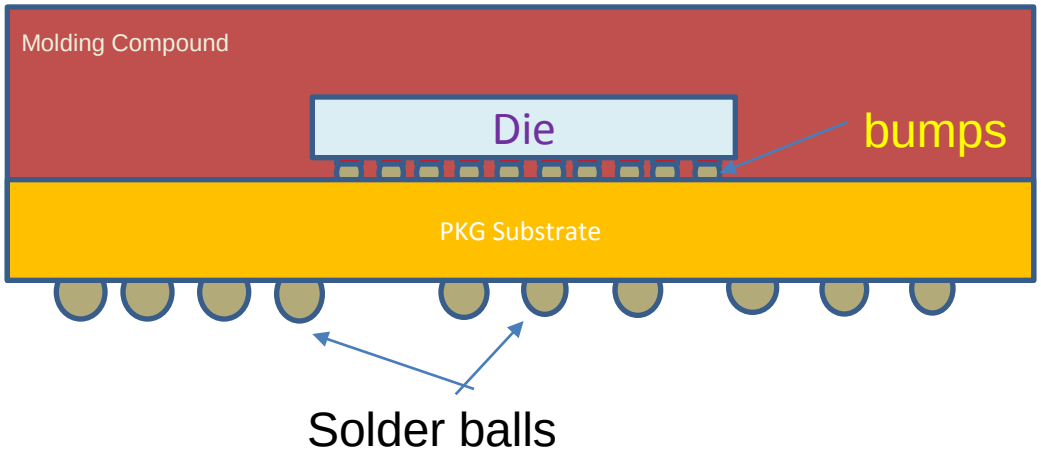
Revised System Centric Electrical/Thermal Co-Simulation Flow



METHODS TO MODEL AN IC PACKAGE FOR ELECTRICAL/THERMAL CO-SIMULATION

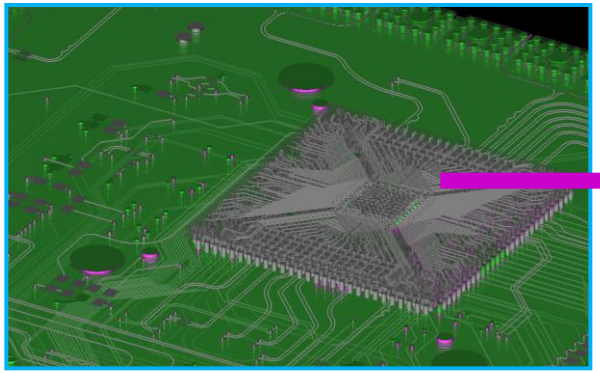
Electrical Model

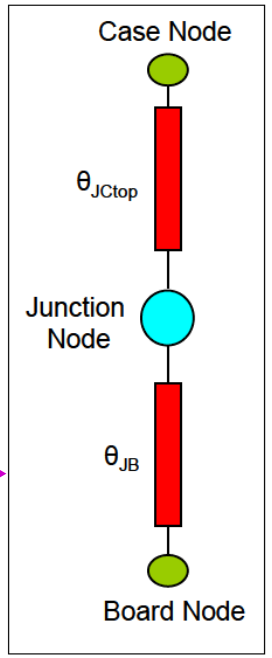
- Resistance network
- Terminal settings
  - Component pin base
  - Grid base
  - Net base



Thermal Model

- 2-Resistor CTM
  - θ_{jc} $\theta_{jc} = \frac{T_j - T_c}{P}$
  - θ_{jb} $\theta_{jb} = \frac{T_j - T_b}{P}$

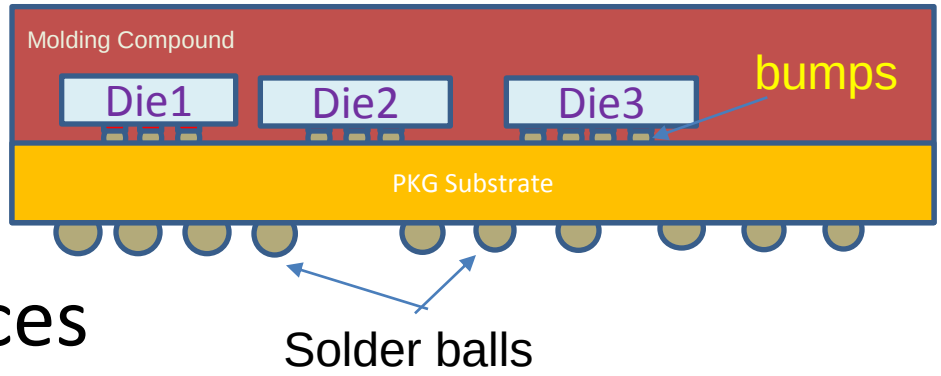




- Multi-terminal thermal resistance network
  - Pin base/grid base/net base terminals for circuits
  - Grid base/net base terminals for substrate layers

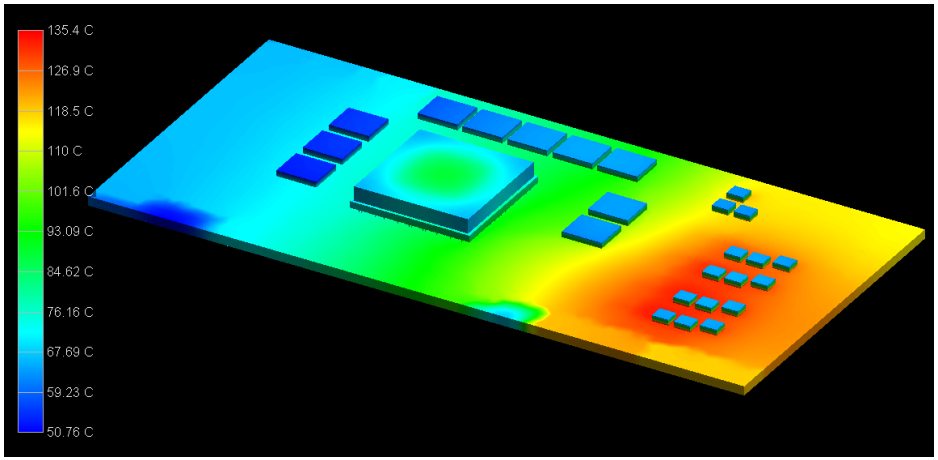
Single-Die and Multi-Dies Package

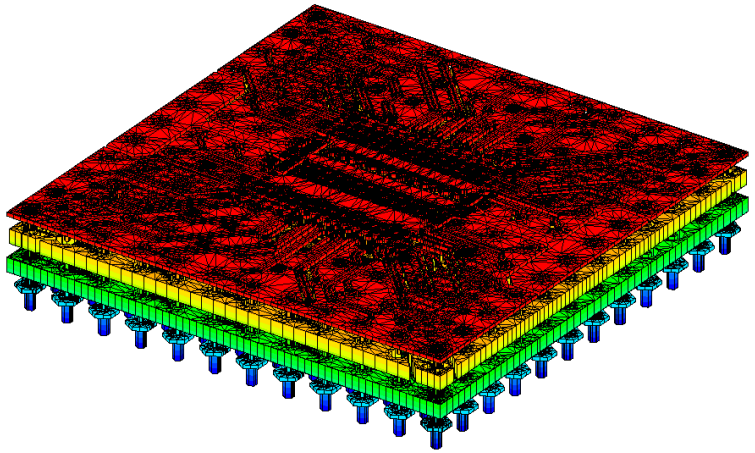
- Bump pin current support
- Die power map
- Multiple heat sources
- Multiple current sources
- Be able to change current and power source values while using the model
  - Re-distribute power map with new power value

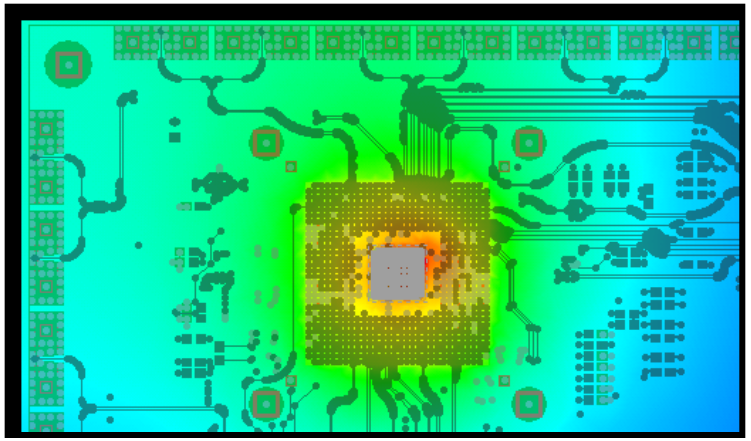


Leading Edge 3D/2.5D Thermal Technologies

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right)+Q=\rho c \frac{\partial T}{\partial t}$$



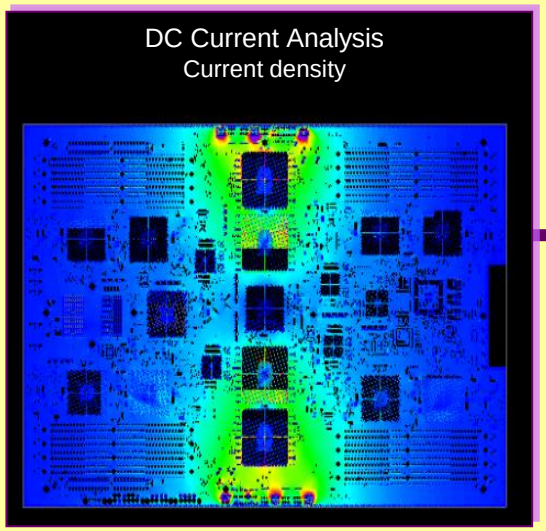




- Steady-state heat conduction with convection and radiation BCs
- Finite element method with adaptive meshing, model order reduction, and multi-grid method solver

Electrical/Thermal Co-Simulation

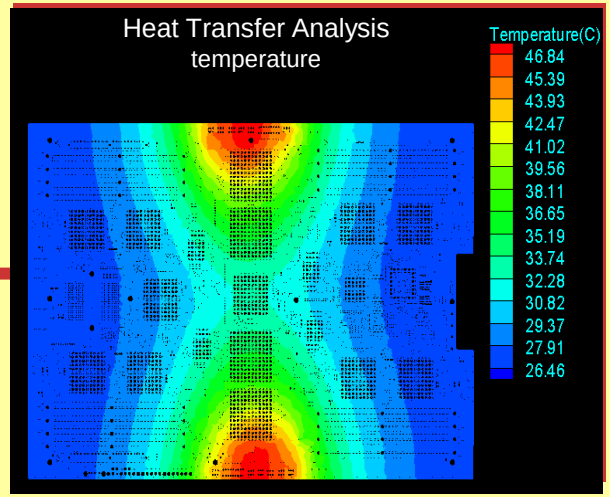
E/T Co-Simulation



Current density is an input for heat transfer analysis

Iteration

Temperature is an input for DC current analysis



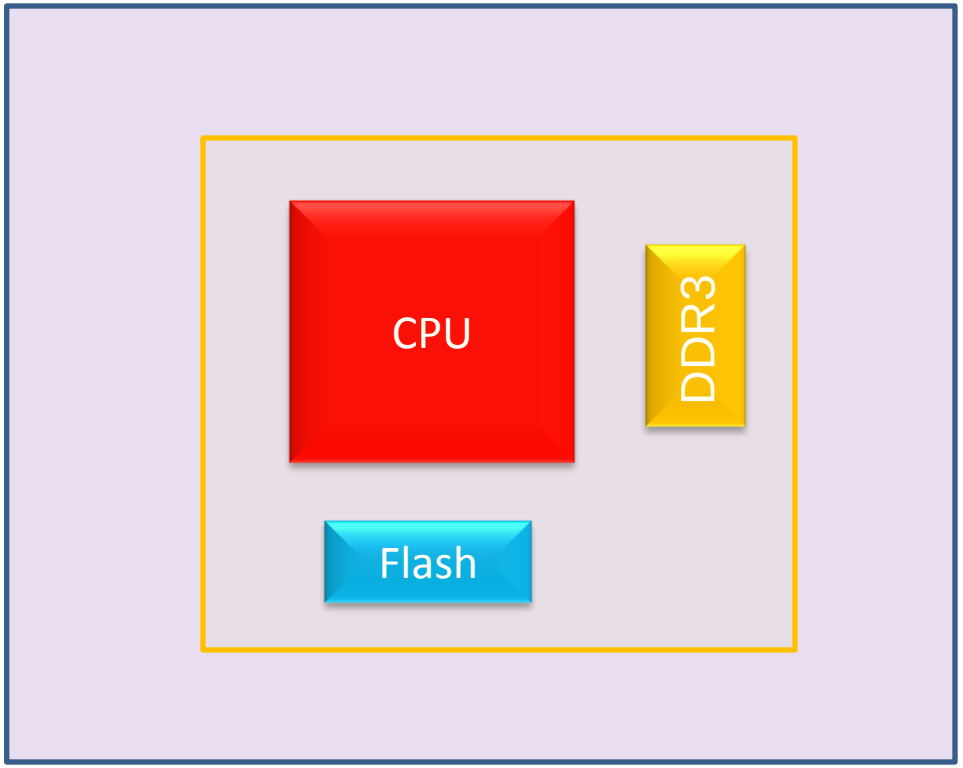
Both electrical resistance and leakage power dissipation increase at higher temperatures

Joule and component heating will change temperature distribution

CORRELATION RESULTS

Test Case

- 6 layers package
- 4 layer PCB
  - Top
  - Plane02
  - Plane03
  - Bottom
- Multi-dies
- Ambient temperature:25C



Comparison Cases

- Die/Package/Board are merged together for FEM simulation (FEM)
  - Golden
- Package model on PCB simulation (PETM)
  - Compare to golden
- 2-Resistor CTM on PCB simulation (2-R CTM)
  - Compare to golden
- Compare the electrical distributions and temperature distributions on each PCB layer
  - IR drop
  - Current density
  - Temperature
  - PCB Layers
    - Top
    - Plane02
    - Plane03
    - Bottom

Correlation Results

PACKAGE WITH ONE DIE

Package with Single Die Being Enabled

- Single die enabled
  - DDR3 Die
- One heat source
  - Total 1W
  - Power map distribution
- E/T Co-Simulation with 2-Resistor CTM
  - Theta Jc=10.12
  - Theta Jb=11.075
  - Power =1W

Summary for One-Die Package IR Drop on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	535.474nV	1.40276mV	531.757nV	1.38783mV	-0.69~-0.43	531.757nV	1.38783mV	-0.69~-0.43
Plane02 Layer	15.574uV	1.2015 mV	15.5703uV	1.20088mV	-0.024~-0.062	15.5703uV	1.20088mV	-0.024~-0.062
Plane03 Layer	535.474nV	1.2088 mV	531.757nV	1.20894mV	-0.69~0.01	531.757nV	1.20894mV	-0.69~0.01
Bottom Layer	0V	1.20882mV	0V	1.20894mV	0~0.01	0V	1.20894mV	0~0.01

Voltage Drop

Summary for One-Die Package Current Density on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	0.2474 mA/mm2	7.66122 A/mm2	0.248039 mA/mm2	7.30418 A/mm2	0.25 ~ -4.66	0.248039 mA/mm2	7.30418 A/mm2	0.25 ~ -4.66
Plane02 Layer	0 A/mm2	15.111 A/mm2	0 A/mm2	15.1103 A/mm2	0 ~ -0.005	0 A/mm2	15.1103 A/mm2	0~ -0.005
Plane03 Layer	0 A/mm2	15.4063 A/mm2	0 A/mm2	15.4058 A/mm2	0 ~ -0.003	0 A/mm2	15.4058 A/mm2	0 ~ -0.003
Bottom Layer	0 A/mm2	0.95368 A/mm2	0 A/mm2	0.953649 A/mm2	0 ~ -0.003	0 A/mm2	0.953649 A/mm2	0 ~ -0.003

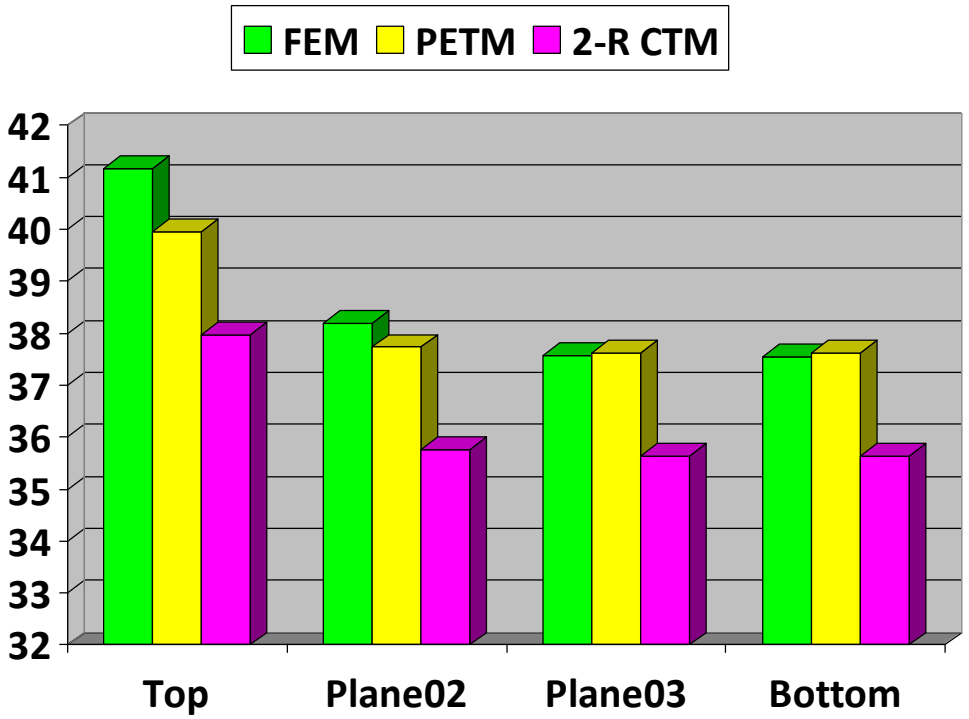
Summary for One-Die Package Temperature on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference %	Min	Max	Difference%
Top Layer	26.6227C	41.1735C	26.5675C	39.9504C	-0.21 ~ -2.88	26.6328C	37.9752C	0.04 ~ -7.77
Plane02 Layer	26.6358C	38.1922C	26.5796C	37.7308C	-0.21 ~ -1.21	26.6454C	35.7604C	0.036 ~ 6.37
Plane03 Layer	26.6432C	37.5607C	26.5853C	37.6288C	-0.22 ~ 0.18	26.6514C	35.6453C	0.03 ~ -5.1
Bottom Layer	26.6364C	37.5393C	26.5786C	37.6202C	-0.22 ~ 0.22	26.6445C	35.6412C	0.03 ~ -5.06

Max Temperature on PCB Layers (Unit: ^{o}C)

PETM vs FEM

Maximum temperature difference: ~1.2^{0}C



2-R CTM vs FEM

Maximum temperature difference: ~3.2^{0}C

Correlation Results

PACKAGE WITH TWO DIES

Two-Die Package Settings

- Two dies enabled
  - CPU and DDR3
- Two heat sources
  - 1.9W for CPU, power map distribution
  - 1W for DDR3, power map distribution
- E/T Co-Simulation with 2-Resistor CTM
  - Theta Jc=4.124
  - Theta Jb=5.424
  - Power =2.9W

Summary for Two-Die Package IR Drop on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	2.30641uV	15.1269mV	2.30658uV	15.0622mV	0.007~-0.43	2.30658uV	15.0622mV	0.007~-0.43
Plane02 Layer	136.037uV	7.03396mV	136.037uV	7.03541mV	0~-0.02	136.037uV	7.03541mV	0~-0.02
Plane03 Layer	321.416nV-	14.311mV	305.839nV	14.3089mV	-4.85~-0.01	305.839nV	14.3089mV	-4.85~-0.01
Bottom Layer	0V	14.311mV	0V	14.3089mV	0~-0.01	0V	14.3089mV	0~-0.01

Summary for Two-Die Package Current Density on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	7.55136mA/mm2	40.5832A/mm2	7.55145 mA/mm2	38.8896 A/mm2	0. 0009~ -0.04	7.55145 mA/mm2	38.8896 A/mm2	0. 0009~ -0.04
Plane02 Layer	0 A/mm2	98.8423 A/mm2	0 A/mm2	98.843 A/mm2	0 ~ 0.0007	0 A/mm2	98.843 A/mm2	0 ~ 0.0007
Plane03 Layer	0 A/mm2	162.037 A/mm2	0 A/mm2	162.04 A/mm2	0 ~ 0.0018	0 A/mm2	162.04 A/mm2	0 ~ 0.0018
Bottom Layer	0 A/mm2	6.22799 A/mm2	0 A/mm2	6.228 A/mm2	0 ~ 0.0016	0 A/mm2	6.228 A/mm2	0 ~ 0.0016

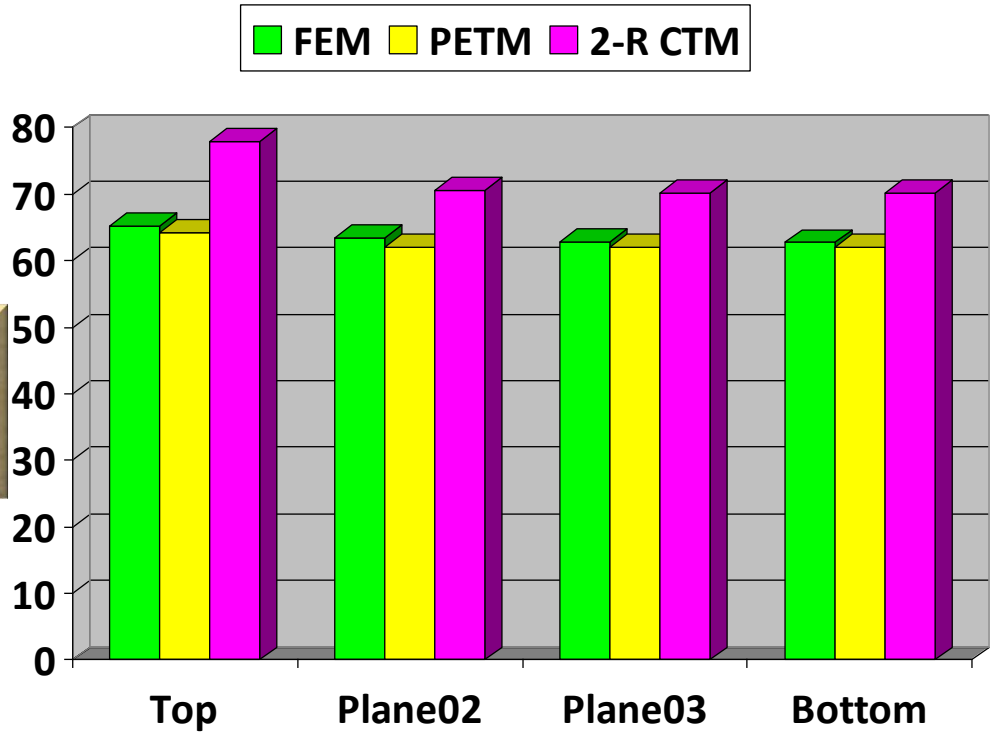
Summary for Two-Die Package Temperature on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	30.3352C	65.1875C	30.7781C	64.2049C	1.46 ~ -1.5	32.2025C	77.9787C	6.16 ~ 19.62
Plane02 Layer	30.3781C	63.4237C	30.8227C	62.0951C	1.46~-2.09	32.258C	70.6339C	6.19 ~ 11.37
Plane03 Layer	30.4027C	62.7613C	30.8438C	61.9574C	1.45 ~ -1.28	32.2844C	70.2099C	6.19 ~ 11.87
Bottom Layer	30.3801C	62.725C	30.8193C	61.9491C	1.45 ~ -1.24	32.2538C	70.196C	6.17 ~ 11.91

Max Temperature on PCB Layers (Unit: ^{o}C)

PETM vs FEM

Maximum temperature difference: ~1.3^{0}C



2-R CTM vs FEM

Maximum temperature difference: ~12.8^{0}C

Correlation Results

PACKAGE WITH THREE DIES

Three-Die Package Settings

- Three dies enabled
  - CPU and DDR3 and Flash
- Three heat sources
  - 1.9W for CPU, power map distribution
  - 1W for DDR3, power map distribution
  - 1W for Flash, power map distribution
- E/T Co-Simulation with 2-Resistor CTM
  - Theta Jc= (87.05184-70.069505)/3.9=4.354
  - Theta Jb= (87.05184-65.184366)/3.9=5.607
  - Power =3.9W

Summary for Three-Die Package IR Drop on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	2.25052uV	15.1255mV	2.2508uV	15.0608mV	0.012~-0.43	2.2508uV	15.0608mV	0.012~-0.43
Plane02 Layer	135.848uV	7.6103mV	135.848uV	7.61131mV	0 ~ 0.013	135.848uV	7.61131mV	0 ~ 0.013
Plane03 Layer	0.648459uV	14.3096mV	0.67202uV	14.3075mV	3.63~ -0.015	0.67202uV	14.3075mV	3.63~ -0.015
Bottom Layer	0V	14.3096mV	0V	14.3075mV	0~-0.01	0V	14.3075mV	0~-0.01

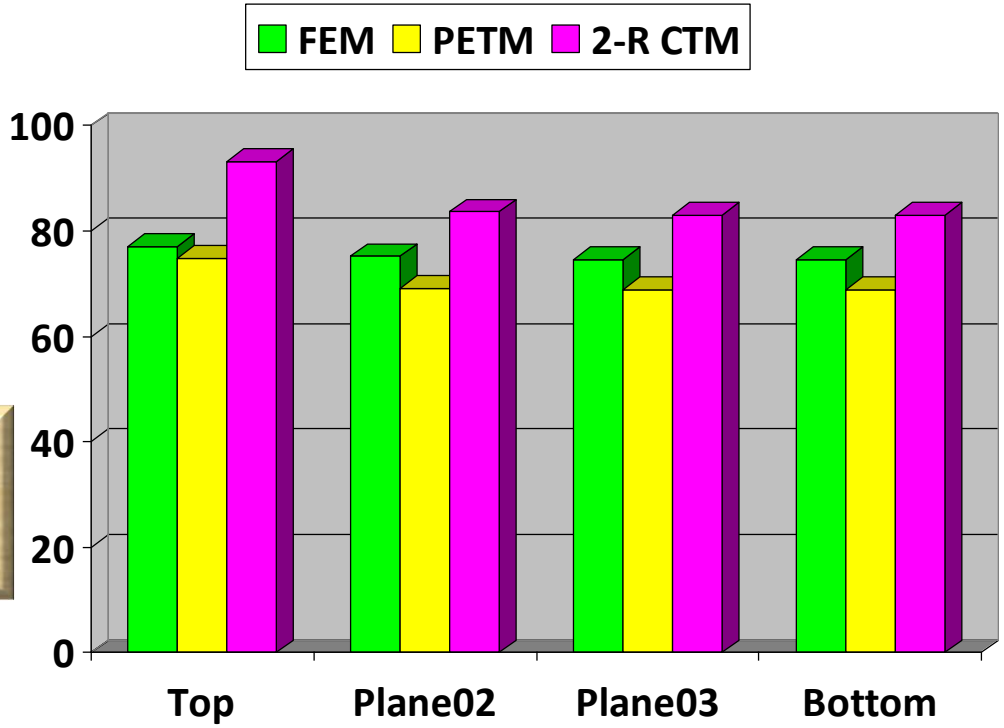
Summary for Three-Die Package Current Density on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	7.56079 mA/mm	40.5831 A/mm2	7.56088 mA/mm2	38.8994 A/mm2	0.001~ -4.15	7.56088 mA/mm2	38.8994 A/mm2	0.001 ~-4.15
Plane02 Layer	0 A/mm2	99.0298 A/mm2	0 A/mm2	99.0302 A/mm2	0 ~ 0.0004	0 A/mm2	99.0302 A/mm2	0~ 0.0004
Plane03 Layer	0 A/mm2	162.034 A/mm2	0 A/mm2	162.037 A/mm2	0 ~0.0019	0 A/mm2	162.037 A/mm2	0 ~0.0019
Bottom Layer	0 A/mm2	6.23648 A/mm2	0 A/mm2	6.23648 A/mm2	0 ~ 0	0 A/mm2	6.23648 A/mm2	0 ~ 0

Summary for Three-Die Package Temperature on PCB Layers

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	32.0426	77.0401C	30.5246C	74.7055C	-4.74 ~ -3.03	34.2308C	93.2286C	6.83 ~ 21.01
Plane02 Layer	32.0992C	75.1669C	30.5672C	69.0727	-4.77 ~ -8.11	34.302C	83.5966C	6.86 ~ 11.21
Plane03 Layer	32.1315C	74.5688C	30.5874C	68.882C	-4.81 ~-7.63	34.3357C	83.0437C	6.86 ~ 11.37
Bottom Layer	32.1018C	74.5513C	30.5639C	68.8673C	-4.79 ~ -7.62	34.2965C	83.0255C	6.84 ~ 11.22

Max Temperature on PCB Layers (Unit: ^{o}C)



PETM vs FEM

Maximum temperature difference: ~$6^{0}C$

2-R CTM vs FEM

Maximum temperature difference: ~$19^{0}C$

CONCLUSIONS

Single Die Package

- Component pin based electrical PETM model works very accurately for IR drop analysis
  - Almost same as FEM
- For small size or low pin count IC package
  - Both 2-R CTM and thermal PETM models work fine for thermal analysis (or E/T co-simulation) with high accuracy comparing to the FEM method
- For large size or high pin count IC package
  - 2-R CTM model does not work well for thermal analysis or E/T co-simulation but PETM models work fine

Multi-Chip Package

- Component pin based electrical PETM model works very accurately for IR drop analysis
  - Almost same as FEM
- For multi-chip IC package thermal analysis
  - 2-R CTM does not work well for thermal analysis (or E/T co-simulation)
  - PETM models work accurately for both thermal or E/T co-simulation for PCB systems