

EDI  
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2019

Electronic Design Innovation Conference  
电子设计创新大会

April 1-3, 2019  
China National Convention Center  
Beijing, China



# LDMOS Technology for 5 GHz Power Amplifiers

S.J.C.H. Theeuwen,  
H. Mollee, R. Heeres, and F. van Rijs

Ampleon Netherlands



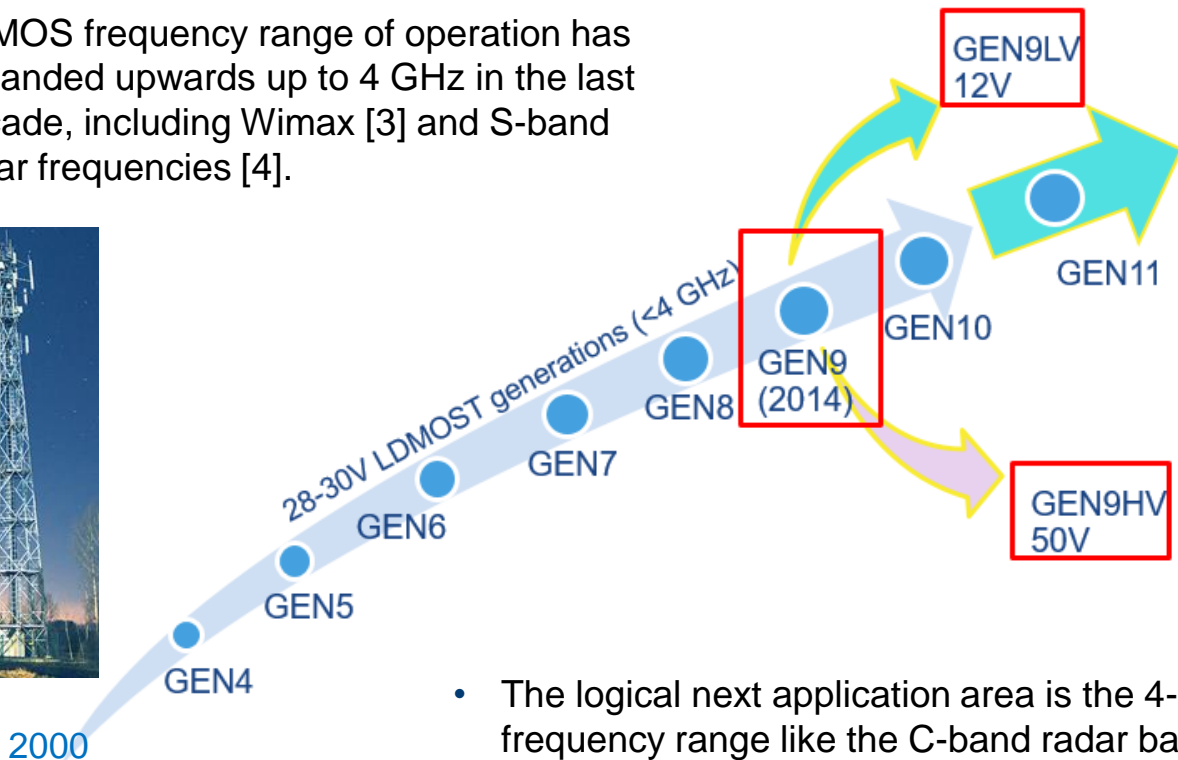
EDI CON 2019 Beijing  
April 2, 2019

# CONTENT OF THE PRESENTATION

- INTRODUCTION, LDMOS DEVICE TECHNOLOGY
- ON WAFER LOAD-PULL RF PERFORMANCE 1-12 GHZ
  - 30V LDMOS IN CLASS AB
  - 12V, 30V, 50V LDMOS COMPARISON IN CLASS AB
- ON WAFER LOAD-PULL RF PERFORMANCE 1-12 GHZ
  - 30V AND 50V LDMOS WITH 2<sup>ND</sup> HARMONIC OUTPUT OPTIMIZED
- LDMOS PRODUCT APPLICATION
  - C-BAND DEMONSTRATOR
- CONCLUSIONS

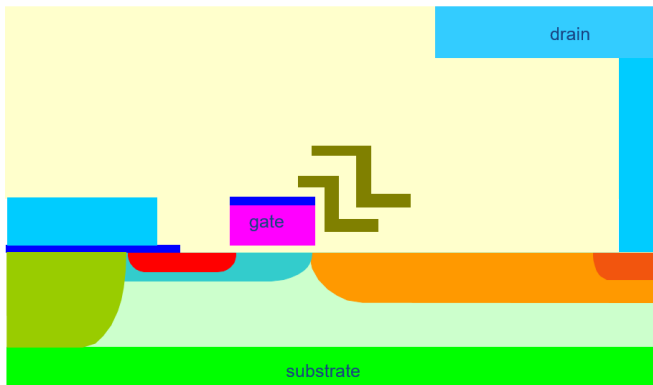
# INTRODUCTION

- LDMOS frequency range of operation has expanded upwards up to 4 GHz in the last decade, including Wimax [3] and S-band radar frequencies [4].



- The logical next application area is the 4-6 GHz frequency range like the C-band radar band and future 5G Base station bands.

# LDMOS DEVICE TECHNOLOGY

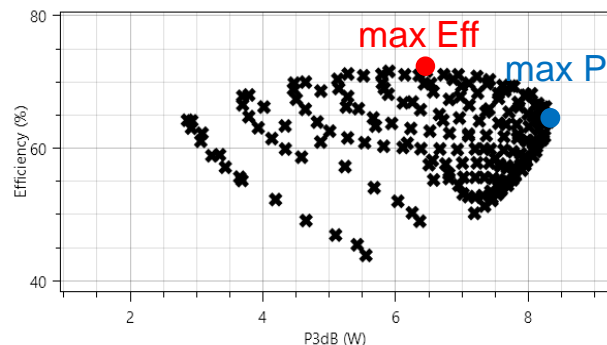
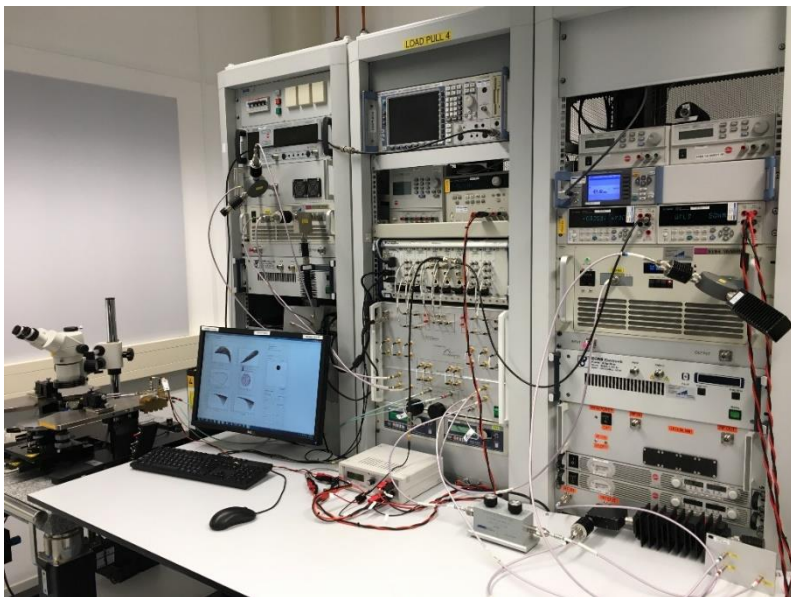


Key parameters	12V LDMOS	30V LDMOS	50V LDMOS
BVdss (V)	40	70	120
Rdson ( $\Omega$ .mm)	8	12	23
Vth (V)	2.0	2.0	2.0
Cds (Vsupply) (pF/mm)	0.33	0.25	0.30
Cgs (0) (pF/mm)	0.9	0.9	0.9
Cgd (Vsupply) (fF/mm)	16	10	3
f <sub>T</sub> (GHz)	15	15	14

- LDMOS has a proven reliability record for many applications, e.g. more than 20yr life time for base station applications.

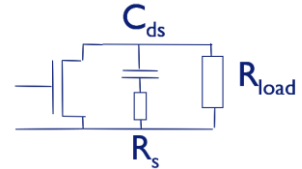
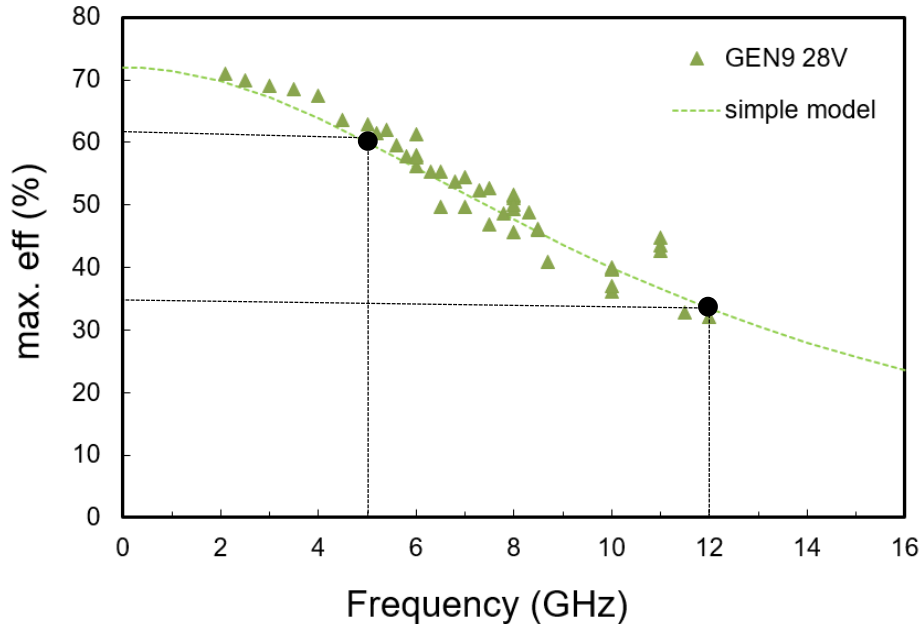
[1] S.J.C.H. Theeuwes, J.H. Qureshi, LDMOS technology for RF power amplifiers, IEEE Transactions On Microwave Theory and Techniques (special issue on Power Amplifiers), Volume 60, Issue 6, Part 2, pp. 1755-1763 (2012)

# ON WAFER LOAD-PULL RF MEASUREMENTS



- To explore the intrinsic RF performance up to high frequencies, we use on-wafer Ground-Signal-Ground (GSG) structures with power levels of 5-10W.
- We force class (A)B operation by shorting the output harmonics up to 12 GHz.

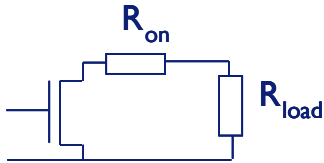
# ON WAFER LOAD-PULL: MAXIMUM EFFICIENCY IN CLASS AB



$$Eff(\%) = 78.5\% \cdot \frac{1}{1 + \omega^2 C_{ds}^2 R_s R_{load}}$$

- The frequency roll-off is due to output capacitance losses.
- 63% at 5 GHz
- 35% at 12 GHz

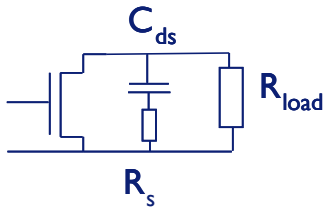
# MAXIMUM EFFICIENCY THEORY



$$Eff (\%) = 78.5\% \cdot \frac{1}{1 + 2R_{on} / R_{load}}$$

LDMOS  $R_{on}$ : Eff=72%

$$R_{load} \sim \frac{V_{swing}}{I_{swing}} \text{ or } R_{load} = \frac{V_{sup}^2}{2P_{dens}}$$



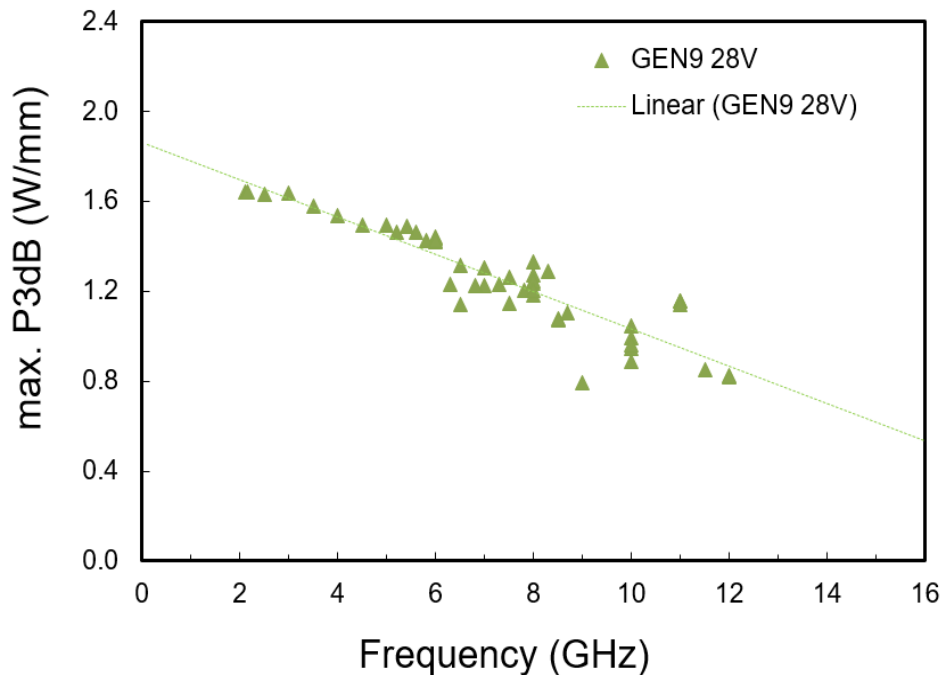
$$Eff (\%) = 78.5\% \cdot \frac{1}{1 + \omega^2 C_{ds}^2 R_s R_{load}}$$

Class AB: 78.5%

Class E: 100%

[2] F. van Rijs, and S.J.C.H. Theeuwes, "Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit," International Electron Device Meeting IEDM, 2006, pp. 205-208

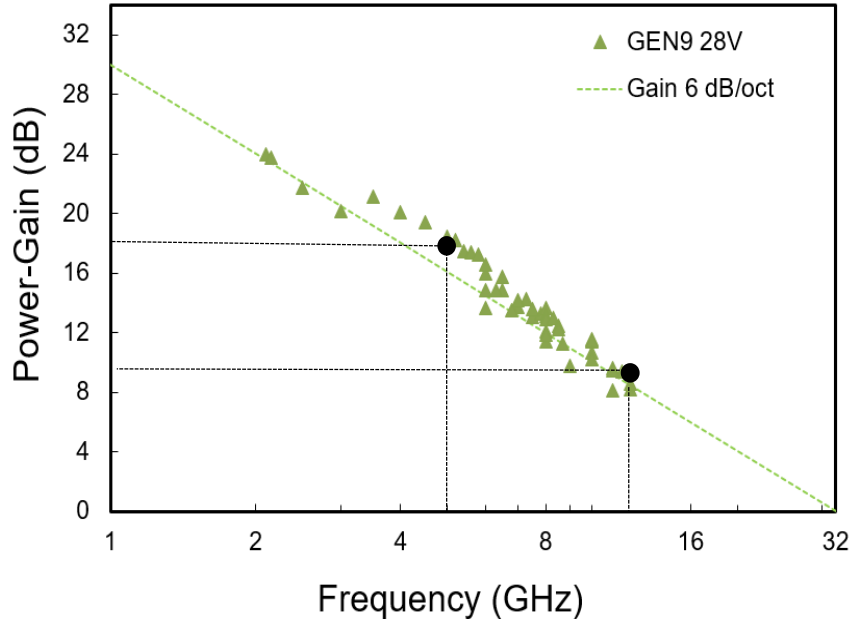
# ON WAFER LOAD-PULL: MAXIMUM POWER DENSITY



- At 12 GHz, the power density is still around 1 W/mm.



# ON WAFER LOAD-PULL: GAIN FOR MAX POWER LOAD

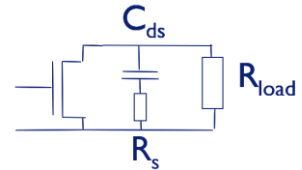
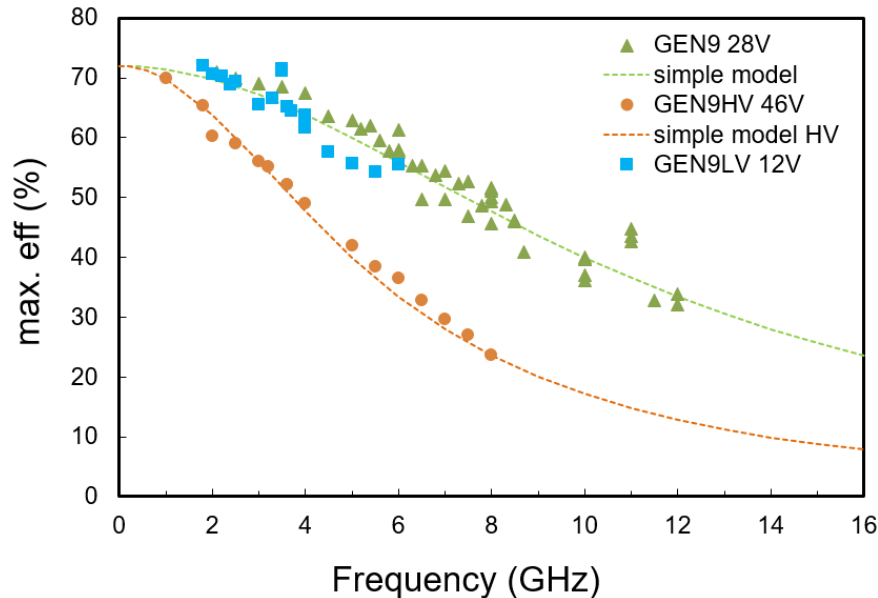


- 18dB at 5 GHz
- 10dB at 12 GHz
- The 0dB frequency is around 30 GHz
- This is much higher than the cut-off frequency of 15 GHz due to additional voltage/ impedance amplification.

# ON WAFER LOAD-PULL RF PERFORMANCE

COMPARISON OF SEVERAL LDMOS NODES

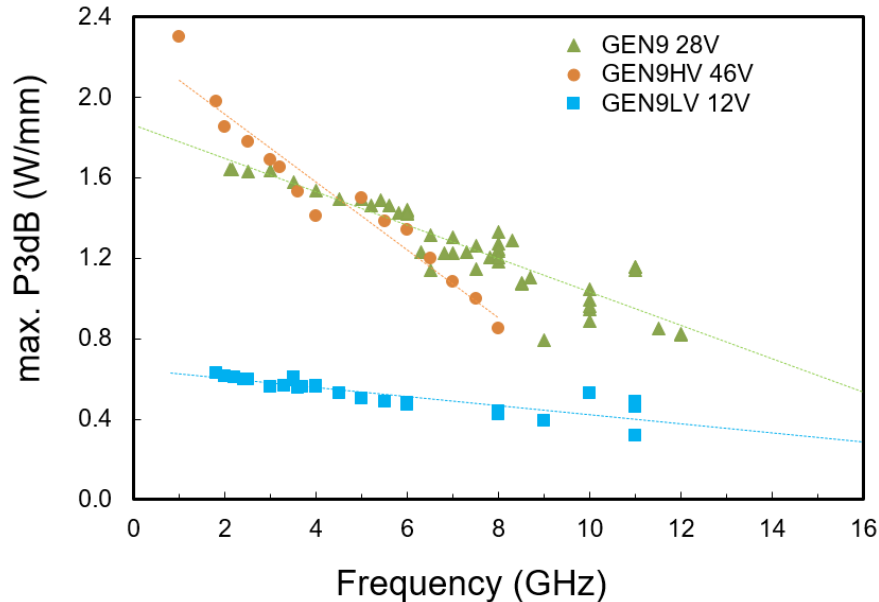
# ON WAFER LOAD-PULL: MAXIMUM EFFICIENCY IN CLASS AB



$$Eff(\%) = 78.5\% \cdot \frac{1}{1 + \omega^2 C_{ds}^2 R_s R_{load}}$$

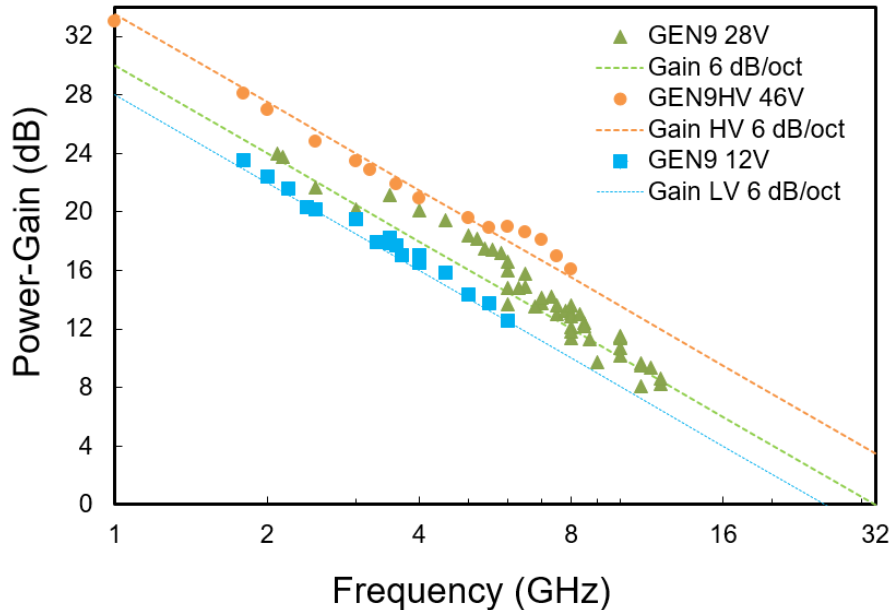
- For the frequency roll-off of the efficiency we see more losses for the 50V node.

# ON WAFER LOAD-PULL: MAXIMUM POWER DENSITY



- The power density scales with supply voltage at the low frequency limit

# ON WAFER LOAD-PULL: GAIN FOR MAX POWER LOAD



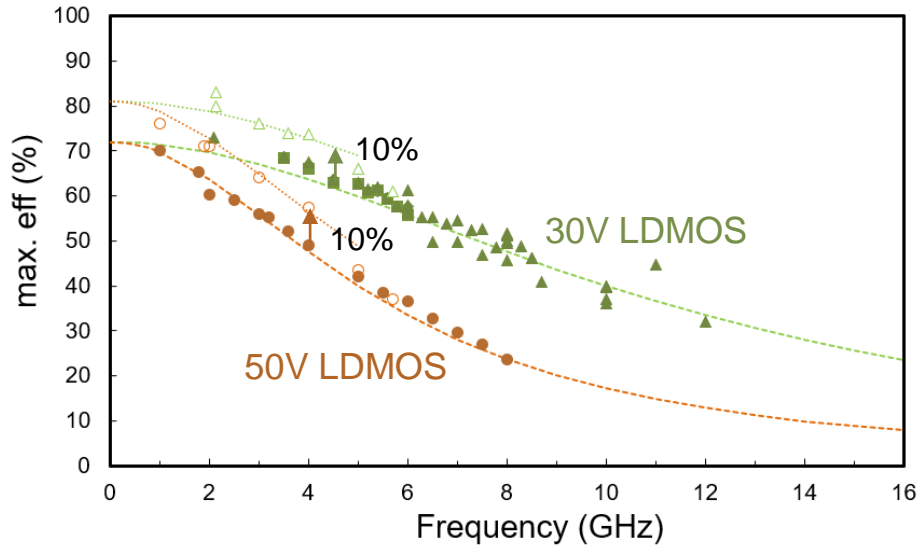
- The cut-off frequency is similar for all technologies, so the additional voltage/impedance amplification explains the gain offset.

# ON WAFER LOAD-PULL RF PERFORMANCE

OUTPUT 2<sup>ND</sup> HARMONIC OPTIMIZED FOR 30V AND 50V LDMOS

# ON WAFER LOAD-PULL: MAXIMUM EFFICIENCY

## OUTPUT 2<sup>ND</sup> HARMONIC OPTIMIZED FOR 30V AND 50V LDMOS



- Optimizing the second harmonic load impedance brings 10% extra efficiency for both 30V and 50V LDMOS

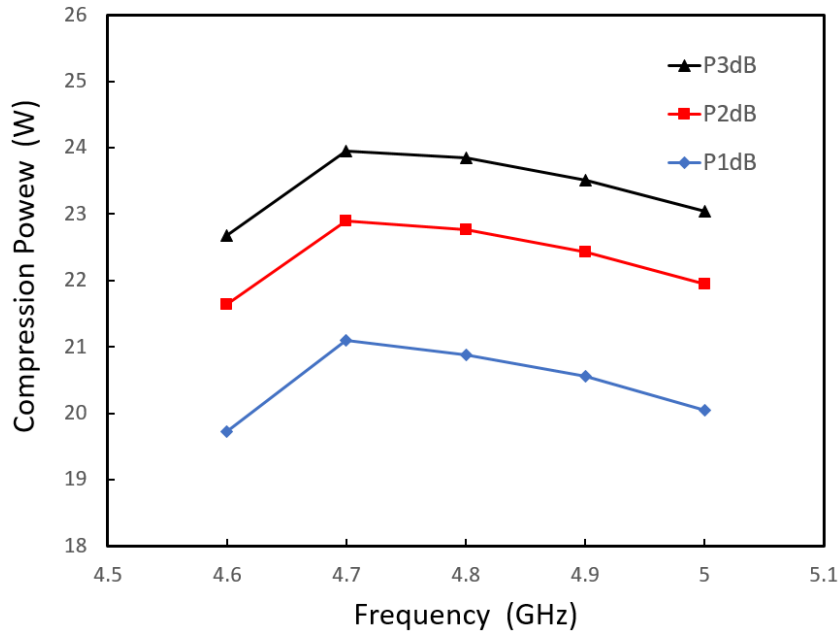
## C-band demo BLCF9G4650L(S)-20 GEN9-30V

BROAD BAND DEMONSTRATOR OF >20W FROM 4.6-5.0 GHZ



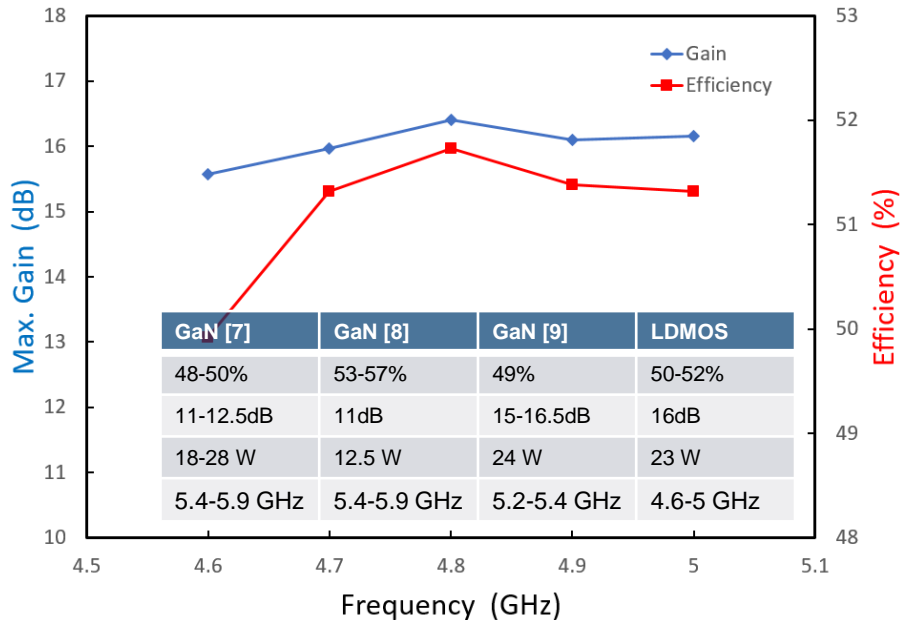


# C-BAND DEMONSTRATOR



- The demo is tuned for gain flatness and has over the entire band 23-24W in 3dB compression.

# C-BAND DEMONSTRATOR



- We achieve a maximum linear gain of 16 dB in combination with 50-52% efficiency
- If we compare the broadband performance to GaN datasheet performance numbers [7,8,9] we see for LDMOS similar efficiencies, and much higher gain

[7] Qorvo GaN data sheet T2G6003028-FS  
[8] Wolfspeed GaN data sheet CGH55015F2  
[9] Sumitomo GaN data sheet SGK5254-30A-R

# CONCLUSIONS

- We have shown that LDMOS technology has good performance at higher frequencies 5-12 GHz, especially the 30V node.
- The intrinsic 30V LDMOS, measured by on-wafer load pull, has
  - at 2 GHz an efficiency of 72%, and 25dB gain; or 83% after 2<sup>nd</sup> harmonic optimization
  - at 5 GHz an efficiency of 63%, and 19dB gain.
  - at 12 GHz an efficiency of 35%, and 10dB gain.
- We show a 23W C-band demonstrator. In this demo circuit LDMOS shows at 4.6-5.0 GHz
  - 51% efficiency, 16dB linear gain.
- This good RF performance in combination with the proven reliability record shows the capabilities of LDMOS at 5 GHz frequencies, and in particular for C band radar applications and for the future 5G Base station applications.

Thank you for your attention

**S.J.C.H. Theeuwes, H. Mollee, R. Heeres, and F. van Rijs**

*LDMOS technology for power amplifiers up to 12 GHz*, Proceedings of the 13<sup>th</sup> European Microwave Integrated Circuits Conference, pp. 162-165 (2018)