Demystifying 5G

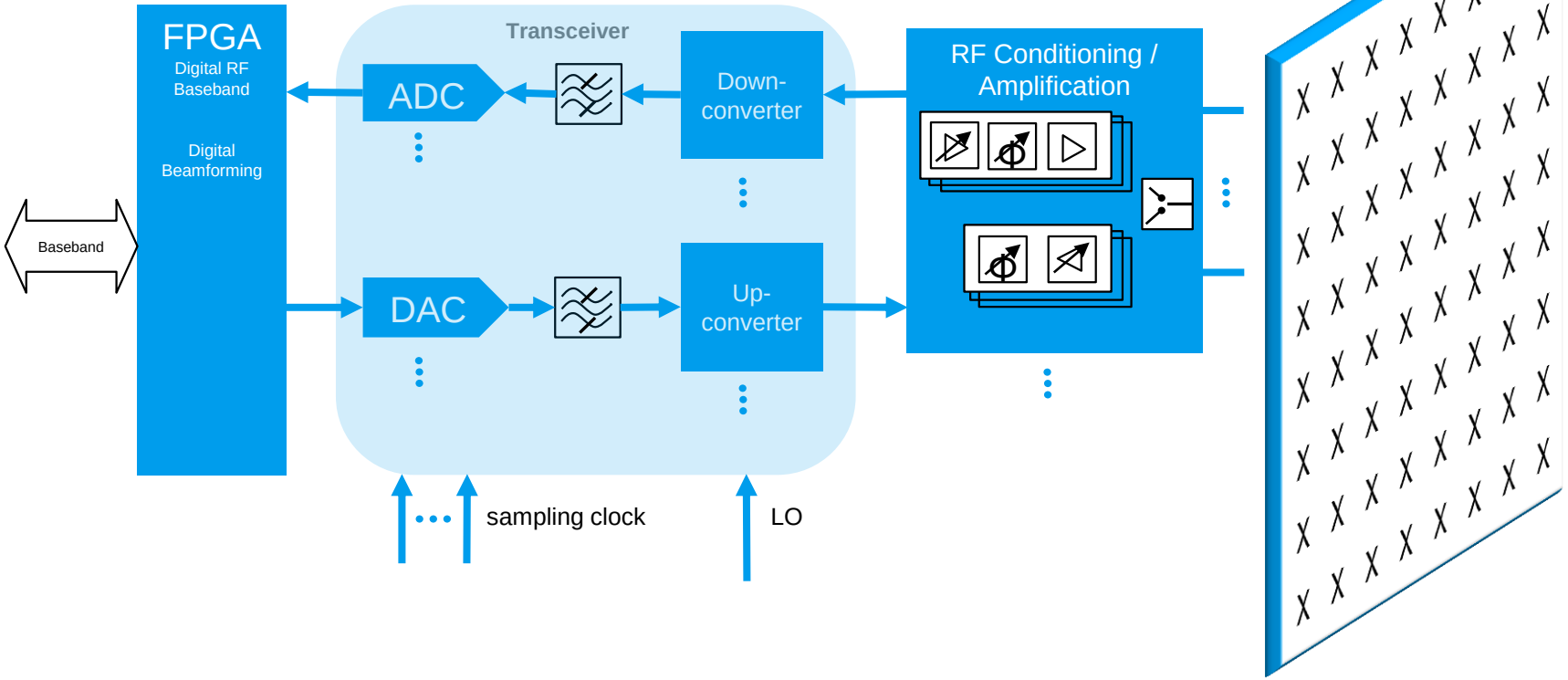
Clock and LO Architectures in 5G Base Stations
- Phase Noise Performance, Output Power

Martin Stumpf - Market Segment Manager, R&S
Steven Gutierrez - Application Manager, IDT
Greg Bonaguide - Application Engineer, R&S

ROHDE&SCHWARZ

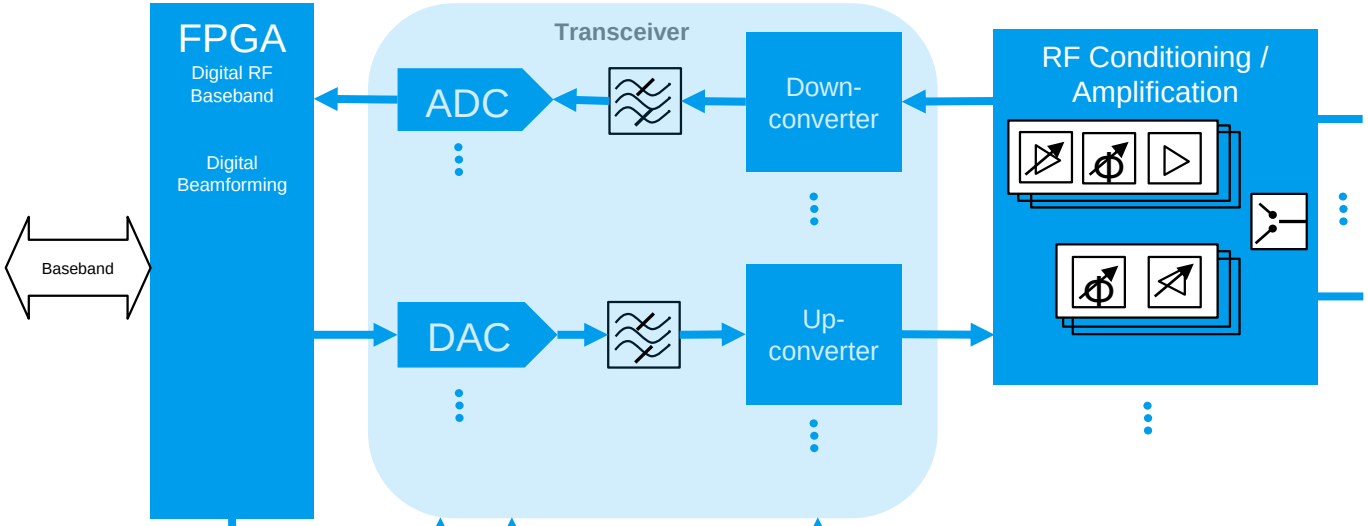
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



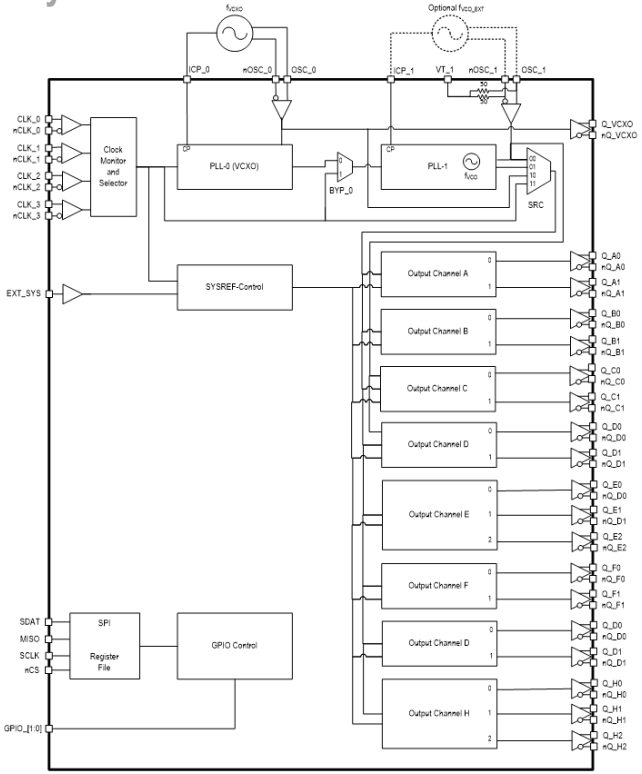
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- **Output Power and Phase Noise Performance**
- Spur Suppression
- Jitter Attenuation
- Signal Waveform Quality and LO Skew
- Delay Resolution, Clock Skew and Timing
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

8V19N880 Clock Generator / Jitter Attenuator

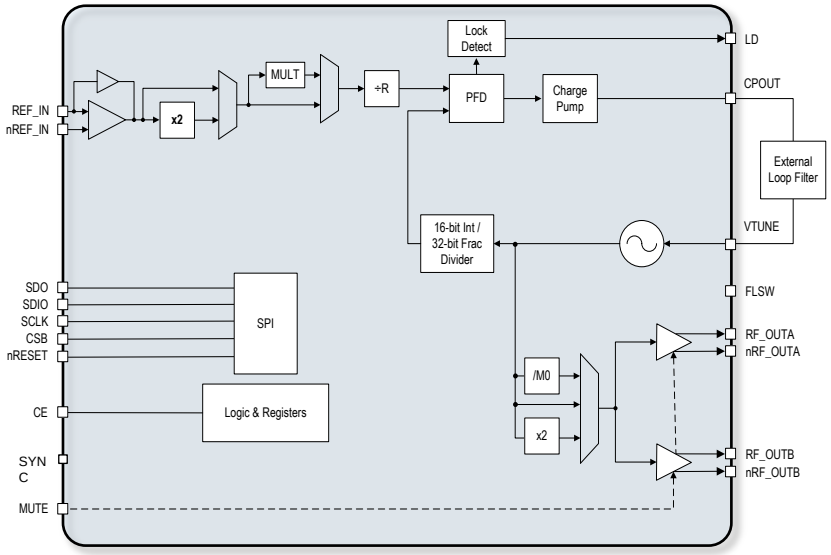
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

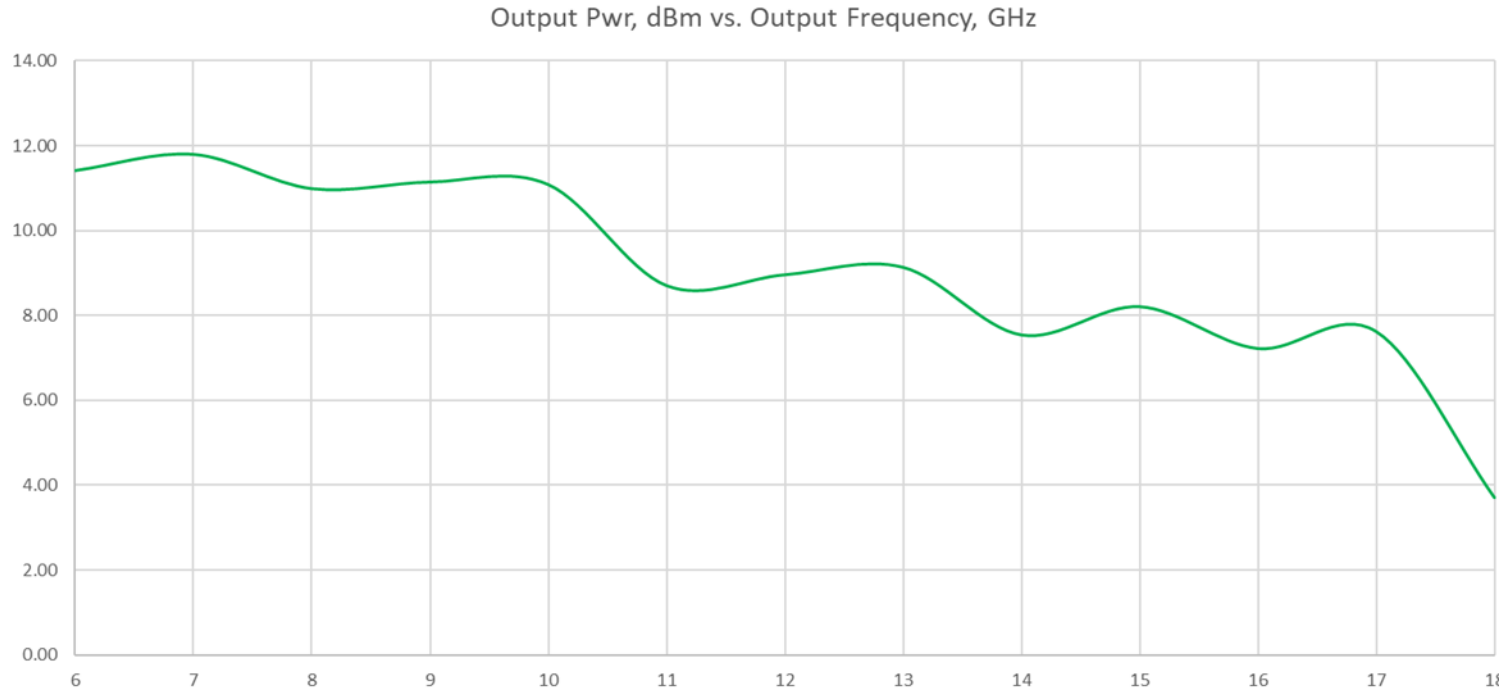
8V97003 18GHz Microwave Synthesizer

Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

RF Synthesizer Output Power versus Frequency (M1)

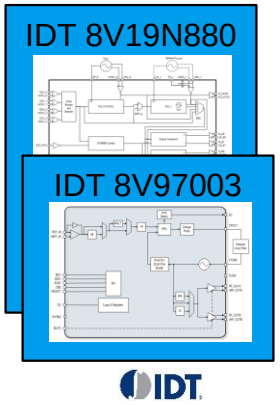


- Inductively loaded terminations, single-ended; double terminated load

Output Power and Phase Noise Performance

IDT 8V19N880 Clock Generator / Jitter Attenuator; IDT 8V97003 18GHz Microwave Synthesizer

122.88MHz



...

Balun

R&S SMA100B
- 8kHz to 3 / 6 / 12.75 / 20GHz
- options for high and ultra high output power
- superior spectral purity:
  - ultra-low phase noise and wideband noise with several performance options
  - low harmonics, subharmonics and nonharmonics
- analog modulation (optional):
  - AM, PM, FM
- optional clock synthesizer:
  - single-ended or differential output
  - sine-wave or square wave signal

R&S FSWP
- 1MHz to 8GHz, 26.5GHz, 50GHz
- high phase noise sensitivity
- options to further improve phase noise sensitivity by cross-correlation
- built-in spectrum analyzer (option)
- options for signal demodulation
- built-in low phase noise signal source and additive phase noise method (option)

Demystifying 5G

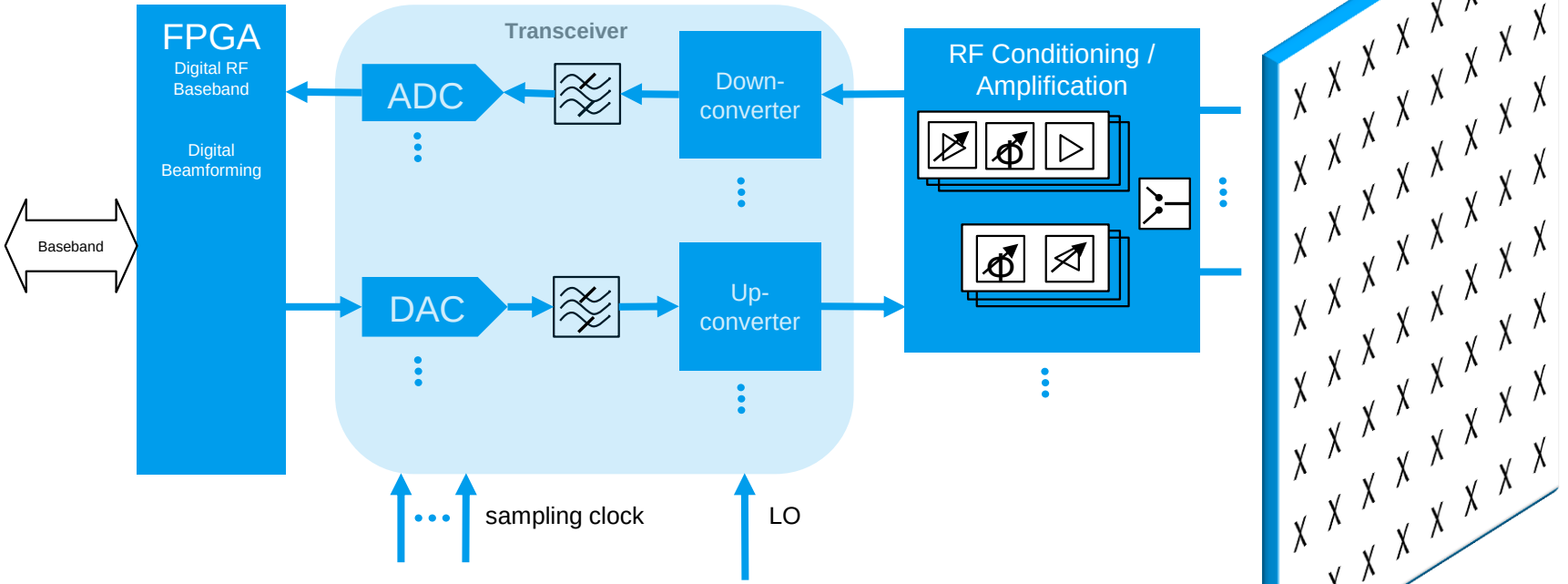
Clock and LO Architectures in 5G Base Stations
- Spur Suppression

Martin Stumpf - Market Segment Manager, R&S
Steven Gutierrez - Application Manager, IDT
Greg Bonaguide - Application Engineer, R&S

ROHDE&SCHWARZ

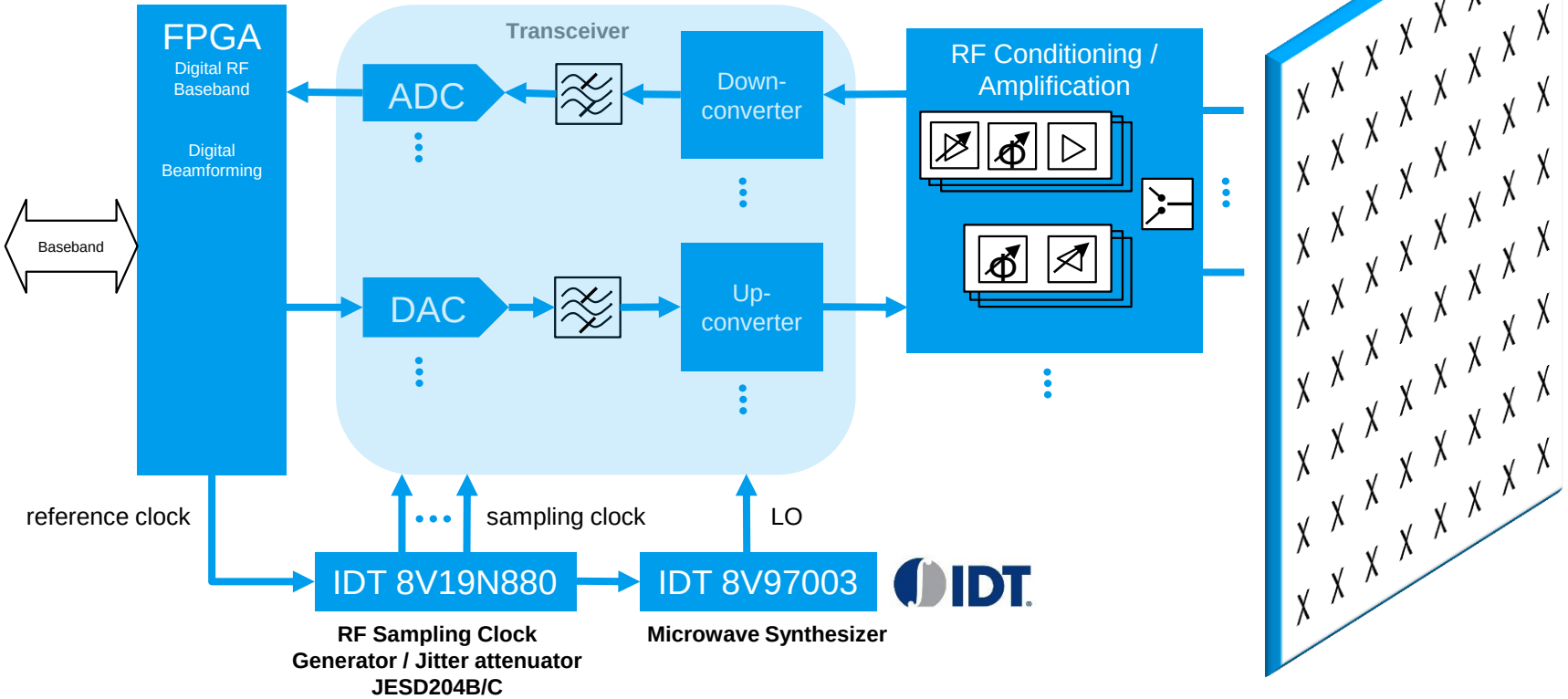
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



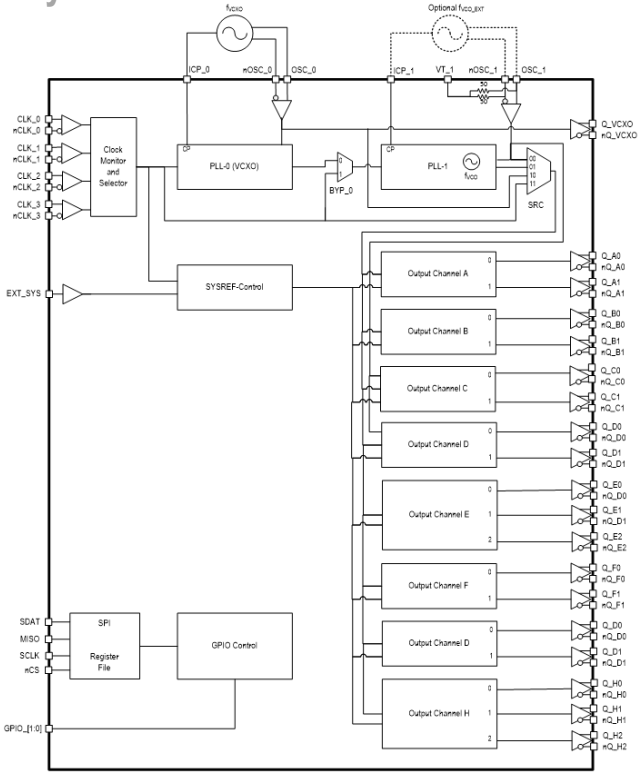
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- Output Power and Phase Noise Performance
- **Spur Suppression**
- Jitter Attenuation
- Signal Waveform Quality and LO Skew
- Delay Resolution, Clock Skew and Timing
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

IDT 8V19N880 Clock Generator / Jitter Attenuator

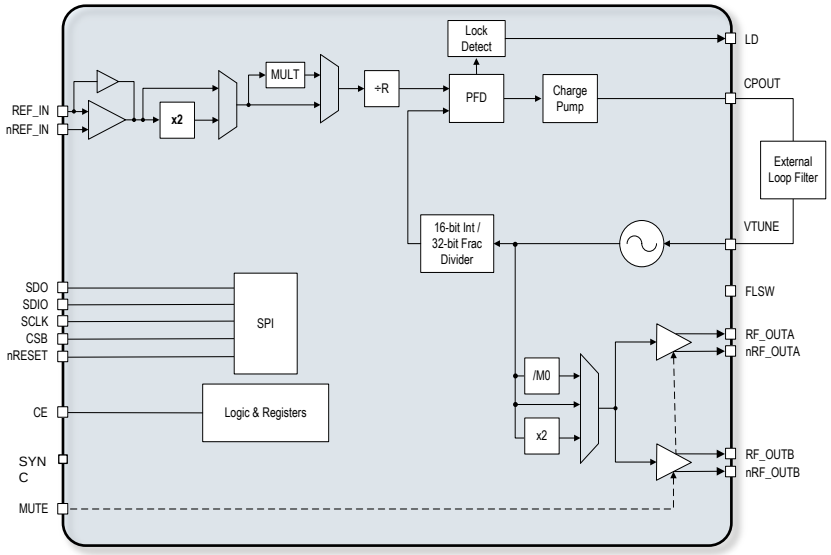
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

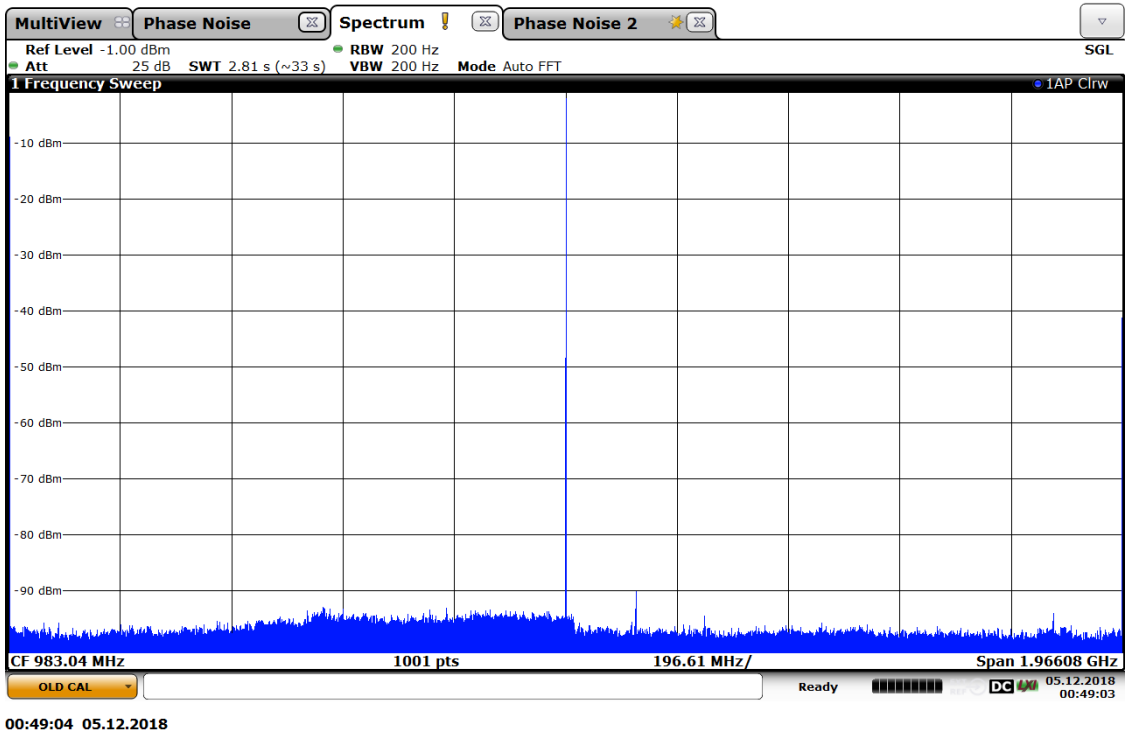
8V97003 18GHz Microwave Synthesizer

Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

IDT 8V19N880 Output Spectrum (M1)

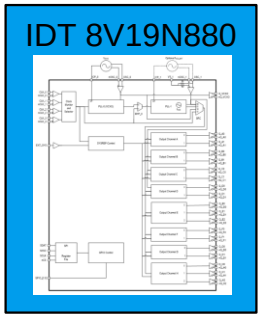


- 8V19N880 893.04MHz clock output
- Spurious reduced to -90dBm (dBc?)
- Improves data converter characteristics

Spur Suppression

IDT 8V19N880 Clock Generator

122.88MHz



clock 1: 983.04MHz

Balun

R&S SMA100B

- 8kHz to 3 / 6 / 12.75 / 20GHz
- options for high and ultra high output power
- superior spectral purity:
  - ultra-low phase noise and wideband noise with several performance options
  - low harmonics, subharmonics and nonharmonics
- analog modulation (optional):
  - AM, PM, FM
- optional clock synthesizer:
  - single-ended or differential output
  - sine-wave or square wave signal

R&S FSWP

- 1MHz to 8GHz, 26.5GHz, 50GHz
- high phase noise sensitivity
- options to further improve phase noise sensitivity by cross-correlation
- built-in spectrum analyzer (option)
- options for signal demodulation
- built-in low phase noise signal source and additive phase noise method (option)

Demystifying 5G

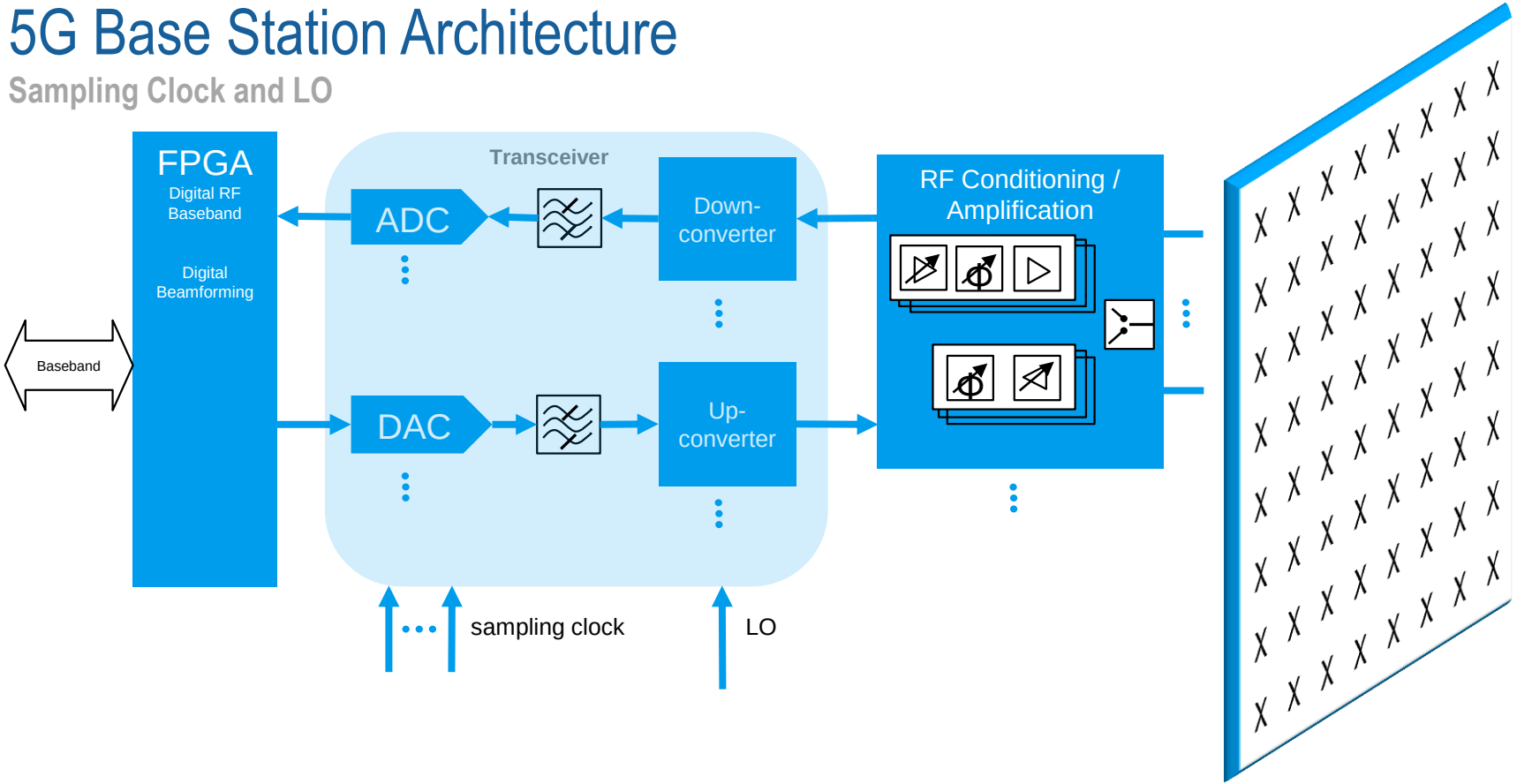
Clock and LO Architectures in 5G Base Stations
- Jitter Attenuation

Martin Stumpf - Market Segment Manager, R&S
Steven Gutierrez - Application Manager, IDT
Greg Bonaguide - Application Engineer, R&S

ROHDE&SCHWARZ

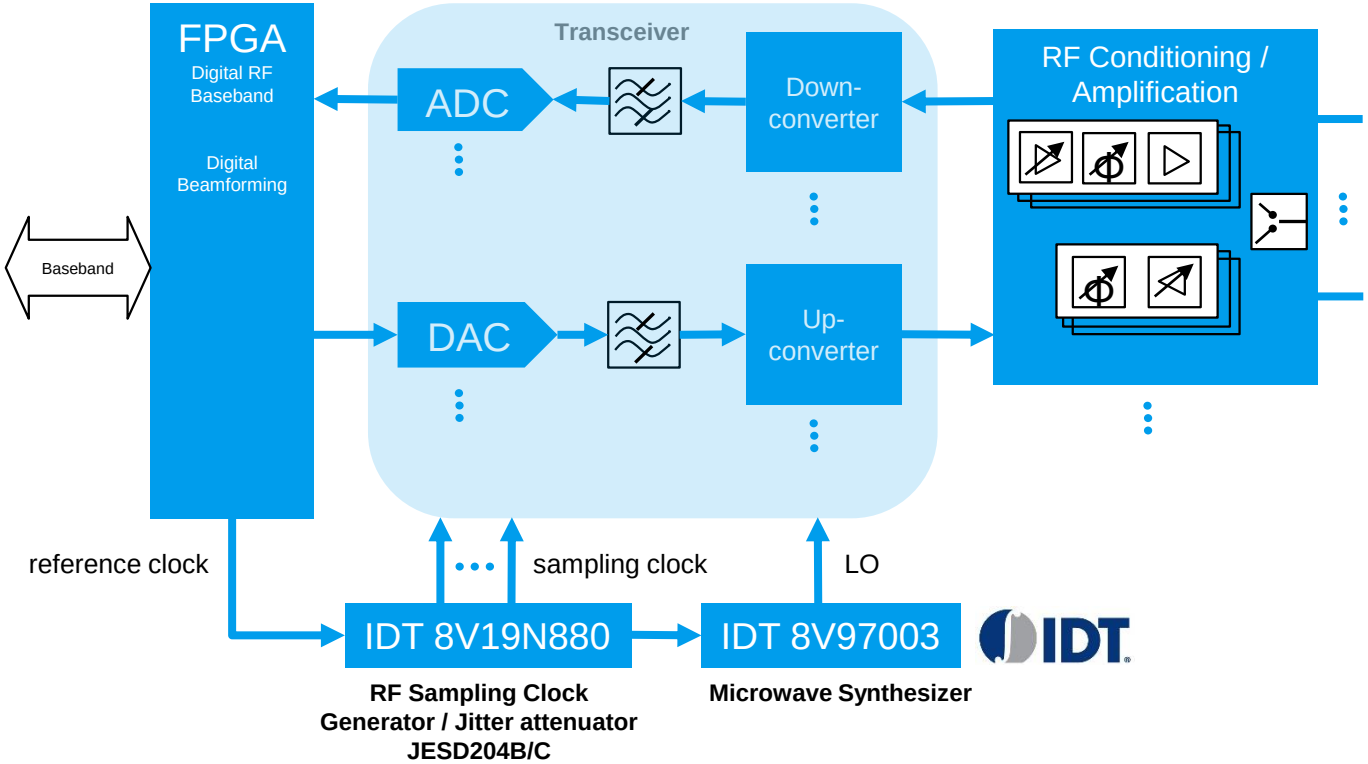
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



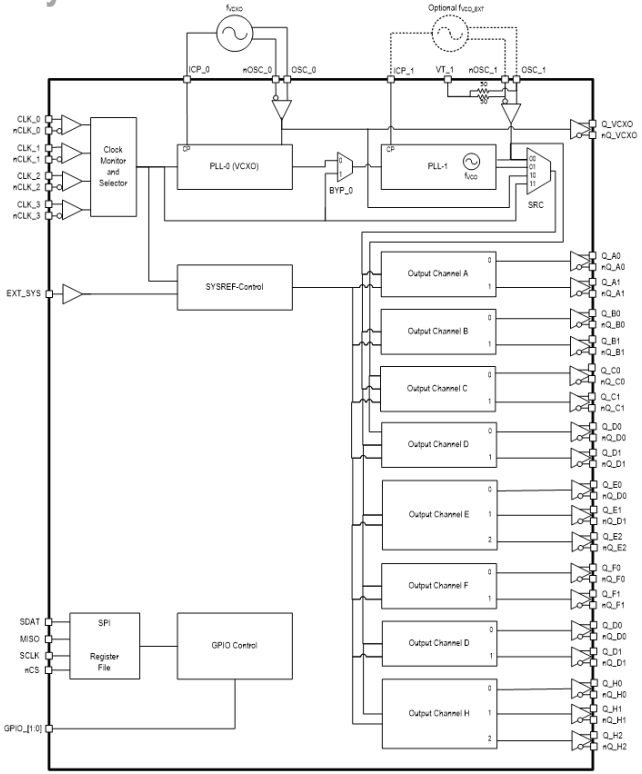
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- Output Power and Phase Noise Performance
- Spur Suppression
- **Jitter Attenuation**
- Signal Waveform Quality and LO Skew
- Delay Resolution, Clock Skew and Timing
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

IDT 8V19N880 Clock Generator / Jitter Attenuator

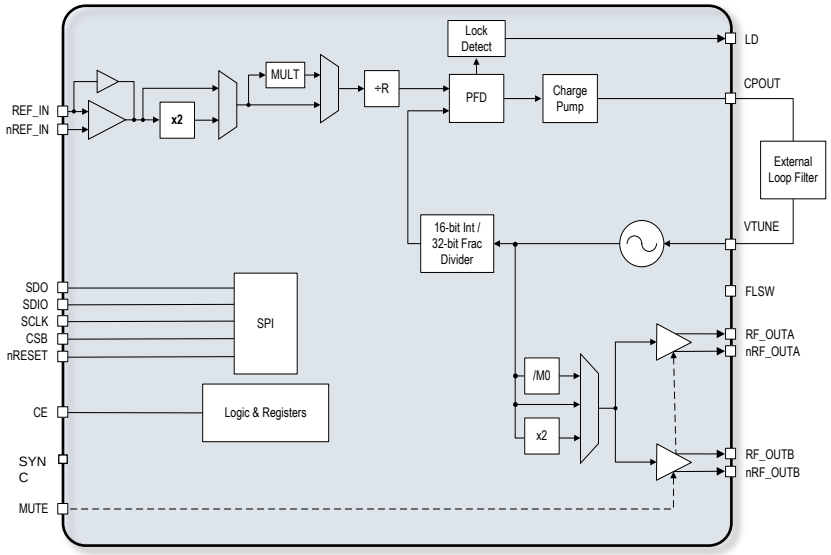
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

8V97003 18GHz Microwave Synthesizer

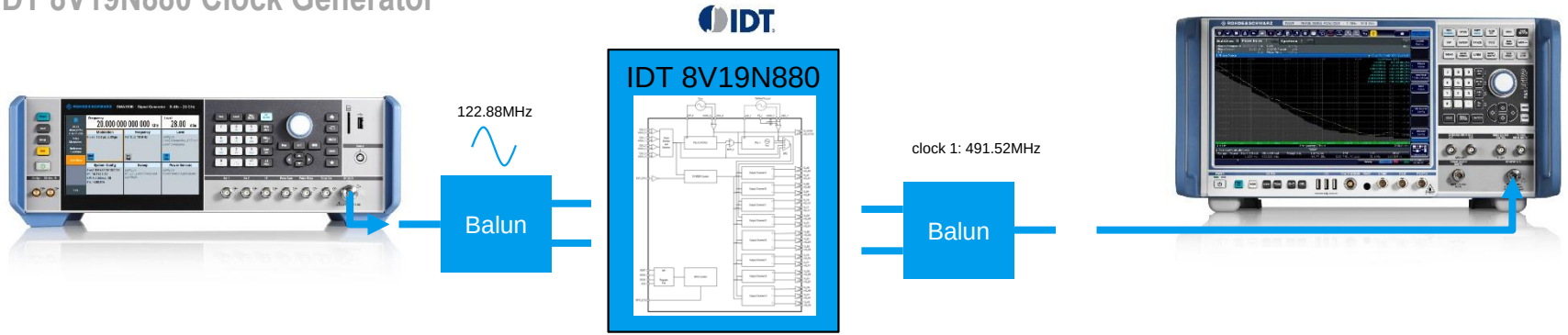
Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

Jitter Attenuation (M2)

IDT 8V19N880 Clock Generator



R&S SMA100B

- 8kHz to 3 / 6 / 12.75 / 20GHz
- options for high and ultra high output power
- superior spectral purity:
  - ultra-low phase noise and wideband noise with several performance options
  - low harmonics, subharmonics and nonharmonics
- analog modulation (optional):
  - AM, PM, FM
- optional clock synthesizer:
  - single-ended or differential output
  - sine-wave or square wave signal

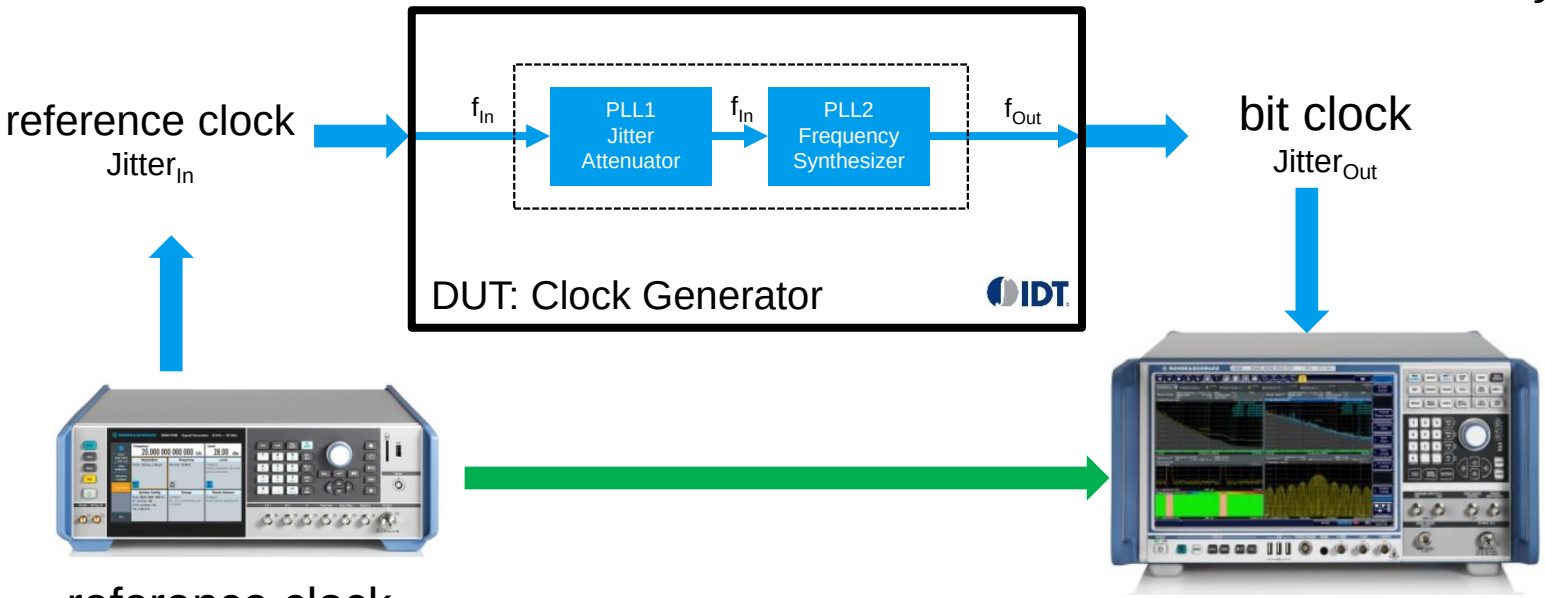
R&S FSWP

- 1MHz to 8GHz, 26.5GHz, 50GHz
- high phase noise sensitivity
- options to further improve phase noise sensitivity by cross-correlation
- built-in spectrum analyzer (option)
- options for signal demodulation
- built-in low phase noise signal source and additive phase noise method (option)

Jitter Transfer Function (JTF)

Setup with FSWP and Signal Source SMA100B

$$JTF = 20 \log \frac{Jitter_{Out}}{Jitter_{In}}$$



reference clock
with artificial jitter
→ PM modulation

Phase noise measurement:
1.) Calibration
2.) Measurement

Demystifying 5G

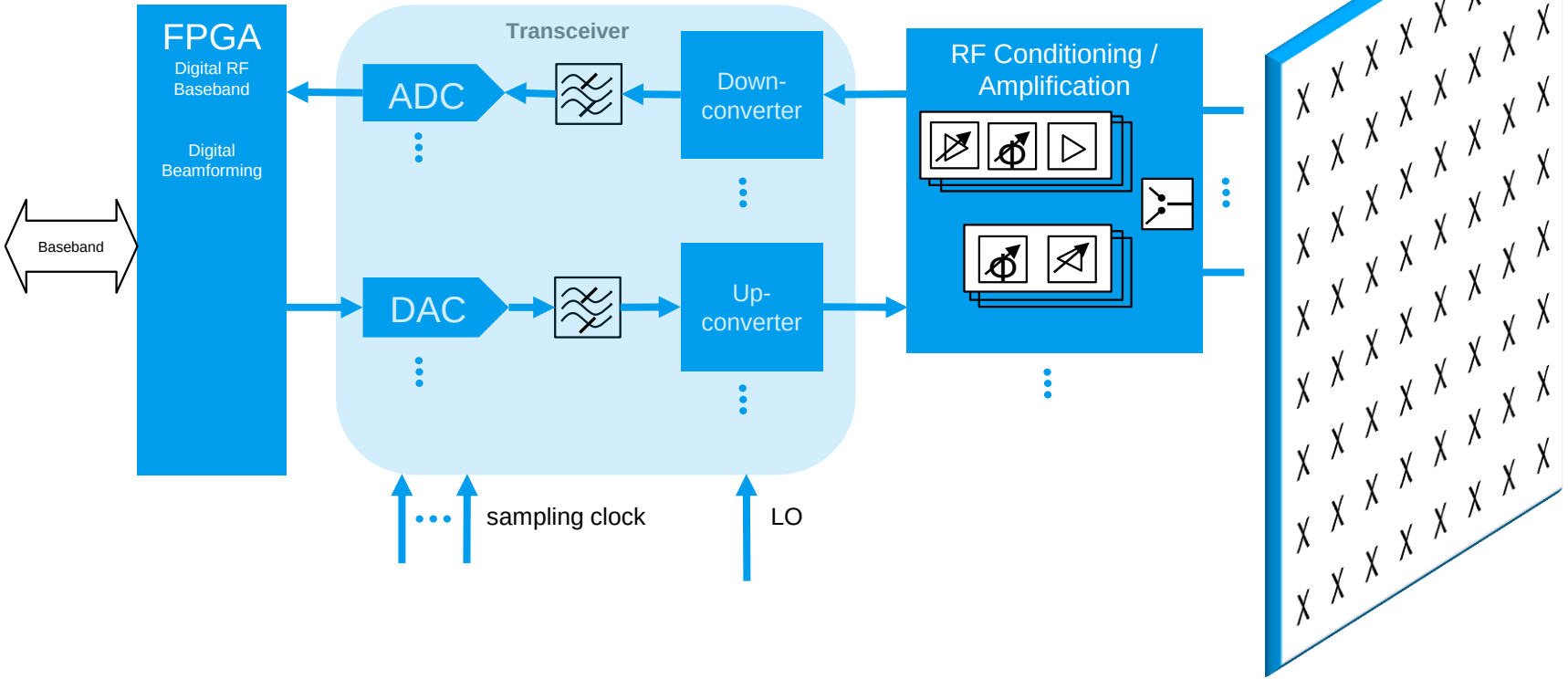
Clock and LO Architectures in 5G Base Stations
- Signal Waveform Quality and LO Skew

Martin Stumpf - Market Segment Manager, R&S
Steven Gutierrez - Application Manager, IDT
Mathias Hellwig - Application Engineer, R&S

ROHDE&SCHWARZ

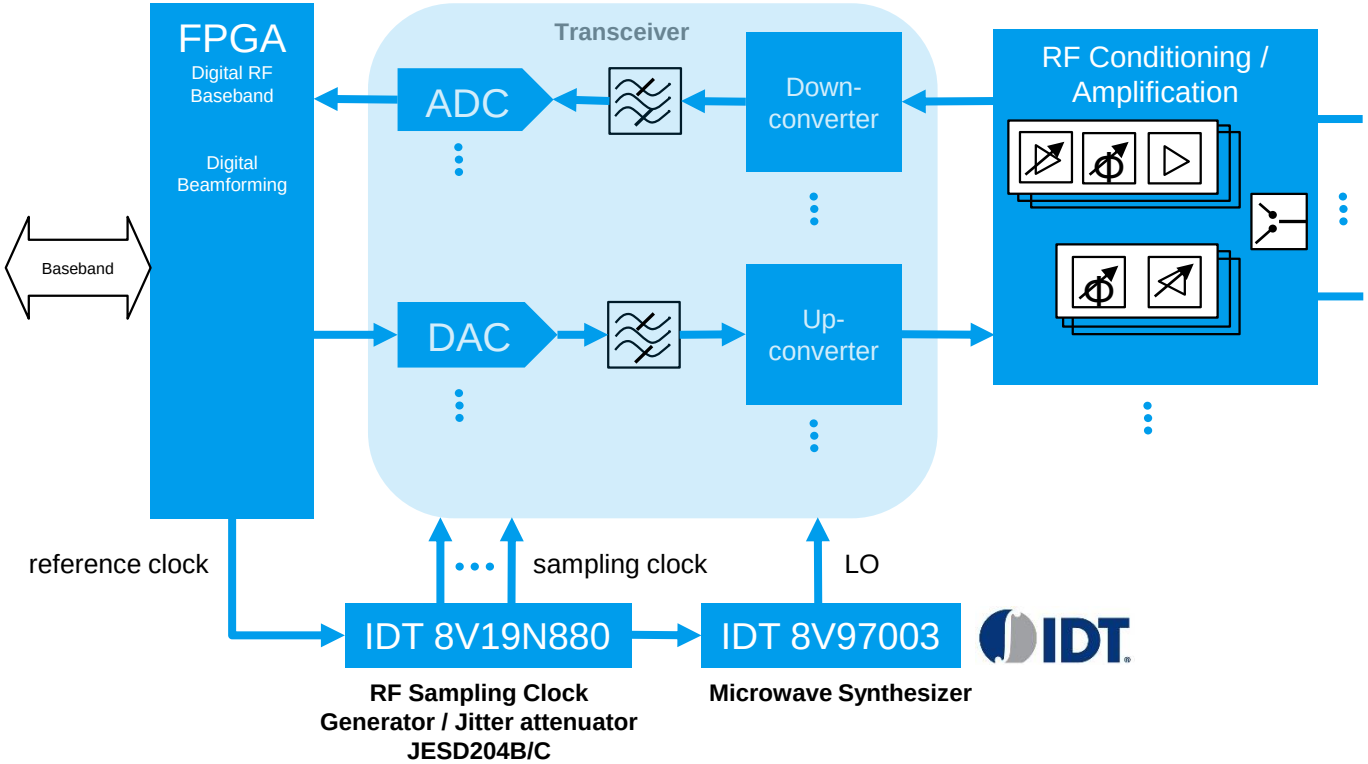
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



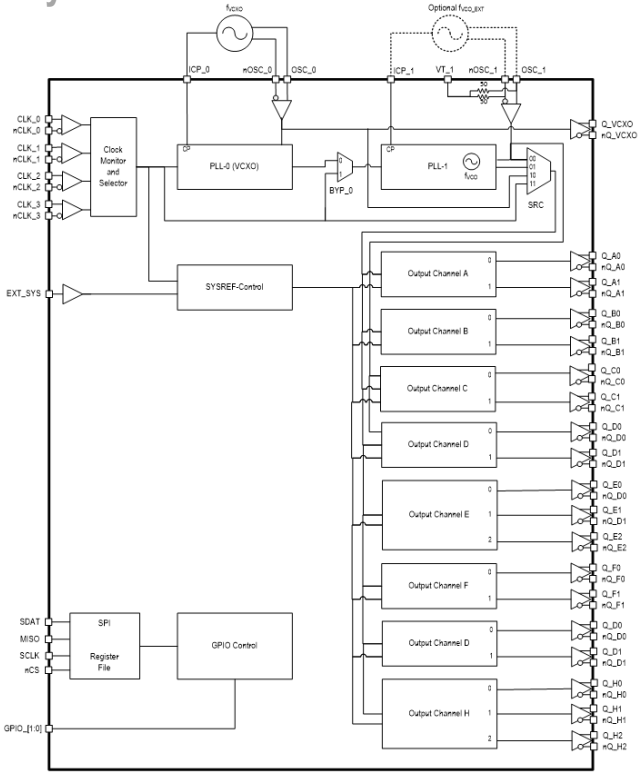
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- Output Power and Phase Noise Performance
- Spur Suppression
- Jitter Attenuation
- **Signal Waveform Quality and LO Skew**
- Delay Resolution, Clock Skew and Timing
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

IDT 8V19N880 Clock Generator / Jitter Attenuator

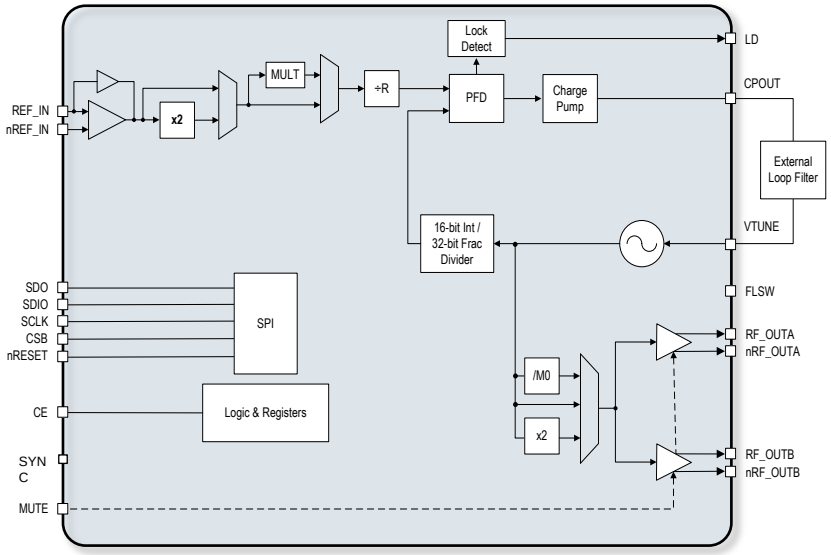
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

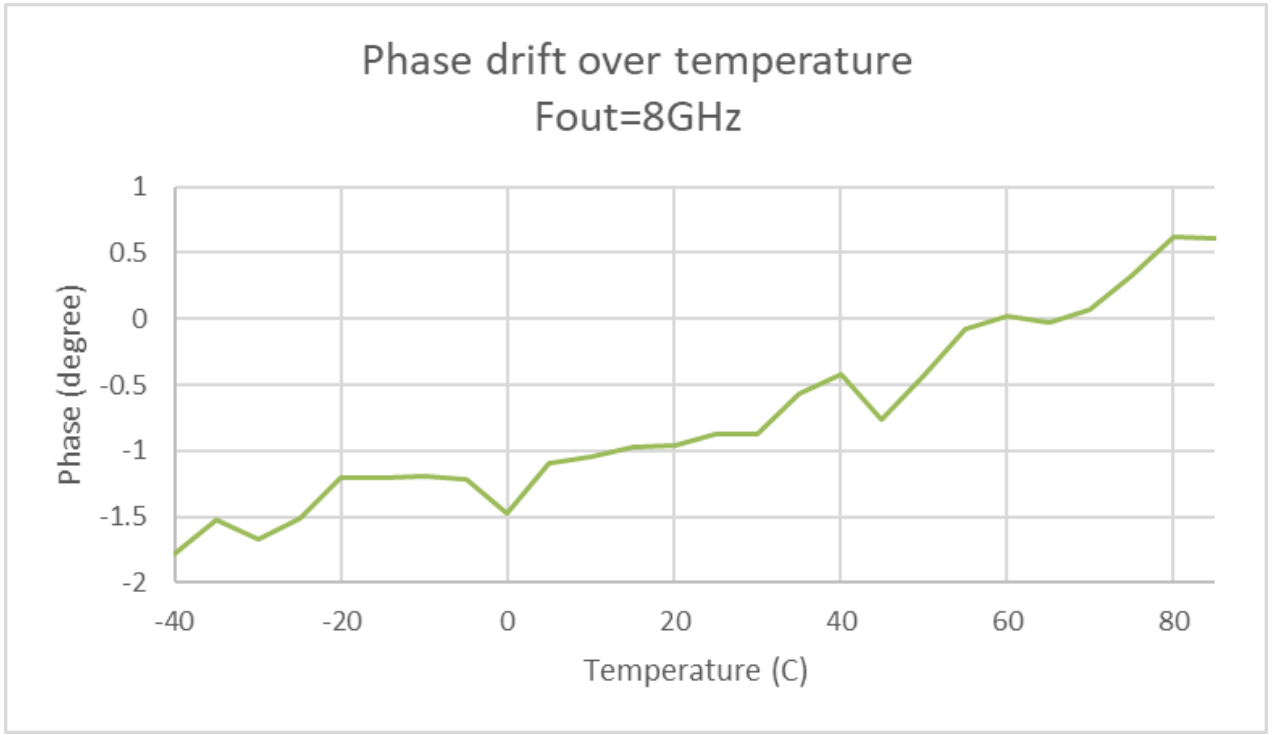
8V97003 18GHz Microwave Synthesizer

Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

IDT 8V97003 Low Output Skew Drift vs. Temperature

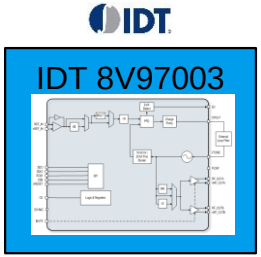


- 8V97003 output to output skew drift at 8GHz
- Low skew drift over full temperature range
- Input to output skew drift shows similar characteristics
- Supports reducing the number of radio path recalibrations events in beamforming applications

Signal Waveform Quality and LO Skew (M3)

IDT 8V97003 18GHz Microwave Synthesizer

122.88MHz



Clock 1: 8GHz
Clock 2: 8GHz

R&S SMA100B

- 8kHz to 3 / 6 / 12.75 / 20GHz
- options for high and ultra high output power
- superior spectral purity:
  - ultra-low phase noise and wideband noise with several performance options
  - low harmonics, subharmonics and nonharmonics
- analog modulation (optional):
  - AM, PM, FM
- optional clock synthesizer:
  - single-ended or differential output
  - sine-wave or square wave signal

R&S RTP

- available bandwidths: 4 / 6 / 8GHz
- channels: 4
- sample rate: 20Gsamples/s
- high-class analog performance
- fastest acquisition rate: 1,000,000 wfms/s
- real-time deembedding
- digital trigger up to full bandwidth
- multi-domain functionality, incl.:
  - digital interface test
  - spectrum and signal analysis
  - power integrity
  - …

Demystifying 5G

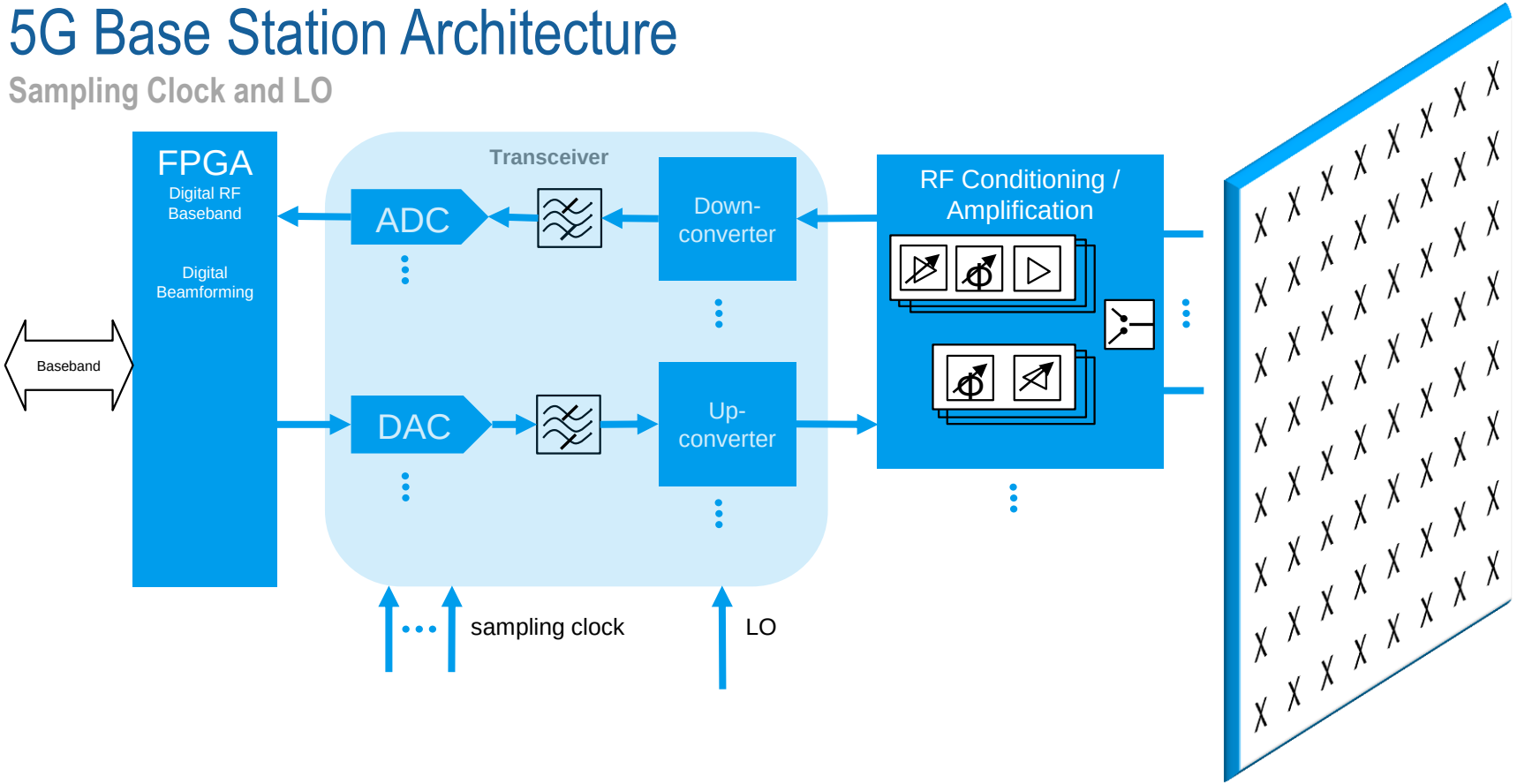
Clock and LO Architectures in 5G Base Stations
- Delay Resolution, Clock Skew and Timing

(Martin Stumpf - Market Segment Manager, R&S)
Steven Gutierrez - Application Manager, IDT
Greg Bonaguide - Application Engineer, R&S
Mathias Hellwig - Application Engineer, R&S

ROHDE&SCHWARZ

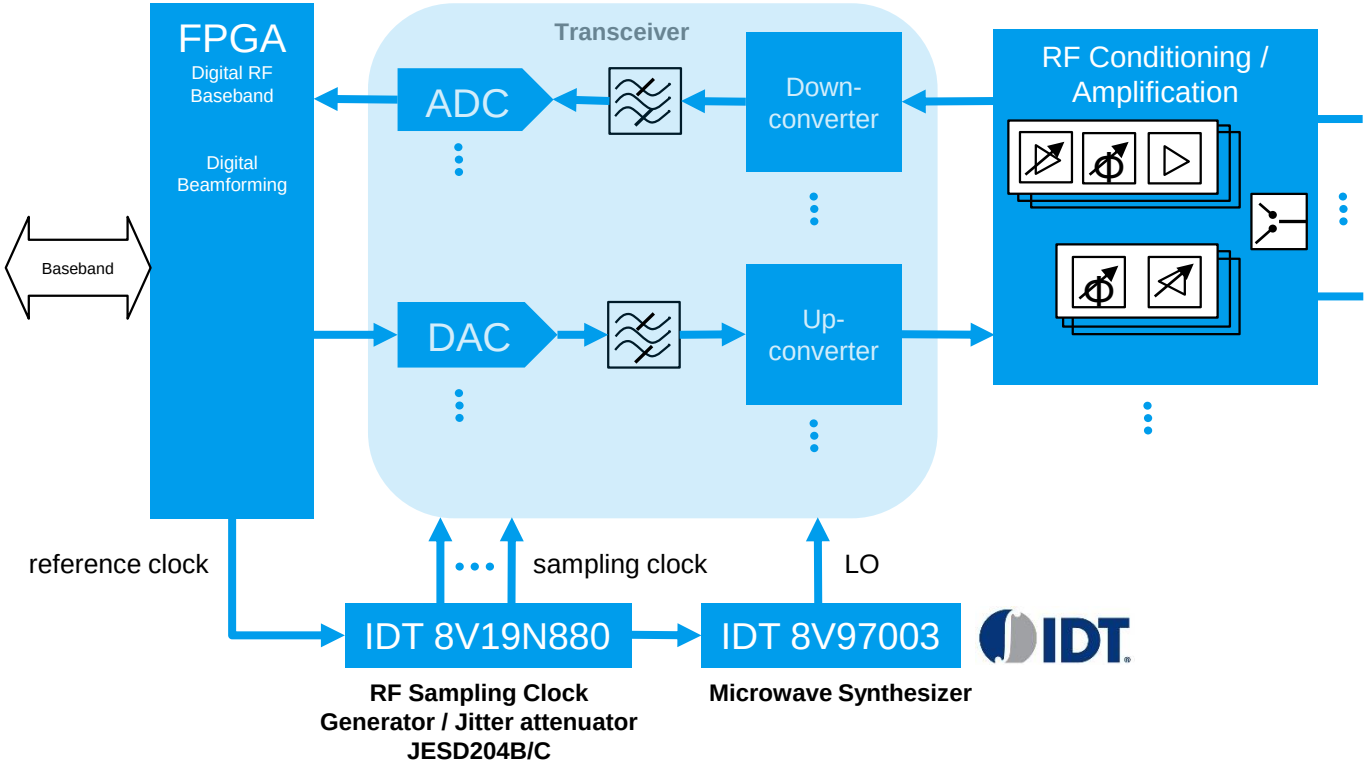
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



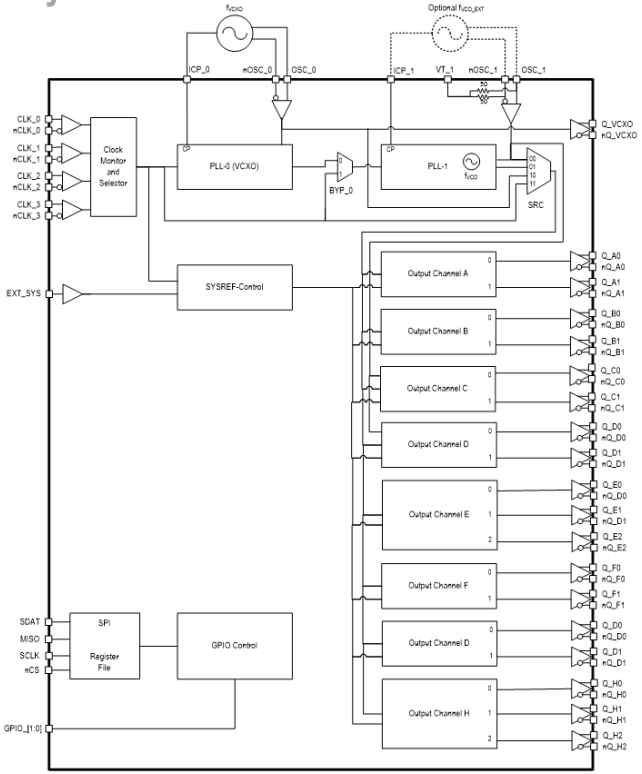
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- Output Power and Phase Noise Performance
- Spur Suppression
- Jitter Attenuation
- Signal Waveform Quality and LO Skew
- **Delay Resolution, Clock Skew and Timing**
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

IDT 8V19N880 Clock Generator / Jitter Attenuator

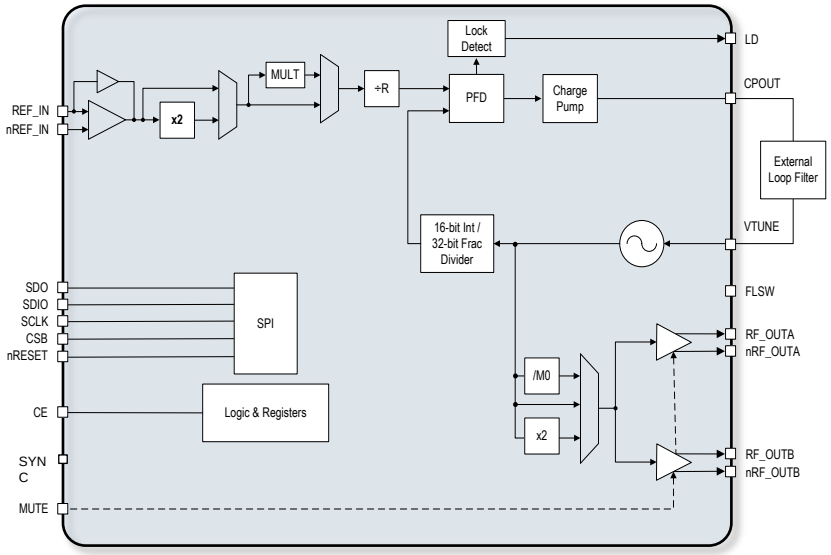
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

8V97003 18GHz Microwave Synthesizer

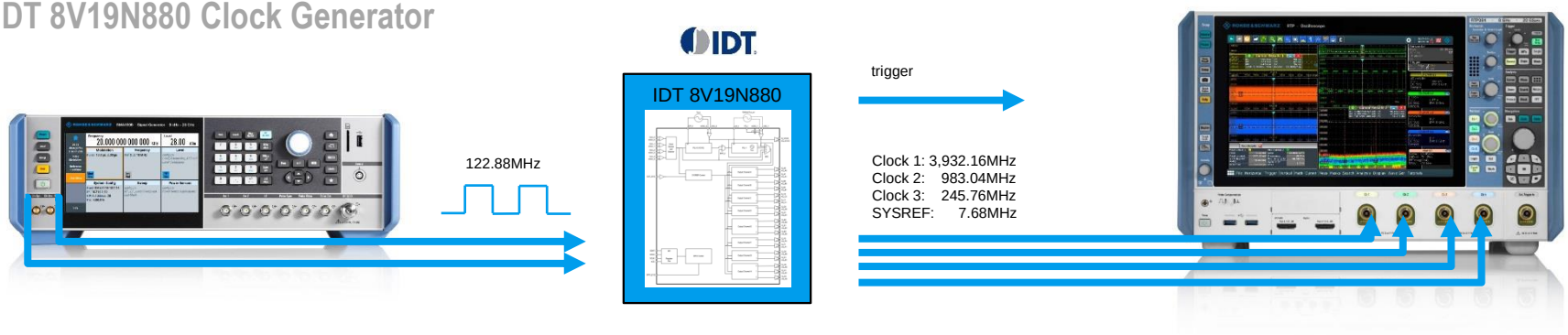
Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

Delay Resolution, Clock Skew and Timing (M4)

IDT 8V19N880 Clock Generator



R&S SMA100B

- 8kHz to 3 / 6 / 12.75 / 20GHz
- options for high and ultra high output power
- superior spectral purity:
  - ultra-low phase noise and wideband noise with several performance options
  - low harmonics, subharmonics and nonharmonics
- analog modulation (optional):
  - AM, PM, FM
- optional clock synthesizer:
  - single-ended or differential output
  - sine-wave or square wave signal

R&S RTP

- available bandwidths: 4 / 6 / 8GHz
- channels: 4
- sample rate: 20Gsamples/s
- high-class analog performance
- fastest acquisition rate: 1,000,000 wfms/s
- real-time deembedding
- digital trigger up to full bandwidth
- multi-domain functionality, incl.:
  - digital interface test
  - spectrum and signal analysis
  - power integrity
  - …

Demystifying 5G

Clock and LO Architectures in 5G Base Stations

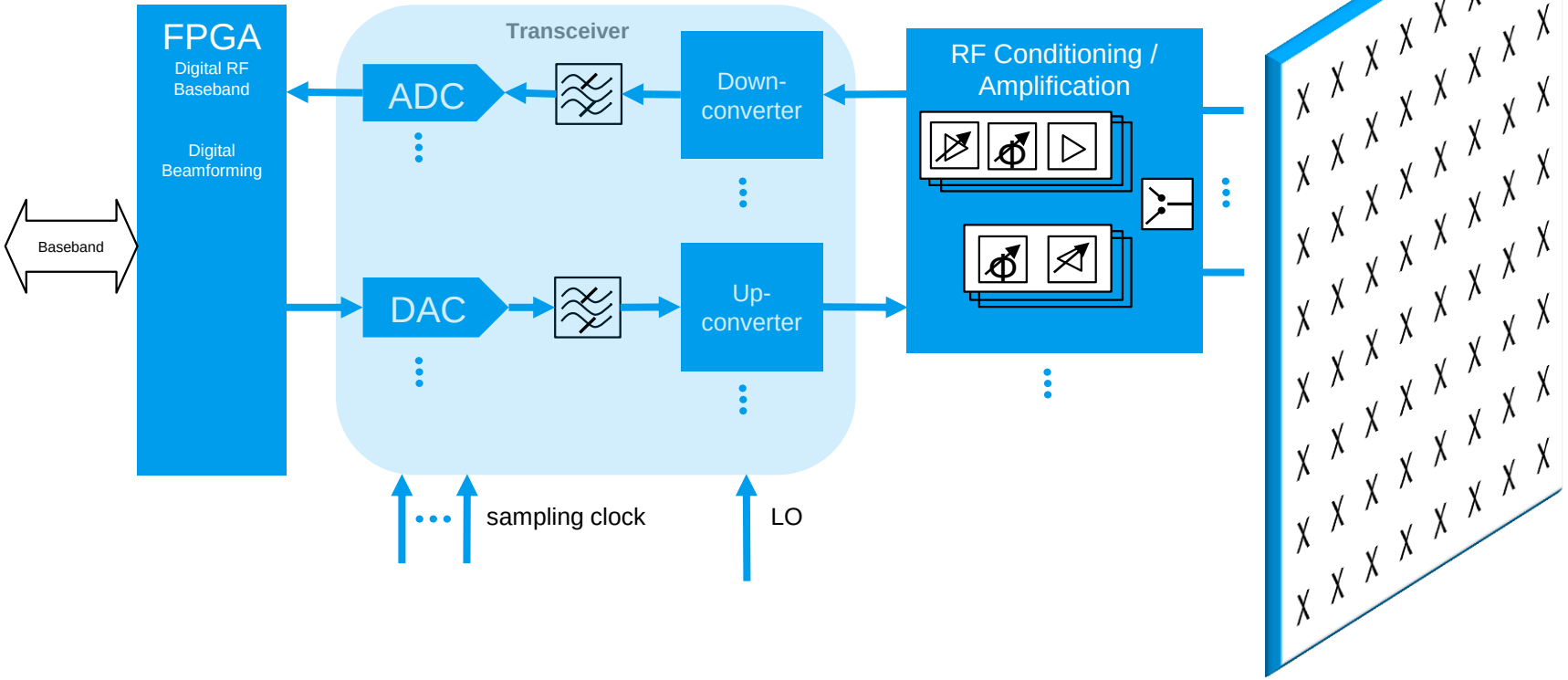
- LOS Monitoring, Hold-Over, Relocking and Phase Transients

Martin Stumpf - Market Segment Manager, R&S
Steven Gutierrez - Application Manager, IDT
Mathias Hellwig - Application Engineer, R&S

ROHDE&SCHWARZ

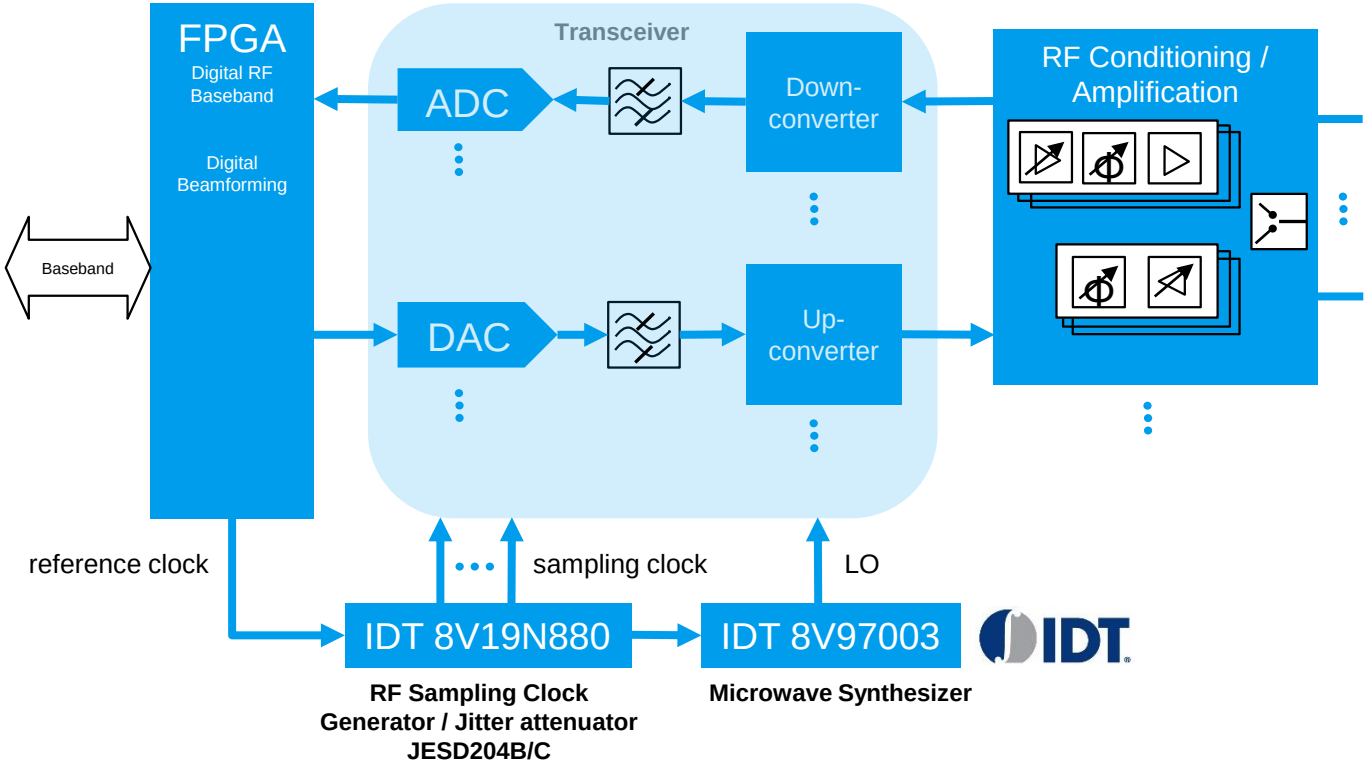
5G Base Station Architecture

Sampling Clock and LO



5G Base Station Architecture

IDT 8V19N880 and IDT 8V97003



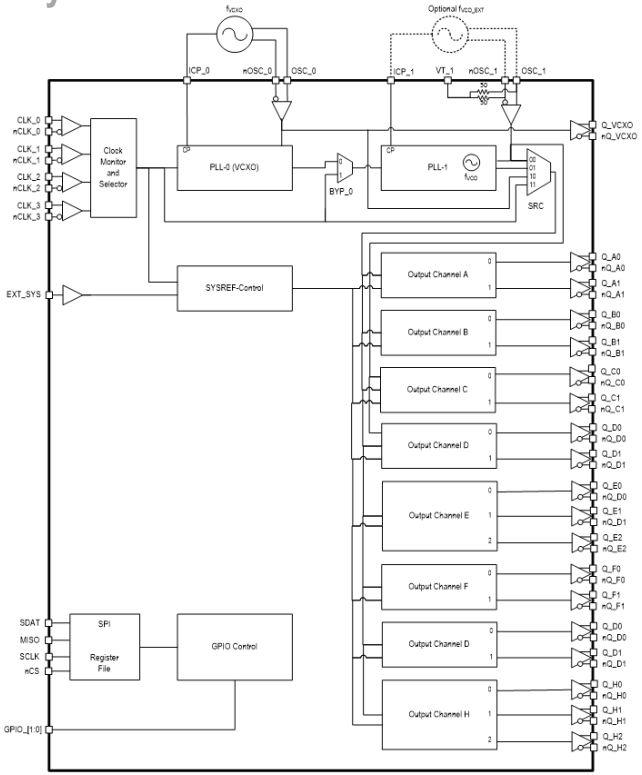
Clock and LO Architectures in 5G Base Stations

Key Performance Parameters

- Output Power and Phase Noise Performance
- Spur Suppression
- Jitter Attenuation
- Signal Waveform Quality and LO Skew
- Delay Resolution, Clock Skew and Timing
- **LOS Monitoring, Hold-Over, Relocking and Phase Transients**

IDT 8V19N880 Clock Generator / Jitter Attenuator

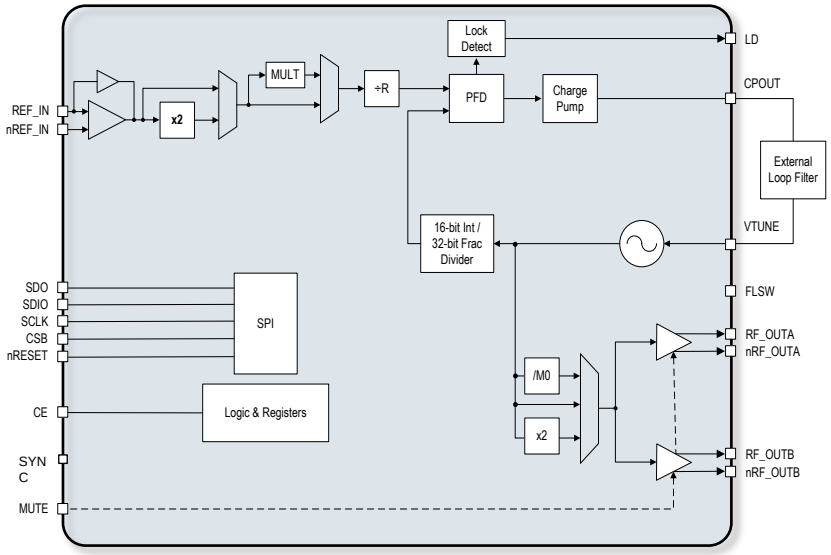
Key Performance Parameters



- Jitter attenuation of reference clock
- Generates sampling clock of ADC/DAC/transceiver components
- Designed and optimized for:
  - Low phase noise and spurious
  - Frequency generation up to 4GHz
  - JESD204B/C: SYSREF generation and phase management
- Dual PLL loop
  - PLL-0: jitter attenuation
  - PLL-1: frequency generation
- High fanout and low clock skew
  - 18 outputs (clock and SYSREF)

8V97003 18GHz Microwave Synthesizer

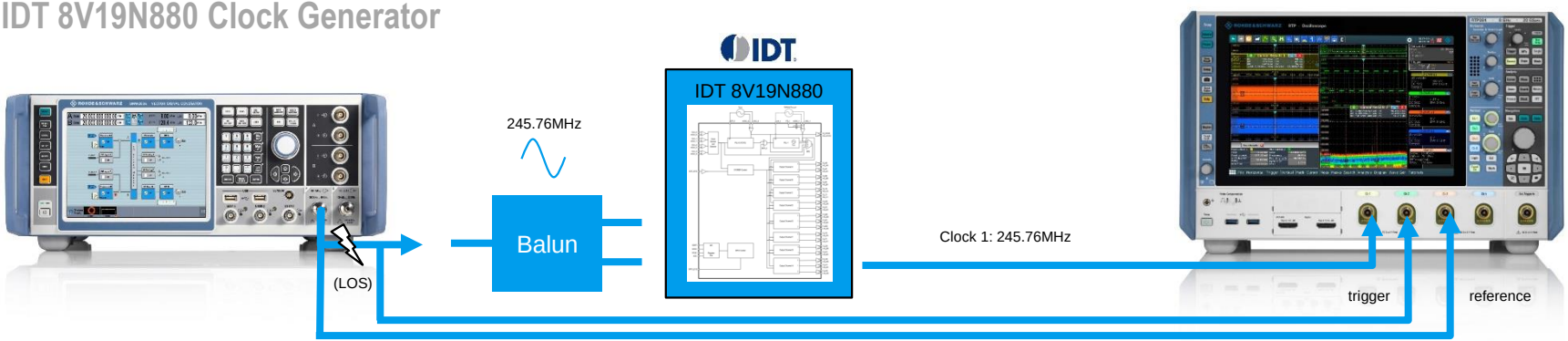
Key Performance Parameters



- RF range: 187.5 to 18,000 MHz
- Generates a high-performance reference frequency for up/down converters
- Wideband integrated VCO allows for wide and continuous output frequency range
- RMS jitter (20kHz -100 MHz) at 6GHz: -60dBc
- High output power for best output signal integrity and simplifies layout at high frequencies
- Very low skew drift contributes to reduction of radio path calibration events in beamforming applications
- +95C ambient / +105C case temperature

LOS Monitoring, Hold-Over, Relocking and Phase Transients (M5)

IDT 8V19N880 Clock Generator



R&S SMW200A

- 2 RF paths (optional):
  path A: 100kHz to 3 / 6 / 12.75 / 20 / 31.8 / 40GHz
  path B: 100kHz to 3 / 6 / 12.75 / 20GHz
- high signal purity:
  - phase noise, harmonics and spurious
- optional phase noise simulation
  - predefined and user definable phase noise profiles
- analog modulation:
  - AM, PM, FM
- digital modulation:
  - real-time and ARB based

R&S RTP

- available bandwidths: 4 / 6 / 8GHz
- channels: 4
- sample rate: 20Gsamples/s
- high-class analog performance
- fastest acquisition rate: 1,000,000 wfms/s
- real-time deembedding
- digital trigger up to full bandwidth
- multi-domain functionality, incl.:
  - digital interface test
  - spectrum and signal analysis
  - power integrity
  - …