Accurately Modeling an Advanced IC Package for Chip/Package/Board Electrical/Thermal Co-Simulation

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Abstract

Traditional electrical IR drop analysis and thermal analysis are conducted separately. That results in the inaccuracy for simulation results. To get the precise simulation results, combining local current density, joule heating and component heating together is necessary for the electrical/thermal (E/T) co-simulation. Usually system level E/T co-simulation is conducted by merging package layout with PCB layout. For advanced packages like high pin count packages or multi-chip packages, IC vendors usually do not provide the detailed package design to system designers. Instead a model is provided to represent the package design so that the intellectual properties will not be disclosed.

A new method to extract an advanced package electrical and thermal model (PETM) for system level E/T co-simulation is provided. Different simulations are done for merged package/PCB layout and PETM plus PCB layout with single die or multiple dies packages. The correlation is pretty good.

Introduction

Today's IC package becomes more and more complicated. A package with high pin count and multi chips within a small size is very common. Thermal issue becomes crucial since the power consumed by chips is increasing dramatically. Traditional considering electrical and thermal effects separately may not work since high temperature due to localized current density can cause smoke or fire hazard. On one side running just electrical simulation (IR drop) will result in under-estimated IR drop because when the trace carries current, there is a rise in temperature which lower down the conductivity and eventually increase IR drop. On other side running IR drop with uniform temperature and conductivity results into over-estimated IR drop. Hence E/T co-simulation should be the approach for any effective and accurate IR drop and thermal analysis.

The following example gives the IR drop differences in different situation:

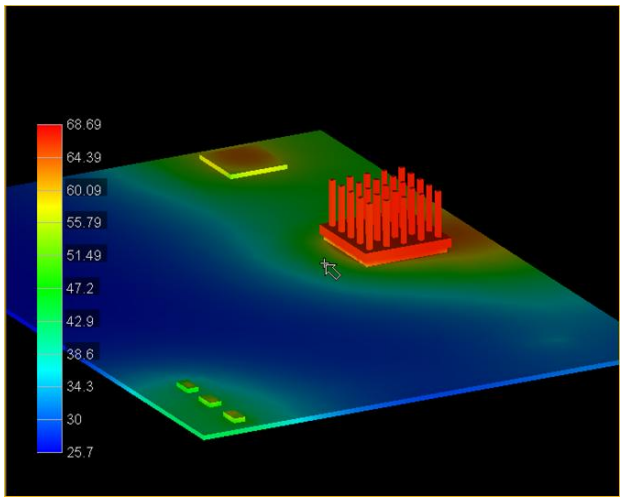

Figure 1. 3D distribution of E/T co-simulation

Sink Devices	IR drop (mV) at 25c	IR drop (mV) with Electrical-thermal co-simulation	IR drop (mV) at worst case temperature (70c)
U1	135	158	171
U2	118	138	150
U3	27	31	35
U4	27	31	35
U5	27	31	35

Table 1. Simulation results comparison

So, when doing only electrical simulation with 25 degrees, there is under-estimation (17%) of voltage drop. On other side when running with uniform conductivity and high temperature, there is over estimation (10%) of voltage drop.

Actually, the propagation of heat in an electronic system can be described electrically as equation (1):

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right)+Q=\rho c \frac{\partial T}{\partial t} \quad (1)$$

To better understand thermal analysis, we can take the heat conduction in solids as an example and use the duality of the two domains. Figure 2 and table 2 give the fundamental and basic relationships between the electrical and thermal domains.

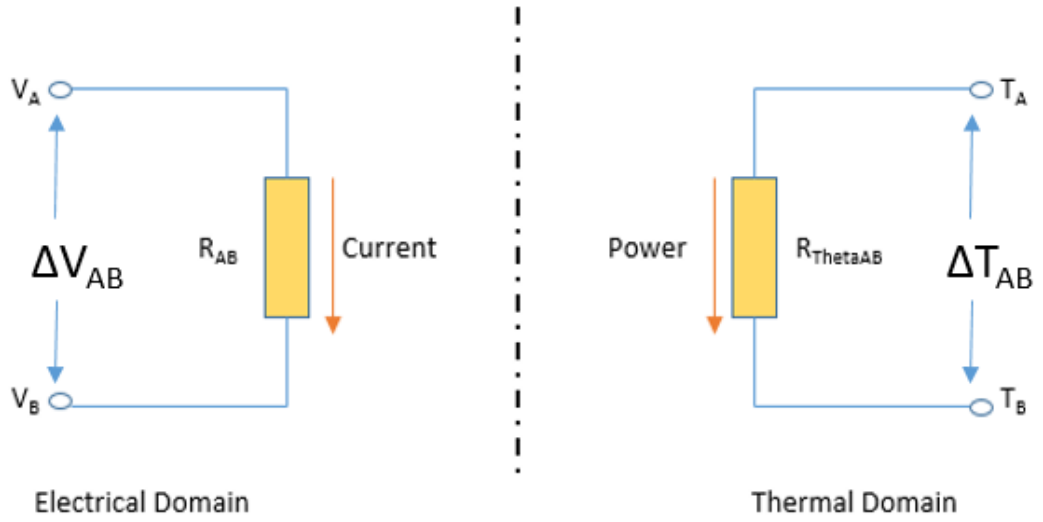

Figure 2. Fundamental relationships between the electrical domain and thermal domain

Electrical Domain			**Thermal Domain**		
Variable	Symbol	Units	Variable	Symbol	Units
Voltage	V	Volts	Temperature	T	^{o}C or K
Current	I	Amperes or Coulombs/s	Power or Heat Flux	$P_{D\ or}$ Q	Watts or Joules/s
Resistance	R	Ohms	Thermal resistance	$R_{ThetaAB}$	^{o}C/W or K/W
Capacitance	C	Farads or Coulombs/V	Thermal capacitance	C_{Theta}	Joules/ ^{o}C
$\Delta V_{AB}=V_A-V_B=I*R_{AB}$			$\Delta T_{AB}=T_A-T_B=P_D* R_{ThetaAB}$		

Table 2. Basic relationships between the electrical domain and thermal domain

For chip/package/board system E/T co-simulation, the traditional analysis algorithm is to use finite element method (FEM) to solve the layout design by merging package and PCB board together. Since the IP issue, system designers are difficult to get the package design for system level chip/package/board E/T co-simulation. Using an equivalent model to represent the package is a normal choice like compact electrical/thermal models. Pin based resistance network is relatively easy to extract and it works accurately for a package IR drop analysis, but the package thermal resistance characterization is much more difficult to balance the accuracy and computing complexity. This paper proposes a new method named Package Electrical Thermal Modeling(PETM) to extract both electrical and thermal compact models at the same time to ensure the accuracy for system level E/T co-simulation.

Methodology of Modeling an IC Package

For electrical/thermal co-extraction, the 2-resistor compact thermal model (CTM) is too simple and inaccurate, even the DELPHI model does not work well for advanced package. The multi-terminal resistance network and thermal resistance network are needed. The approaches of electrical/thermal model co-extraction for a complicated package are developed by combining IR drop and thermal analysis together, using Cadence patented

E/T co-simulation technologies. Three methods to define terminals of a component are provided: pin-base, grid-base and net-base. Users can determine the terminals for electrical model and thermal model based on the design complexity and the accuracy. Multiple terminals are defined at component pins and substrate layers. For resistance network, terminals will be defined at component pin locations. Net based terminals will group all pins with the same net together as one terminal, this will reduce the model, but the accuracy is not high. Pin based terminals will have the highest accuracy for the model but also increase the complexity of the model. For thermal resistance network, terminals need to be defined both component pin locations and package substrate layers. For a substrate layer, we can define the terminals based on the grids. For example, we can define 5x5 grids as terminals for a single layer. To have the high accuracy for a model, we can use the package solder balls and die bumps as terminals to create a resistance network. For thermal resistance network, the terminals are defined at package solder balls and die bumps (pin-base) and package substrate layers(grid-base). See figure 3.

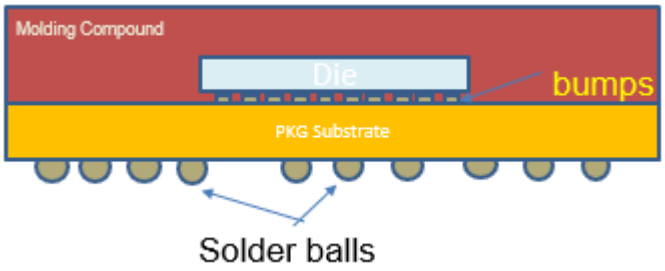

Figure 3. Terminal defining for a package

Both electrical and thermal resistance networks will be combined into one single model file. System designers can directly use the PETM model for chip/package/board co-simulation. The PETM can include the solder balls/bumps effects if needed.

To verify the accuracy of the package electrical thermal model, the simulation results with PETM on PCB including the IR drop, current density and temperature distributions are correlated with those by FEM for the merged package and PCB layouts. The differences are very small.

Results and Conclusions

A test case is used for this study:

- 6 layers package
- 4-layer PCB
  - Top
  - Plane02
  - Plane03
  - Bottom
- Multi-dies

- Ambient temperature:25C
- Power dissipation: DDR3~1W; CPU~1.9W; Flash~1W
- Sink currents: core power~10A; DDR3 1.5V~2A; Flash 2.5V~2A

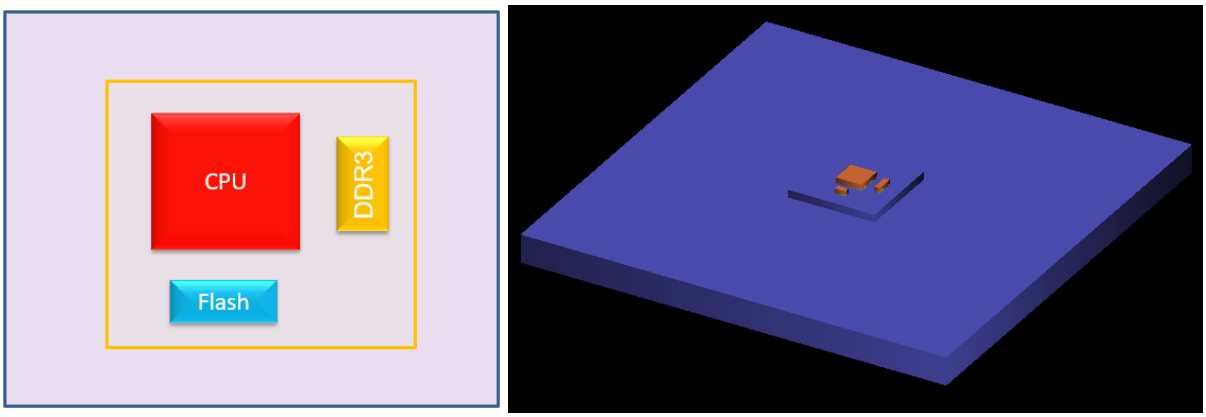

Figure 4. Example design

The study includes:

1. Merging package with PCB and using FEM to do E/T co-simulation and checking the voltage drop/current density/temperature distributions on the PCB layers
    a. Calculating Theta Jb and Theta Jc for the package
2. Extracting package PETM model for the merged designs
    a. Resistance network
    b. Thermal resistance network
3. Using PETM model on the same PCB for E/T co-simulation
4. Using Theta Jb and Theta Jc and the resistance network on the same PCB for E/T co-simulation
5. Repeating above tasks by enabling one die, two dies and three dies

Based on above simulation results, we compared the voltage drop, current density and temperature on each PCB layer, the results are as following:

One die enabled package:

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	535.474nV	1.40276mV	531.757nV	1.38783mV	-0.69~-0.43	531.757nV	1.38783mV	-0.69~-0.43
Plane02 Layer	15.574uV	1.2015 mV	15.5703uV	1.20088mV	-0.024~-0.062	15.5703uV	1.20088mV	-0.024~-0.062
Plane03 Layer	535.474nV	1.2088 mV	531.757nV	1.20894mV	-0.69~0.01	531.757nV	1.20894mV	-0.69~0.01
Bottom Layer	0V	1.20882mV	0V	1.20894mV	0~0.01	0V	1.20894mV	0~0.01

Table 3. IR drop results on PCB layers with single-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	0.2474 mA/mm2	7.66122 A/mm2	0.248039 mA/mm2	7.30418 A/mm2	0.25 ~ -4.66	0.248039 mA/mm2	7.30418 A/mm2	0.25 ~ -4.66
Plane02 Layer	0 A/mm2	15.111 A/mm2	0 A/mm2	15.1103 A/mm2	0 ~ -0.005	0 A/mm2	15.1103 A/mm2	0~ -0.005
Plane03 Layer	0 A/mm2	15.4063 A/mm2	0 A/mm2	15.4058 A/mm2	0 ~ -0.003	0 A/mm2	15.4058 A/mm2	0 ~ -0.003
Bottom Layer	0 A/mm2	0.95368 A/mm2	0 A/mm2	0.953649 A/mm2	0 ~ -0.003	0 A/mm2	0.953649 A/mm2	0 ~ -0.003

Table 4. Current density results on PCB layers with single-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference %	Min	Max	Difference%
Top Layer	26.6227C	41.1735C	26.5675C	39.9504C	-0.21 ~ -2.88	26.6328C	37.9752C	0.04 ~ -7.77
Plane02 Layer	26.6358C	38.1922C	26.5796C	37.7308C	-0.21 ~ -1.21	26.6454C	35.7604C	0.036 ~ 6.37
Plane03 Layer	26.6432C	37.5607C	26.5853C	37.6288C	-0.22 ~ 0.18	26.6514C	35.6453C	0.03 ~ -5.1
Bottom Layer	26.6364C	37.5393C	26.5786C	37.6202C	-0.22 ~ 0.22	26.6445C	35.6412C	0.03 ~ -5.06

Temperature

Table 5. Temperature results on PCB layers with single-die package model

Two dies enabled package:

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	2.30641uV	15.1269mV	2.30658uV	15.0622mV	0.007~-0.43	2.30658uV	15.0622mV	0.007~-0.43
Plane02 Layer	136.037uV	7.03396mV	136.037uV	7.03541mV	0~-0.02	136.037uV	7.03541mV	0~-0.02
Plane03 Layer	321.416nV-	14.311mV	305.839nV	14.3089mV	-4.85~-0.01	305.839nV	14.3089mV	-4.85~-0.01
Bottom Layer	0V	14.311mV	0V	14.3089mV	0~-0.01	0V	14.3089mV	0~-0.01

Voltage Drop

Table 6. IR drop results on PCB layers with two-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	7.55136mA/mm2	40.5832A/mm2	7.55145 mA/mm2	38.8896 A/mm2	0. 0009~ -0.04	7.55145 mA/mm2	38.8896 A/mm2	0. 0009~ -0.04
Plane02 Layer	0 A/mm2	98.8423 A/mm2	0 A/mm2	98.843 A/mm2	0 ~ 0.0007	0 A/mm2	98.843 A/mm2	0 ~ 0.0007
Plane03 Layer	0 A/mm2	162.037 A/mm2	0 A/mm2	162.04 A/mm2	0 ~ 0.0018	0 A/mm2	162.04 A/mm2	0 ~ 0.0018
Bottom Layer	0 A/mm2	6.22799 A/mm2	0 A/mm2	6.228 A/mm2	0 ~ 0.0016	0 A/mm2	6.228 A/mm2	0 ~ 0.0016

Table 7. Current density results on PCB layers with two-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	30.3352C	65.1875C	30.7781C	64.2049C	1.46 ~ -1.5	32.2025C	77.9787C	6.16 ~ 19.62
Plane02 Layer	30.3781C	63.4237C	30.8227C	62.0951C	1.46~-2.09	32.258C	70.6339C	6.19 ~ 11.37
Plane03 Layer	30.4027C	62.7613C	30.8438C	61.9574C	1.45 ~ -1.28	32.2844C	70.2099C	6.19 ~ 11.87
Bottom Layer	30.3801C	62.725C	30.8193C	61.9491C	1.45 ~ -1.24	32.2538C	70.196C	6.17 ~ 11.91

Table 8. Temperature results on PCB layers with two-die package model

Three dies enabled package:

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	2.25052uV	15.1255mV	2.2508uV	15.0608mV	0.012~-0.43	2.2508uV	15.0608mV	0.012~-0.43
Plane02 Layer	135.848uV	7.6103mV	135.848uV	7.61131mV	0 ~ 0.013	135.848uV	7.61131mV	0 ~ 0.013
Plane03 Layer	0.648459uV	14.3096mV	0.67202uV	14.3075mV	3.63~ -0.015	0.67202uV	14.3075mV	3.63~ -0.015
Bottom Layer	0V	14.3096mV	0V	14.3075mV	0~-0.01	0V	14.3075mV	0~-0.01

Table 9. IR drop results on PCB layers with three-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	7.56079 mA/mm	40.5831 A/mm2	7.56088 mA/mm2	38.8994 A/mm2	0.001~ -4.15	7.56088 mA/mm2	38.8994 A/mm2	0.001 ~-4.15
Plane02 Layer	0 A/mm2	99.0298 A/mm2	0 A/mm2	99.0302 A/mm2	0 ~ 0.0004	0 A/mm2	99.0302 A/mm2	0~ 0.0004
Plane03 Layer	0 A/mm2	162.034 A/mm2	0 A/mm2	162.037 A/mm2	0 ~0.0019	0 A/mm2	162.037 A/mm2	0 ~0.0019
Bottom Layer	0 A/mm2	6.23648 A/mm2	0 A/mm2	6.23648 A/mm2	0 ~ 0	0 A/mm2	6.23648 A/mm2	0 ~ 0

Table 10. Current density results on PCB layers with three-die package model

	FEM		PETM			2-R CTM		
	Min	Max	Min	Max	Difference%	Min	Max	Difference%
Top Layer	32.0426	77.0401C	30.5246C	74.7055C	-4.74 ~ -3.03	34.2308C	93.2286C	6.83 ~ 21.01
Plane02 Layer	32.0992C	75.1669C	30.5672C	69.0727	-4.77 ~ -8.11	34.302C	83.5966C	6.86 ~ 11.21
Plane03 Layer	32.1315C	74.5688C	30.5874C	68.882C	-4.81 ~-7.63	34.3357C	83.0437C	6.86 ~ 11.37
Bottom Layer	32.1018C	74.5513C	30.5639C	68.8673C	-4.79 ~ -7.62	34.2965C	83.0255C	6.84 ~ 11.22

Table 11. Temperature results on PCB layers with three-die package model

From the simulation results above, we can find component pin based PETM models work very accurate for system level IR drop analysis for all kinds of package designs, no matter single die or multiple dies included. For thermal analysis or E/T co-simulation, simple 2 resistor CMT model may work for the simple package designs but it does not work accurately for advanced package designs. However, PETM package models still work accurately for thermal analysis or E/T co-simulation in system level analysis for both simple or advanced packages.